# Port A Wait Support for the DP8420A/21A/22A, DP8420V/21V/22V, DP84T22V, DP8430V/31V/32V, DP8520A/21A/22A and NS32CG821A DRAM Controllers

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Port A Wait Support for the DP8420A/21A/22A, DP8420V/21V/22V, DP84T22V, DP8430V/31V/32V, DP8520A/21A/22A and NS32CG821A DRAM Controllers

AN-773

## INTRODUCTION

This application brief looks into the wait support offered by the above DRAM controllers. All of these controllers behave in the same way with respect to the insertion of wait states; therefore, this application brief is valid to any and all of them.

Wait states are necessary for interfacing fast microprocessors with slower memory or I/O devices. CPU manufacturers name differently their Wait or Ready input line, however, any CPU's Wait or Ready input is compatible to either the $\overline{\text{WAIT}}$ or $\overline{\text{DTACK}}$ output from these DRAM controllers. These outputs basically extend the normal CPU cycle to ensure: 1) that valid data is on the data bus before the CPU latches this information into its registers, (in the read cycle) and 2) that data is long enough on the data bus for the data to be copied into memory before the CPU take this data of the bus, (in the write cycle).

Both $\overline{\text{WAIT}}$ and $\overline{\text{DTACK}}$ signals are active low but with different meaning. $\overline{\text{WAIT}}$ asserted means that while this output is low wait states will be inserted in the memory cycle. $\overline{\text{DTACK}}$ asserted means that when this output is low the transfer has taken place and the memory cycle may be finished by the CPU.

The user must first decide which kind of output is required by the CPU in his or her application, and program the DRAM controller accordingly (programming bit R7).

For example, the 68000/08/10/20/30/40 and i286/i386/i486 uses a $\overline{\text{READY}}$ input active low, (named differently by each CPU). This input asserted indicates to the microprocessor that data has been written into memory or that valid data is on the bus for the CPU to latch into its registers. In the case of a memory cycle, the DRAM controller must keep this signal high and assert it low when it is ready to indicate that the access may finish. As long as the CPU samples this signal high, wait states will be inserted into the access cycle. These microprocessors can use the $\overline{\text{DTACK}}$ type output from the DRC.

On the other hand, Intel's 8086/8088/186 and NSC's NS32008/016/132, to name a few, use the READY input active high. When this signal is sampled high by the microprocessor, it indicates that the transfer can be finished. In the case of a memory cycle, the DRAM controller must keep the signal low and assert it high when it is ready to indicate that the access may finish. While this signal is sampled low by the CPU, wait states will be inserted in the access cycle. These microprocessors can use the $\overline{\text{WAIT}}$ type output from these DRAM controllers.

A microprocessor may request a memory access while the DRAM controller is in the middle of a refresh cycle, in the middle of precharge for the previous access, while a Port B access is in progress, or when the DRAM controller is idle or free. In any case, the DRAM controller arbitrates between accesses, refreshes and precharge, and two situations may arise: 1) A Delayed Access meaning that a refresh cycle, precharge time or other access was in progress when the access was requested. And 2) A Non-Delayed Access which means that no refresh cycle, precharge time or other access were in progress when the access was requested.

## NON-DELAYED ACCESS

If $\overline{\text{WAIT}}$ is selected, the DRAM controller will assert this output, normally high, if and only if wait states are programmed. The CPU will prolong the access cycle for as long as $\overline{\text{WAIT}}$ is asserted low. The DRAM controller will bring $\overline{\text{WAIT}}$ high after the programmed wait states allowing the CPU to finish the memory access. If no wait states were programmed, the DRAM controller will keep $\overline{\text{WAIT}}$ high and the CPU will read or write data at the usual CPU cycle.

If $\overline{\text{DTACK}}$ is selected and because this output is normally high, the DRAM controller will always assert this output to indicate the end of the access. If wait states are programmed, the DRAM controller will assert $\overline{\text{DTACK}}$ after the programmed wait states. If no wait states are programmed the DRAM controller will assert $\overline{\text{DTACK}}$ at the beginning of the access from $\overline{\text{CS}}$ and $\overline{\text{ADS}}$ (ALE) asserted.

## DELAYED ACCESS

If **$\overline{\text{WAIT}}$** is selected, the DRAM controller will assert this output immediately from the access request by $\overline{\text{CS}}$ and $\overline{\text{ADS}}$ (ALE). This will insert wait states allowing precharge or the refresh cycle to finish. After precharge or the refresh cycle is over, the previously requested access will start by asserting $\overline{\text{RAS}}$, at that time the $\overline{\text{WAIT}}$ output will follow the programming selection on bits R2, R3.

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If $\overline{\text{DTACK}}$ is selected, the DRAM controller will keep this output negated high allowing precharge or the refresh cycle to finish. After precharge or the refresh cycle is over, the previously requested access will start by asserting $\overline{\text{RAS}}$, at that time the $\overline{\text{DTACK}}$ output will follow the programming selection on bits R2, R3.

The user may choose to read only the section regarding his particular design, $\overline{\text{WAIT}}$ Type Output or $\overline{\text{DTACK}}$ Type Output. In each section 4 possible programming selections are shown. Every programming selection explains the behavior of Mode 0 and Mode 1. In each mode the access can be Non Delayed or Delayed. See table below.

| | | $\overline{\text{WAIT}}$ Output Selected | | | | $\overline{\text{DTACK}}$ Output Selected | | | |
|---|---|---|---|---|---|---|---|---|---|
| R3 | R2 | Mode 0 | | Mode1 | | Mode 0 | | Mode 1 | |
| | | Non-Delayed | Delayed | Non-Delayed | Delayed | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 0 | 0 | 0T | 0T | 0T | 0T | 0T | 0T | 0T | 0T |
| 0 | 1 | 0T | ½T | 0T | ½T | ½T | ½T | ½T | ½T |
| 1 | 0 | ½T | ½T | ½T | ½T | 1T | 1T | 1T | 1T |
| 1 | 1 | 1T | 1T | 1T | 1T | 1½T | 1½T | 1½T | 1½T |

## $\overline{\text{WAIT}}$ AND $\overline{\text{DTACK}}$ SUPPORT

### $\overline{\text{Wait}}$ During Single Accesses

$\overline{\text{WAIT}}$ can be programmed to delay a number of positive edges and/or negative levels of CLK. These options are programmed through address bits R2 and R3 at programming time. The user is given four options described below:

| R3 | R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|---|
| | | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 0 | 0 | 0T | 0T | 0T | 0T |

0T during non-delayed and delayed acceses. During a non-delayed access, $\overline{\text{WAIT}}$ will stay negated as shown in *Figures 1a* and *1b*.

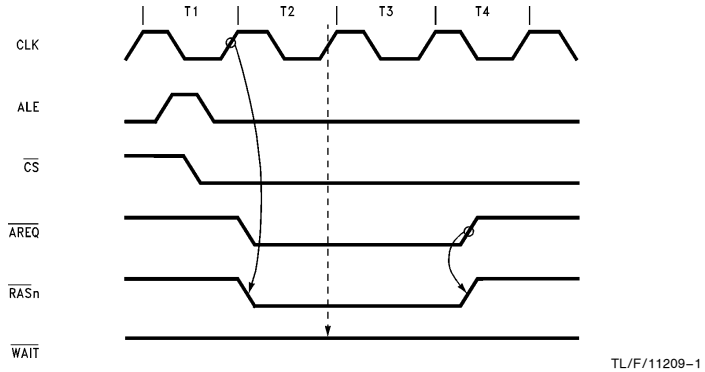


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**FIGURE 1a. Mode 0 Non-Delayed Access with $\overline{\text{WAIT}}$ 0T ($\overline{\text{WAIT}}$ is Sampled at the End of the "T2" Clock State)**

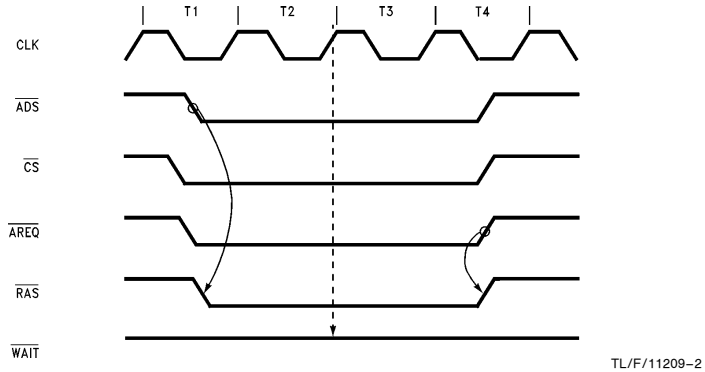


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**FIGURE 1b. Mode 1 Non-Delayed Access with $\overline{\text{WAIT}}$ 0T ($\overline{\text{WAIT}}$ is Sampled at the End of the "T2" Clock State)**

During an access that is delayed, $\overline{WAIT}$ will assert at the start of the access ($\overline{CS}$ and ALE or $\overline{ADS}$) and it will negate from the positive edge of $\overline{CLK}$ that starts $\overline{RAS}$ for that access as shown in *Figures 1c* and *1d*.

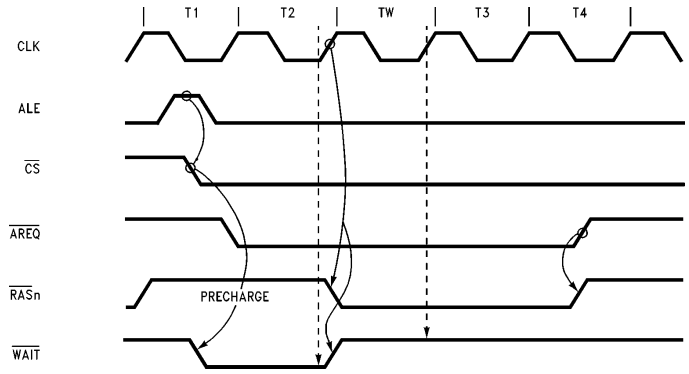


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**FIGURE 1c. Mode 0 Delayed Access with $\overline{WAIT}$ 0T ("2T" $\overline{RAS}$ Precharge, $\overline{WAIT}$ is Sampled at the End of the "T2" Clock State)**

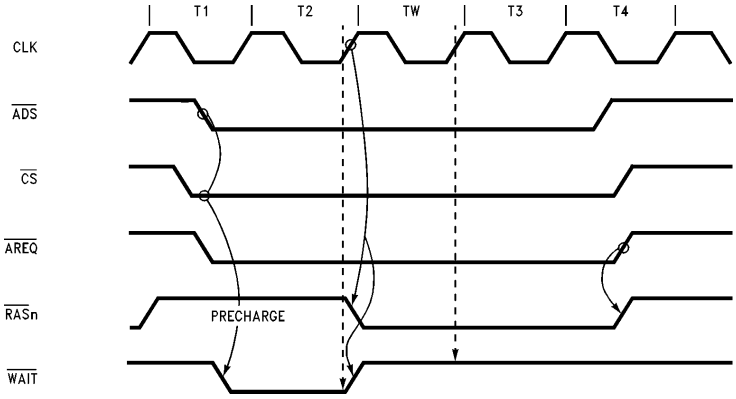


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**FIGURE 1d. Mode 1 Delayed Access with $\overline{WAIT}$ 0T ($\overline{WAIT}$ is Sampled at the End of the "T2" Clock State)**

| R3 | R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|---|
| | | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 0 | 1 | 0T | ½T | 0T | ½T |

0T during non-delayed accesses and ½T during delayed accesses. During a non-delayed access, $\overline{WAIT}$ will stay negated as shown in *Figures 2a* and *2b*.

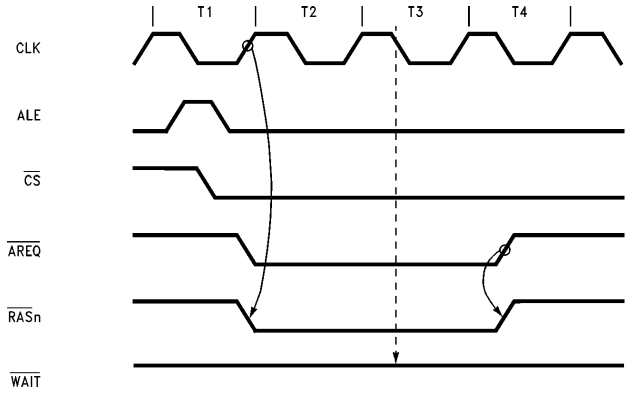


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**FIGURE 2a. Mode 0 Non-Delayed Access with $\overline{WAIT}$ 0T ($\overline{WAIT}$ is Sampled at the "T3" Falling Clock Edge)**

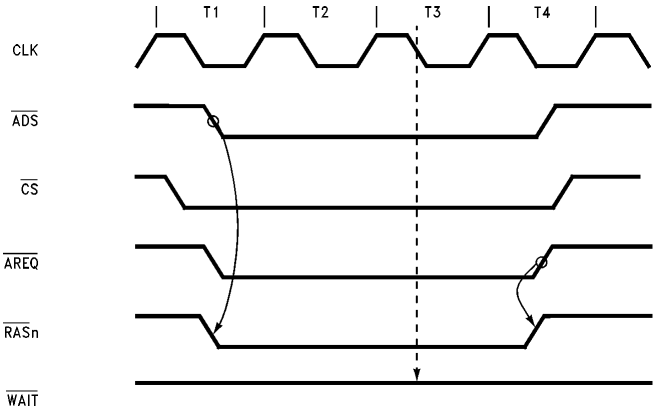


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**FIGURE 2b. Mode 1 Non-Delayed Access with $\overline{WAIT}$ 0T ($\overline{WAIT}$ is Sampled at the "T3" Falling Clock Edge)**

During an access that is delayed, $\overline{WAIT}$ will assert at the start of the access ($\overline{CS}$ and ALE or $\overline{ADS}$) and $\overline{WAIT}$ will negate on the negative level of CLK after the positive edge of CLK that asserted $\overline{RAS}$ for that access, as shown in *Figures 2c* and *2d*.

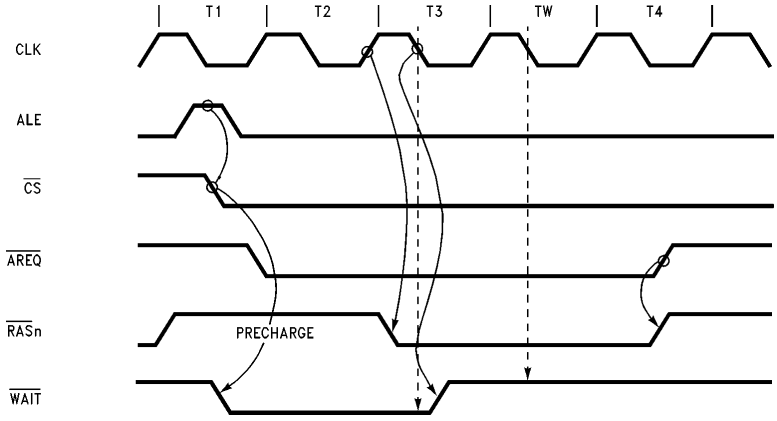


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**FIGURE 2c. Mode 0 Delayed Access with $\overline{WAIT}$ ½T ($\overline{WAIT}$ is Sampled at the "T3" Falling Clock Edge)**

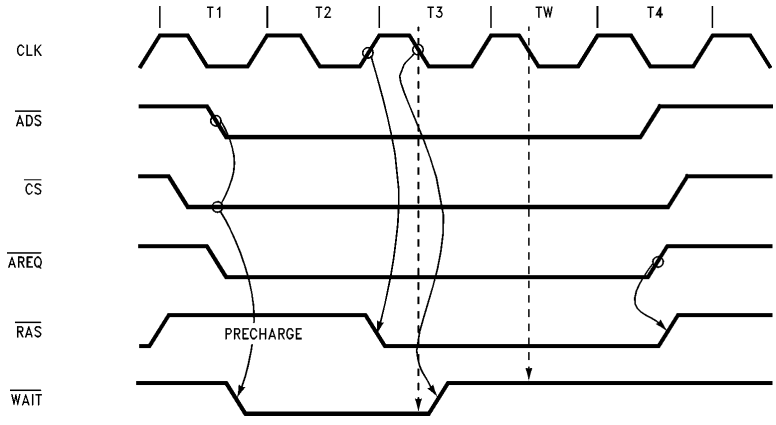


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**FIGURE 2d. Mode 1 Delayed Access with $\overline{WAIT}$ ½T ($\overline{WAIT}$ is Sampled at the "T3" Falling Clock Edge)**

| R3 | R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|---|
| | | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 1 | 0 | ½T | ½T | ½T | ½T |

½T during non-delayed and delayed accesses. If mode 0 is used, $\overline{WAIT}$ will assert when ALE is asserted and $\overline{CS}$ is asserted. $\overline{WAIT}$ will then negate on the negative level of CLK after the positive edge of CLK that asserts $\overline{RAS}$ for the access as shown in *Figure 3a*.

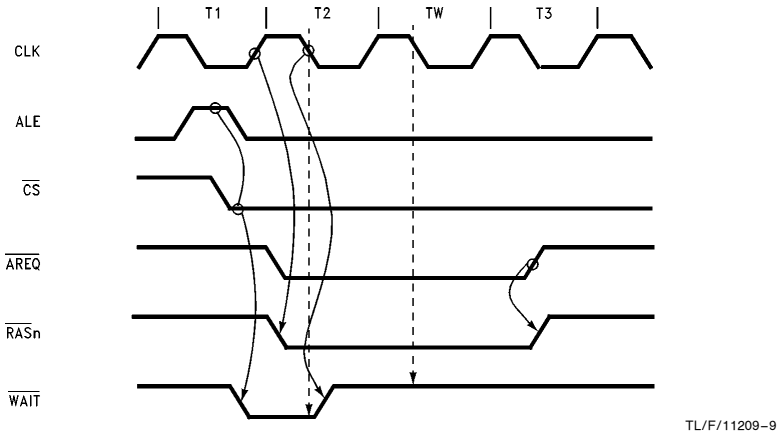


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**FIGURE 3a. Mode 0 Non-Delayed Access with $\overline{WAIT}$ ½T ($\overline{WAIT}$ is Sampled at the "T2" Falling Clock Edge)**

If Mode 1 is used, $\overline{WAIT}$ will assert from $\overline{CS}$ asserted and $\overline{ADS}$ asserted. $\overline{WAIT}$ will then negate on the negative level of CLK after $\overline{RAS}$ has been asserted for the access as shown in *Figure 3b*.

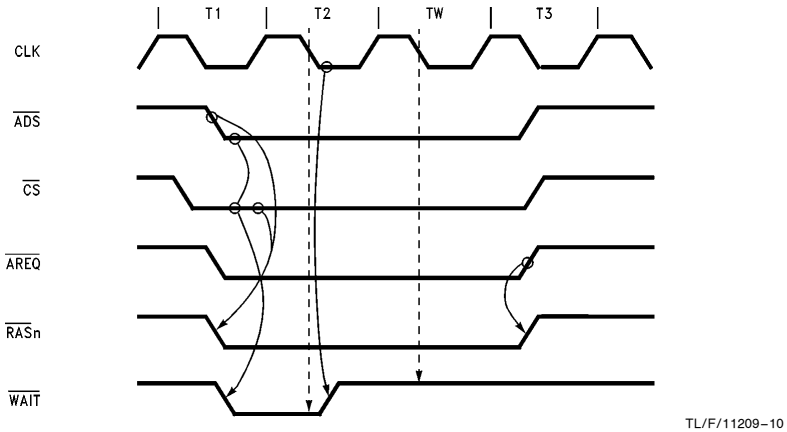


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**FIGURE 3b. MODE 1 Non-Delayed Access with $\overline{WAIT}$ ½T ($\overline{WAIT}$ is Sampled at the "T2" Falling Clock Edge)**

During delayed accesses, in both modes, $\overline{WAIT}$ will assert at the start of the access and negate on the negative level of CLK after the positive edge of CLK that started $\overline{RAS}$ for that access as shown in *Figures 3c* and *3d*.

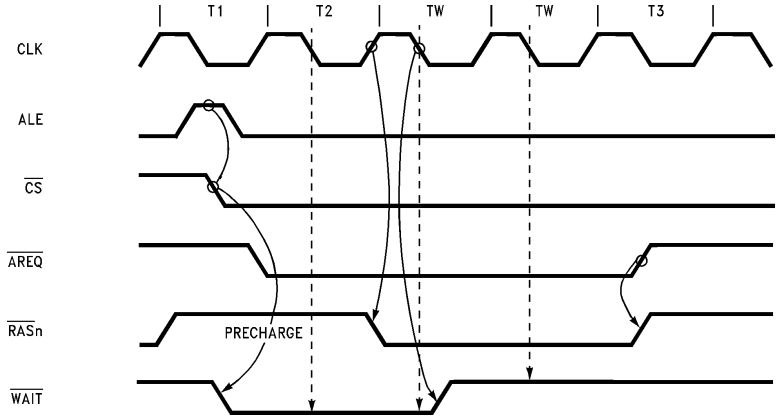


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**FIGURE 3c. Mode 0 Delayed Access with $\overline{WAIT}$ ½T ($\overline{WAIT}$ is Sampled at the "T2" Falling Clock Edge)**

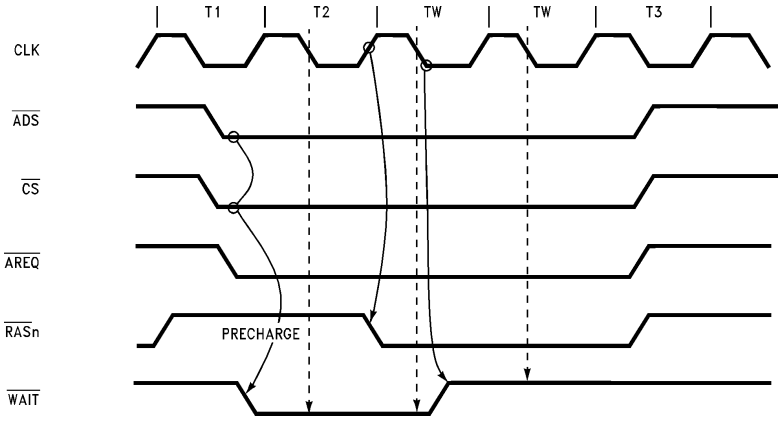


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**FIGURE 3d. Mode 1 Delayed Access with $\overline{WAIT}$ ½T ($\overline{WAIT}$ is Sampled at the "T2" Falling Clock Edge)**

| R3 | R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|---|
| | | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 1 | 1 | 1T | 1T | 1T | 1T |

1T during non-delayed and delayed accesses. In Mode 0, $\overline{WAIT}$ will assert from ALE asserted and $\overline{CS}$ asserted. $\overline{WAIT}$ will negate from the next positive edge of CLK that asserts $\overline{RAS}$ for that access as shown in *Figure 4a*.

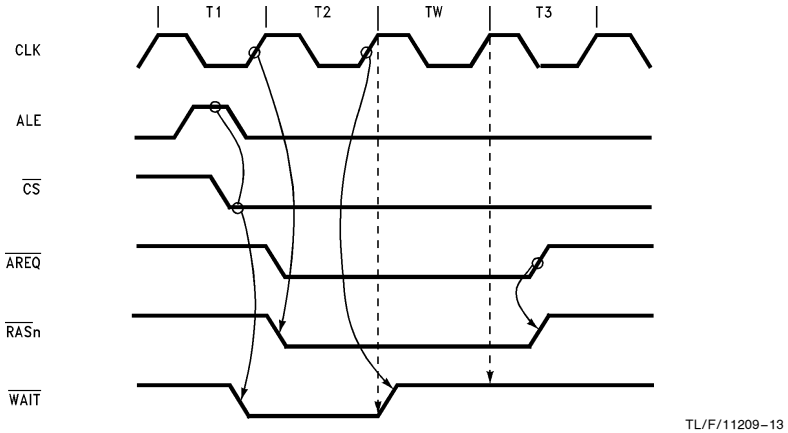


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**FIGURE 4a. Mode 0 Non-Delayed Access with $\overline{WAIT}$ 1T ($\overline{WAIT}$ is Sampled at the End of the "T2" Clock State)**

In Mode 1, $\overline{WAIT}$ will assert from $\overline{ADS}$ asserted and $\overline{CS}$ asserted. $\overline{WAIT}$ will negate from the first positive edge of CLK after $\overline{ADS}$ and $\overline{CS}$ have been asserted as shown in *Figure 4b*.

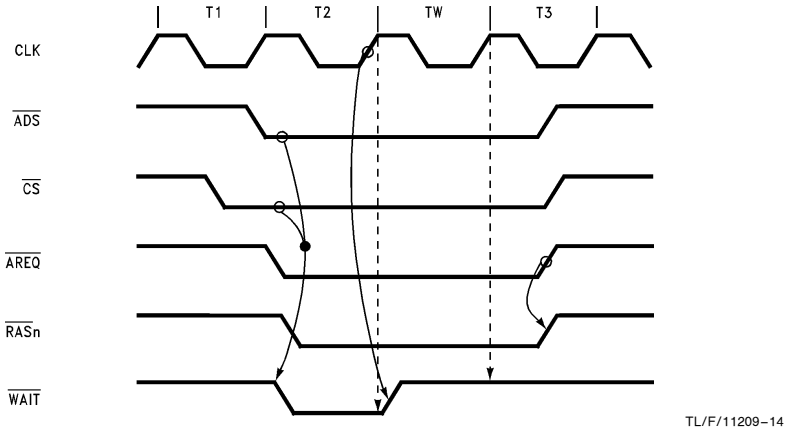


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**FIGURE 4b. Mode 1 Non-Delayed Access with $\overline{WAIT}$ 1T ($\overline{WAIT}$ is Sampled at the End of the "T2" Clock State)**

During delayed accesses in both modes, $\overline{WAIT}$ will assert at the beginning of the access and will negate on the next positive edge of CLK after the positive edge of CLK that starts $\overline{RAS}$ for that access as shown in *Figures 4c* and *4d*.

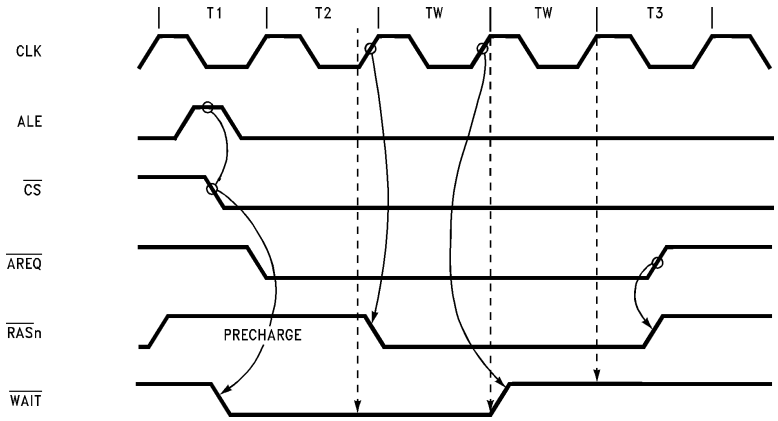


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**FIGURE 4c. Mode 0 Delayed Access with $\overline{WAIT}$ 1T ($\overline{WAIT}$ is Sampled at the End of the "T2" Clock State)**

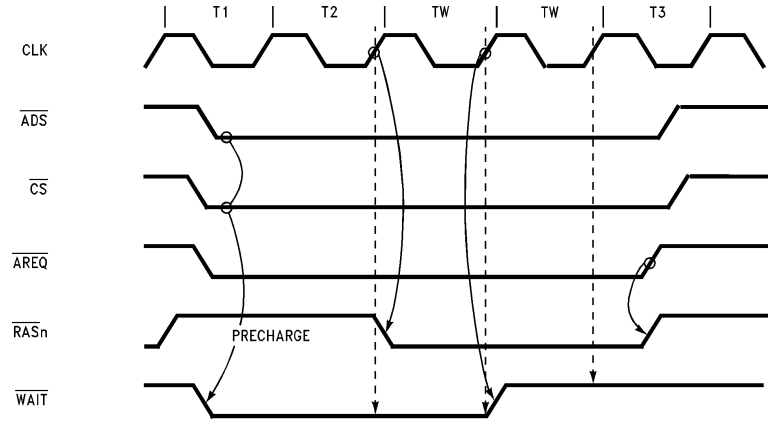


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**FIGURE 4d. Mode 1 Delayed Access with $\overline{WAIT}$ 1T ($\overline{WAIT}$ is Sampled at the End of the "T2" Clock State)**

When ending $\overline{WAIT}$ from a negative level of CLK, if $\overline{RAS}$ is asserted while CLK is high then $\overline{WAIT}$ will negate from the negative edge of CLK. If $\overline{RAS}$ is asserted while CLK is low then $\overline{WAIT}$ will negate from $\overline{RAS}$ asserting.

When ending $\overline{WAIT}$ from a positive edge of clock in Mode 0, the user can think of the positive edge of CLK that starts $\overline{RAS}$ as 0T and the next positive edge of CLK as 1T.

When ending $\overline{WAIT}$ from a positive edge of clock in Mode 1, the positive edge of CLK that $\overline{ADS}$ is setup to, can be thought of as 1T in a non-delayed access. In a delayed access, the positive edge of CLK that starts $\overline{RAS}$ can be thought of as 0T and the next positive edge as 1T.

**Wait During Page Burst Accesses**

$\overline{WAIT}$ can be programmed to function differently during page/burst type accesses. During a page/burst access, the $\overline{ECAS}$ inputs will be asserted then negated while $\overline{AREQ}$ is asserted. Through address bits R4 and R5, $\overline{WAIT}$ can be programmed to assert and negate during these type of accesses. The user is given four programming options described below.

No Wait States (R5 = 0, R4 = 0): In this case, $\overline{WAIT}$ will remain negated even if the $\overline{ECAS}$ inputs are toggled as shown in *Figure 5*.

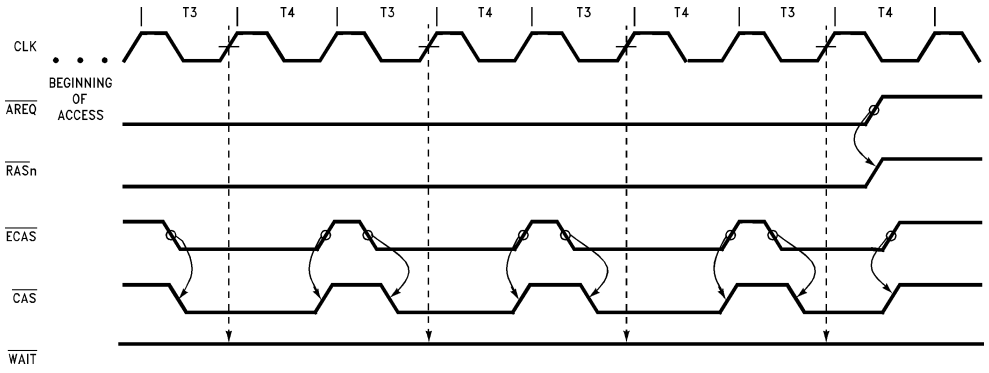


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**FIGURE 5. No Wait States during Burst ($\overline{WAIT}$ is Sampled at the End of the "T3" Clock State)**

0T (R5 = 0, R4 = 1): $\overline{WAIT}$ will be asserted when the $\overline{ECAS}$ inputs are negated with $\overline{AREQ}$ remaining asserted. When a single or group of $\overline{ECAS}$ inputs are asserted, $\overline{WAIT}$ will be negated as shown in *Figure 6*.

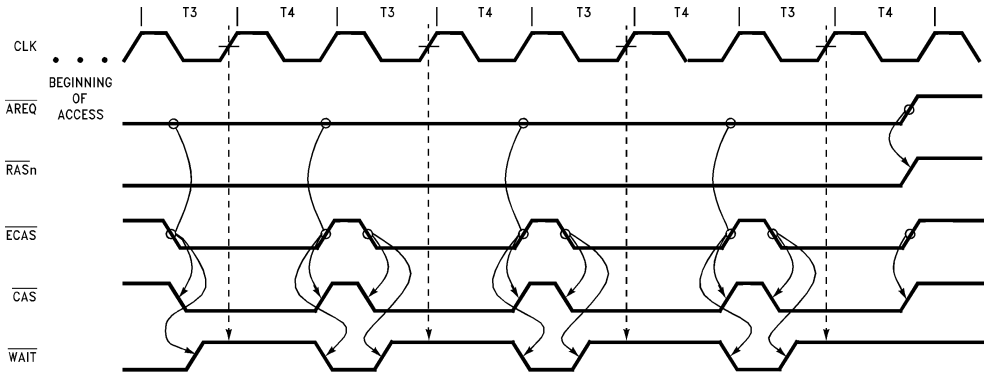


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**FIGURE 6. 0T during Burst ($\overline{WAIT}$ is Sampled at the End of the "T3" Clock State)**

½T (R5 = 1, R4 = 0): $\overline{\text{WAIT}}$ will be asserted when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ remaining asserted. When a single or group of $\overline{\text{ECAS}}$ inputs are asserted again, $\overline{\text{WAIT}}$ will be negated from the first negative level of CLK after a single $\overline{\text{ECAS}}$ or group of $\overline{\text{ECAS}}$s are asserted as shown in *Figure 7*.

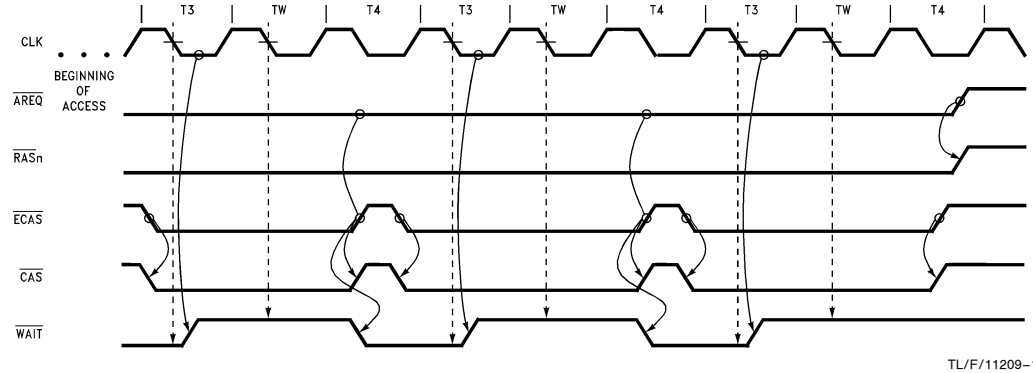


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**FIGURE 7. ½T during Burst Access ($\overline{\text{WAIT}}$ is Sampled at the "T3" Falling Clock Edge)**

1T (R5 = 1, R4 = 1): $\overline{\text{WAIT}}$ will be asserted when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ remaining asserted. When a single or group of $\overline{\text{ECAS}}$ are asserted again, $\overline{\text{WAIT}}$ will be negated from the first positive edge of CLK after a single $\overline{\text{ECAS}}$ or group of $\overline{\text{ECAS}}$s are asserted as shown in *Figure 8*.

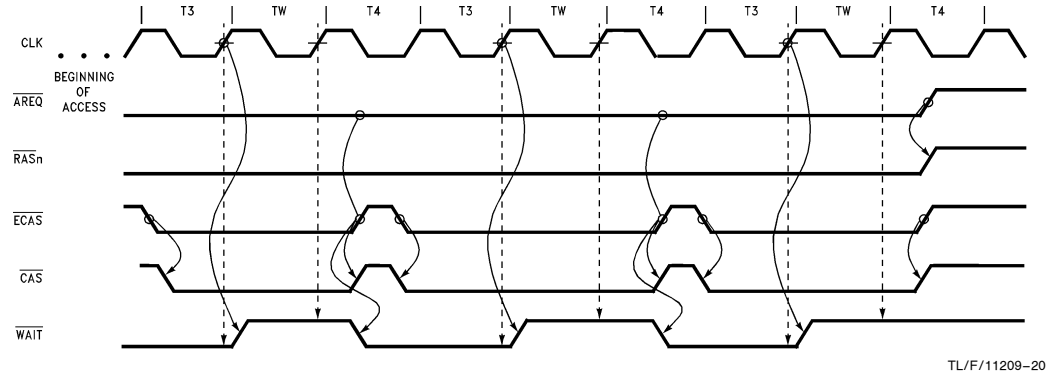


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**FIGURE 8. 1T during Burst Access ($\overline{\text{WAIT}}$ is Sampled at the End of the "T3" Clock State)**

When ending $\overline{\text{WAIT}}$ from a negative level of CLK: If the $\overline{\text{ECAS}}$ are asserted while CLK is high, then $\overline{\text{WAIT}}$ will negate from the negative edge of CLK. If the $\overline{\text{ECAS}}$ are asserted while CLK is low, then $\overline{\text{WAIT}}$ will negate from the $\overline{\text{ECAS}}$s asserting.

When ending $\overline{\text{WAIT}}$ from a positive edge of CLK, the positive edge of CLK that $\overline{\text{ECAS}}$ is set up to, can be thought of as 1T.

**$\overline{\text{DTACK}}$ During Single Accesses**

$\overline{\text{DTACK}}$ can be programmed to delay a number of positive edges and/or negative levels of CLK. These options are programmed through address bits R2 and R3 at programming time. The user is given four options described by the following.

| R3 R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|
| | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 0 0 | 0T | 0T | 0T | 0T |

0T During Non-Delayed and Delayed Accesses. In Mode 0, $\overline{\text{DTACK}}$ will assert from the positive edge of CLK that starts $\overline{\text{RAS}}$ as shown in *Figure 9a*.

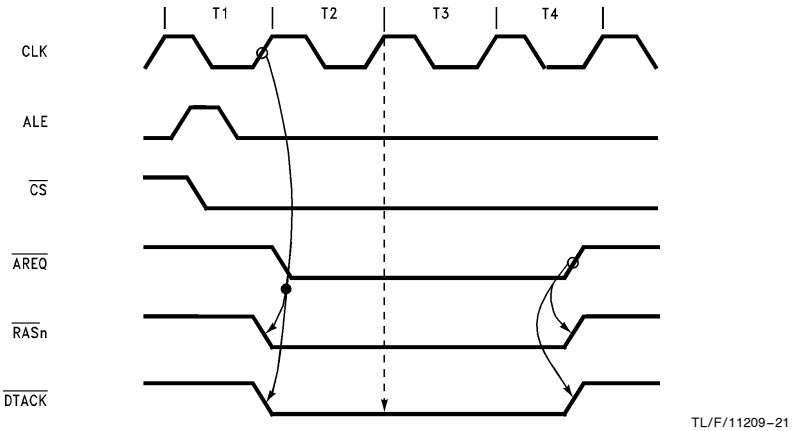


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**FIGURE 9a. Mode 0 Non-Delayed Access with $\overline{\text{DTACK}}$ 0T ($\overline{\text{DTACK}}$ is Sampled at the End of the "T2" Clock State)**

In Mode 1, $\overline{\text{DTACK}}$ will assert from $\overline{\text{ADS}}$ and $\overline{\text{CS}}$ as shown in *Figure 9b*.

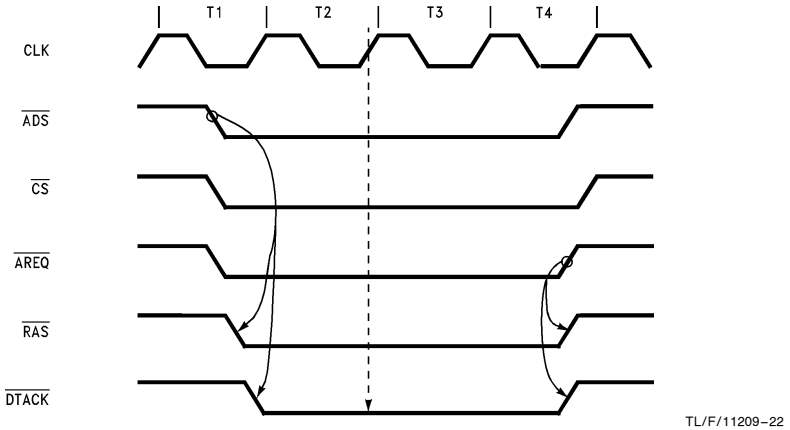


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**FIGURE 9b. Mode 1 Non-Delayed Access with $\overline{\text{DTACK}}$ 0T ($\overline{\text{DTACK}}$ is Sampled at the End of the "T2" Clock State)**

During delayed accesses in both modes, $\overline{\text{DTACK}}$ will assert from the positive edge of CLK which starts $\overline{\text{RAS}}$ for that access as shown in *Figures 9c* and *9d*.

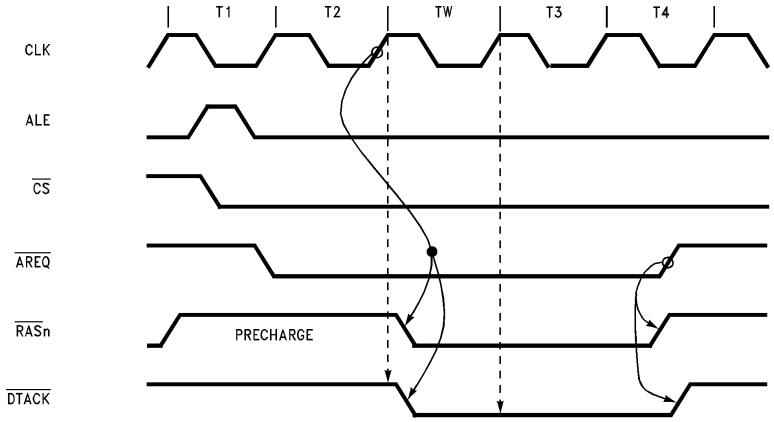


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**FIGURE 9c. Mode 0 Delayed Access with $\overline{\text{DTACK}}$ 0T (2T Clock Periods are Programmed for $\overline{\text{RAS}}$ Precharge, $\overline{\text{DTACK}}$ is Sampled at the End of the "T2" Clock State)**

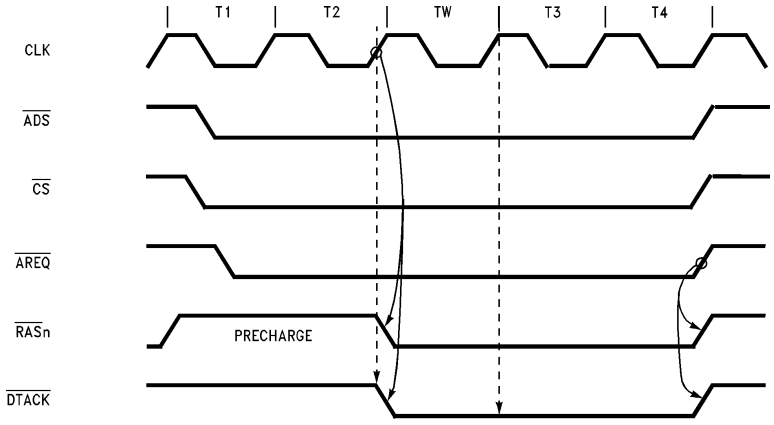


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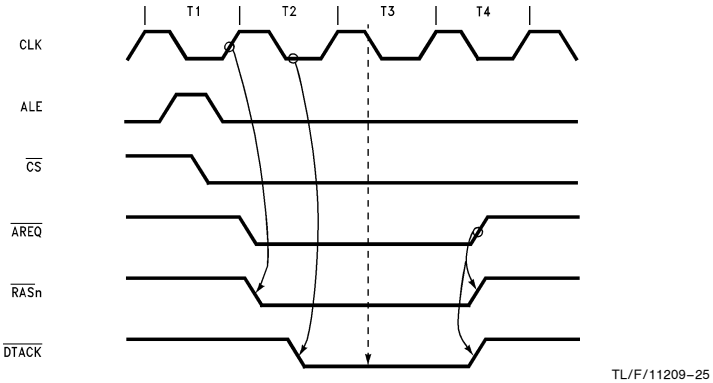
**FIGURE 9d. Mode 1 Delayed Access with $\overline{\text{DTACK}}$ 0T ($\overline{\text{DTACK}}$ is Sampled at the End of the "T2" Clock State)**

| R3 | R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|---|
| | | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 0 | 1 | ½T | ½T | ½T | ½T |

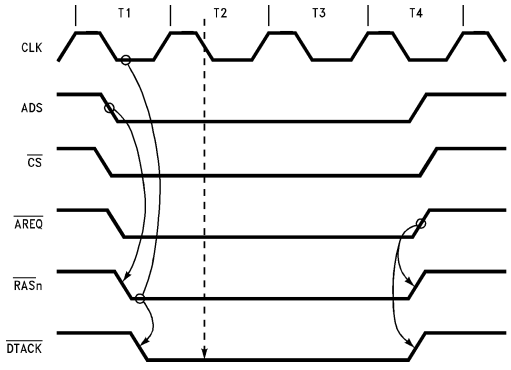
½T During Non-Delayed and Delayed Accesses. In Mode 0, $\overline{\text{DTACK}}$ will asert on the negative level of CLK after the positive edge of CLK that starts $\overline{\text{RAS}}$ as shown in *Figure 10a*.




TL/F/11209–25

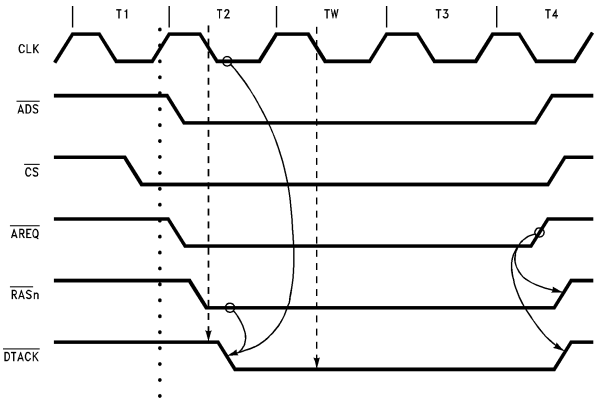
**FIGURE 10a. Mode 0 Non-Delayed Access with $\overline{\text{DTACK}}$ of ½T ($\overline{\text{DTACK}}$ is Sampled at the "T3" Falling Clock Edge)**

In Mode 1, $\overline{\text{DTACK}}$ will assert from the negative level of clock after $\overline{\text{ADS}}$ has been asserted, given that $\overline{\text{RAS}}$ is asserted as shown in *Figures 10b* and *10c*.




TL/F/11209–26

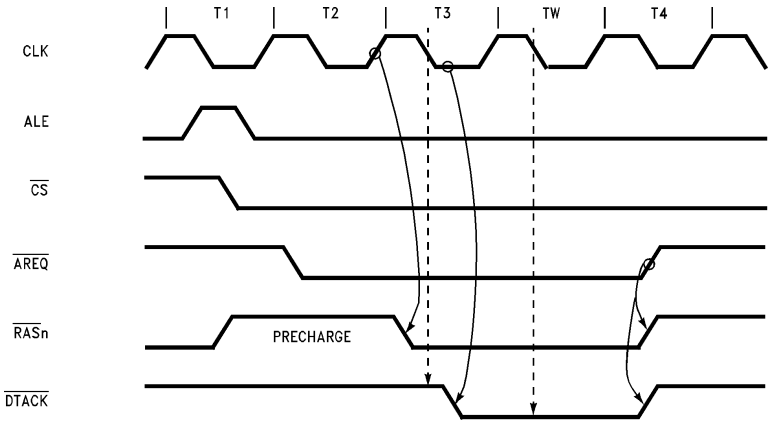
**FIGURE 10b. Mode 1 Non-Delayed Access with $\overline{\text{DTACK}}$ of ½T ($\overline{\text{DTACK}}$ is Sampled at the "T2" Falling Clock Edge)**




TL/F/11209–27

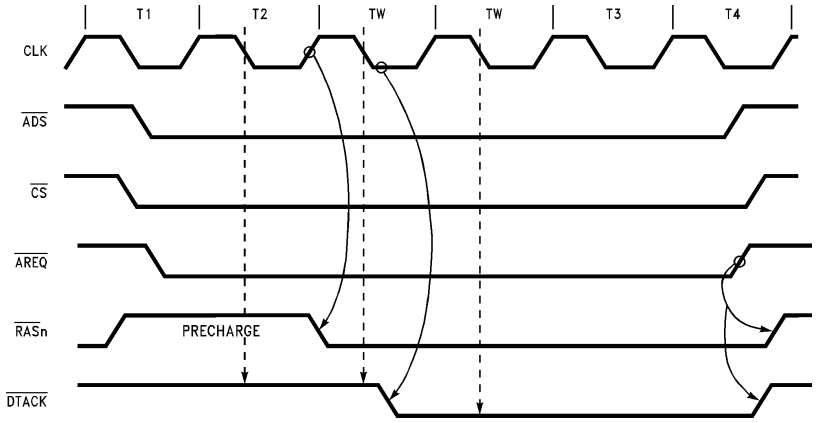
**FIGURE 10c. Mode 1 Non-Delayed Access with $\overline{\text{DTACK}}$ of ½T ($\overline{\text{DTACK}}$ is Sampled at the "T2" Falling Clock Edge)**

During delayed accesses in both modes, $\overline{\text{DTACK}}$ will assert from the negative level of CLK after the positive edge of CLK that started $\overline{\text{RAS}}$ for that access as shown in *Figures 10d* and *10e*.




TL/F/11209–28

**FIGURE 10d. Mode 0 Delayed Access with $\overline{\text{DTACK}}$ of ½T ($\overline{\text{DTACK}}$ is Sampled at the "T3" Falling Clock Edge)**

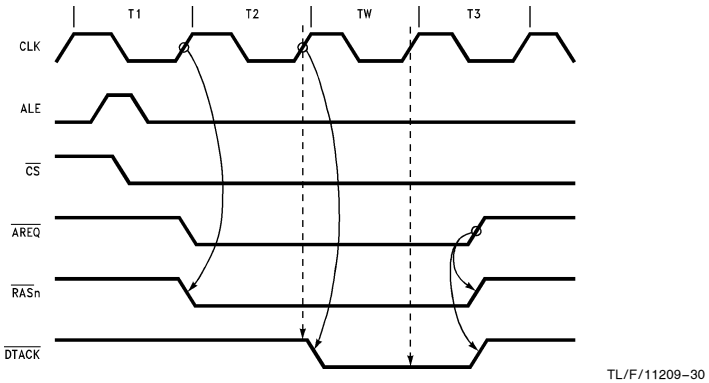



TL/F/11209–29

**FIGURE 10e. Mode 1 Delayed Access with $\overline{\text{DTACK}}$ of ½T ($\overline{\text{DTACK}}$ is Sampled at the "T2" Falling Clock Edge)**

| R3 | R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|---|
| | | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 1 | 0 | 1T | 1T | 1T | 1T |

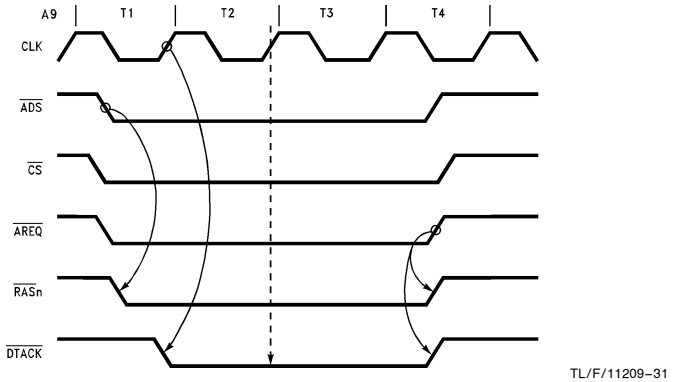
1T During Delayed and Non-Delayed Accesses. In Mode 0, $\overline{DTACK}$ will assert from the first positive edge of CLK after the positive edge of CLK which starts $\overline{RAS}$ for that access as shown in *Figure 11a*.




TL/F/11209–30

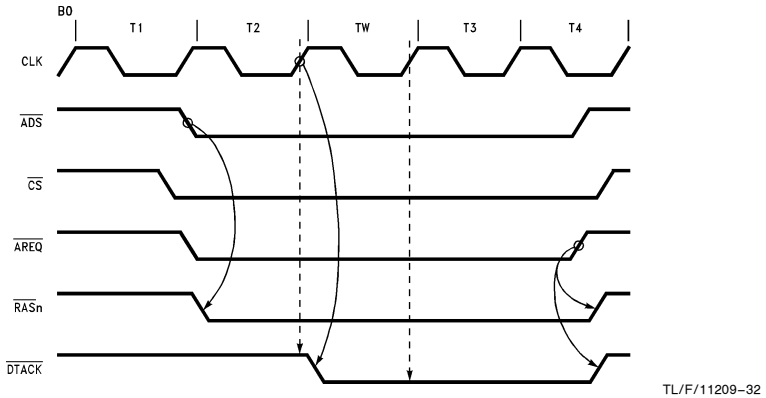
**FIGURE 11a. Mode 0 Non-Delayed Access with $\overline{DTACK}$ of 1T ($\overline{DTACK}$ is Sampled at the End of the "T2" Clock State)**

In Mode 1, $\overline{DTACK}$ will assert from the positive edge of CLK after $\overline{ADS}$ and $\overline{CS}$ are asserted as shown in *Figures 11b* and *11c*.




TL/F/11209–31

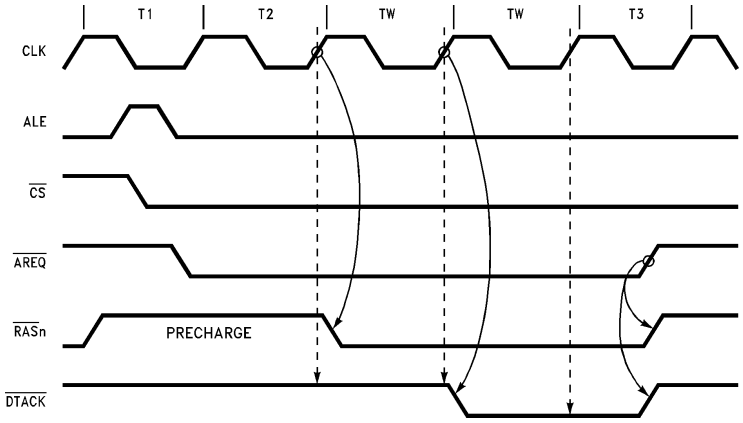
**FIGURE 11b. Mode 1 Non-Delayed Access with $\overline{DTACK}$ of 1T ($\overline{DTACK}$ is Sampled at the End of the "T2" Clock State)**




TL/F/11209–32

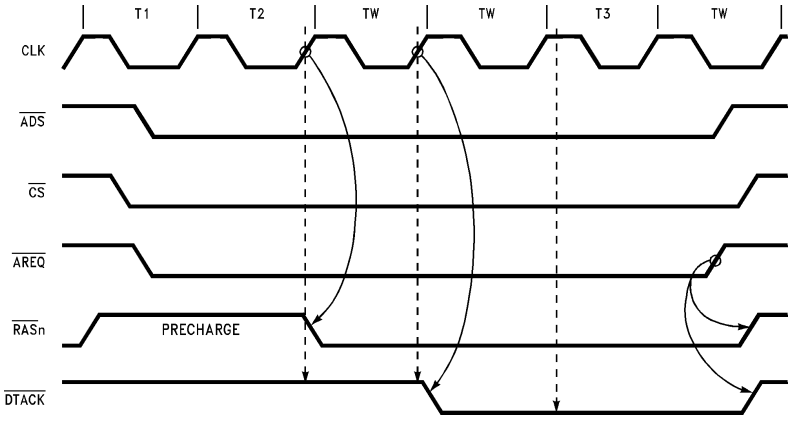
**FIGURE 11c. Mode 1 Late Non-Delayed Access with $\overline{DTACK}$ of 1T ($\overline{DTACK}$ is Sampled at the End of the "T2" Clock State)**

During delayed accesses in both modes, $\overline{\text{DTACK}}$ will assert from the first positive edge of CLK after the positive edge of CLK that started $\overline{\text{RAS}}$ for that access as shown in *Figures 11d* and *11e*.




TL/F/11209–33

**FIGURE 11d. Mode 0 Delayed Access with $\overline{\text{DTACK}}$ of 1T ($\overline{\text{DTACK}}$ is Sampled at the End of the "T2" Clock State)**

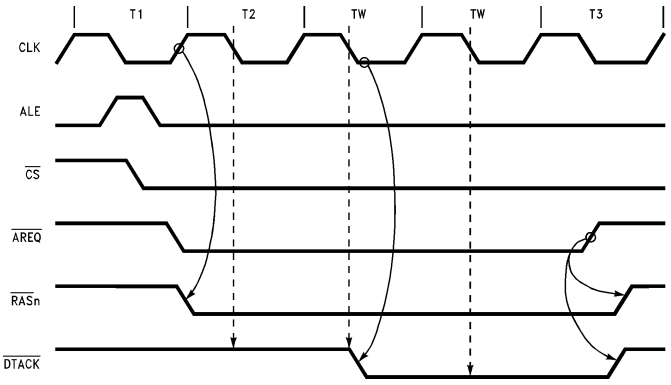



TL/F/11209–34

**FIGURE 11e. Mode 1 Delayed Access with $\overline{\text{DTACK}}$ of 1T ($\overline{\text{DTACK}}$ is Sampled at the End of the "T2" Clock State)**

| R3 | R2 | Mode 0 | | Mode 1 | |
|---|---|---|---|---|---|
| | | Non-Delayed | Delayed | Non-Delayed | Delayed |
| 1 | 1 | 1½T | 1½T | 1½T | 1½T |

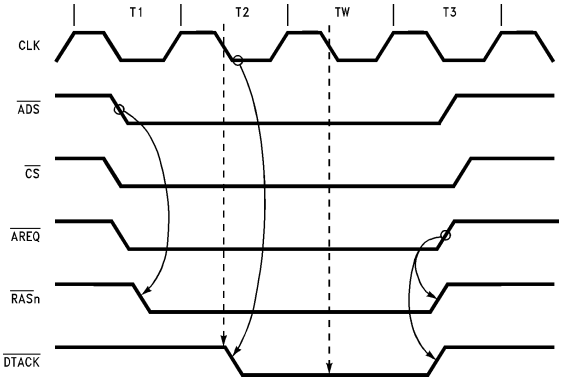
1½T During Delayed and Non-Delayed Accesses. In Mode 0, $\overline{DTACK}$ will assert from the negative level after the first positive edge of CLK after the positive edge of CLK that started $\overline{RAS}$ for that access as shown in *Figure 12a*.




TL/F/11209–35

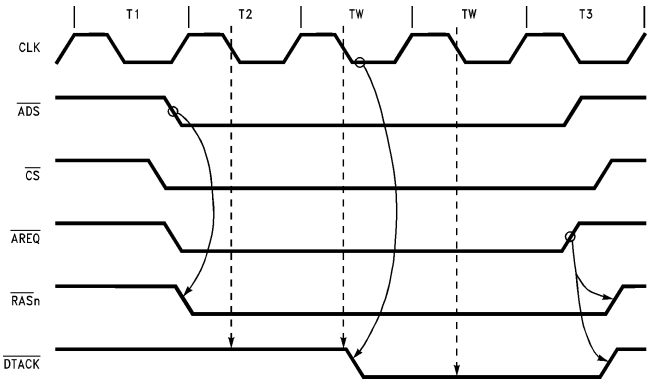
**FIGURE 12a. Mode 0 Non-Delayed Access with $\overline{DTACK}$ of 1½T ($\overline{DTACK}$ is Sampled at the "T2" Falling Clock Edge)**

In Mode 1, $\overline{DTACK}$ will assert from the negative level after the first positive edge of CLK after $\overline{ADS}$ and $\overline{CS}$ are asserted as shown in *Figures 12b* and *12c*.




TL/F/11209–36

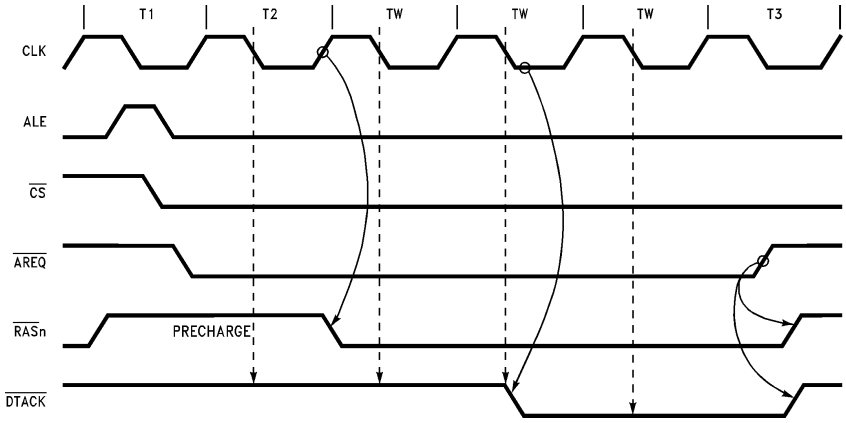
**FIGURE 12b. Mode 1 Non-Delayed Access with $\overline{DTACK}$ of 1½T ($\overline{DTACK}$ is a Sampled at the "T2" Falling Clock Edge)**




TL/F/11209–37

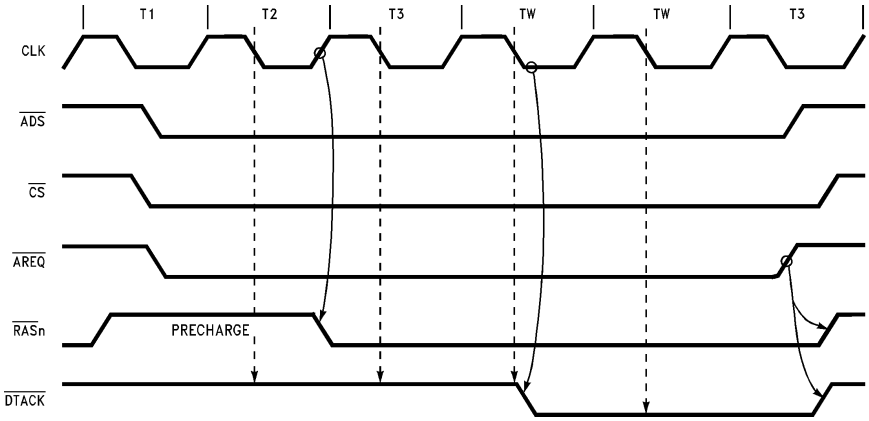
**FIGURE 12c. Mode 1 Non-Delayed Access with $\overline{DTACK}$ of 1½T ($\overline{DTACK}$ is Sampled at the "T2" Falling Clock Edge)**

During delayed accesses in both modes, $\overline{DTACK}$ will assert from the negative level after the first positive edge of CLK after the positive edge of CLK that starts $\overline{RAS}$ for that access as shown in *Figures 12d* and *12e*.




TL/F/11209–38

**FIGURE 12d. Mode 0 Delayed Access with $\overline{DTACK}$ of 1½T ($\overline{DTACK}$ is Sampled at the "T2" Falling Clock Edge)**




TL/F/11209–39

**FIGURE 12e. Mode 1 Delayed Access with $\overline{DTACK}$ of 1½T ($\overline{DTACK}$ is Sampled at the "T2" Falling Clock Edge)**

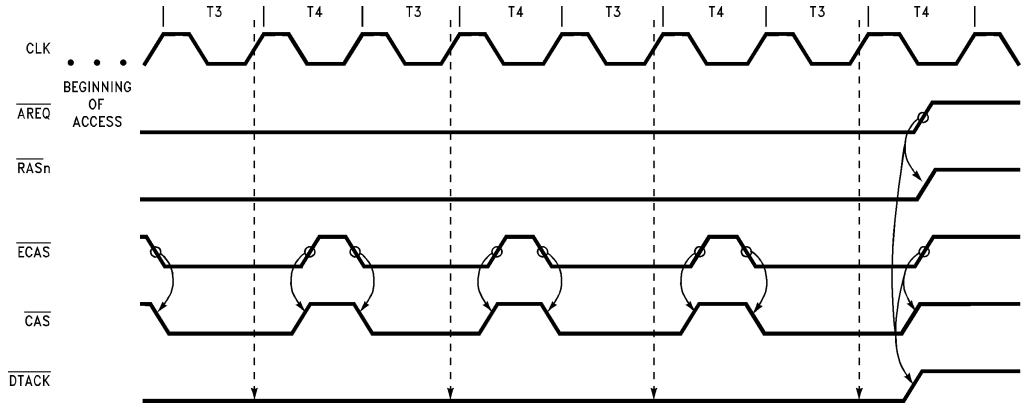
When starting $\overline{DTACK}$ from a negative level of CLK: If $\overline{RAS}$ is asserted while CLK is high, then $\overline{DTACK}$ will assert from the negative edge of CLK. If $\overline{RAS}$ is asserted while CLK is low, then $\overline{DTACK}$ will assert from $\overline{RAS}$ asserting. When starting $\overline{DTACK}$ from a positive edge of CLK: In Mode 0, the positive edge of CLK that starts $\overline{RAS}$ can be thought of as 0T.

In Mode 1, during non-delayed accesses, the positive edge of CLK that $\overline{ADS}$ is set up to, can be thought of as 1T. During delayed accesses, the positive edge of CLK that starts $\overline{RAS}$ can be thought of as 0T and the next positive edge of CLK as 1T.

**$\overline{\text{DTACK}}$ During Page/Burst Accesses**

$\overline{\text{DTACK}}$ can be programmed to function directly page/burst types of accesses. During a page/burst access, the $\overline{\text{ECAS}}$ inputs will be asserted then negated while $\overline{\text{AREQ}}$ remains asserted. Through address bits R4 and R5, $\overline{\text{DTACK}}$ can be programmed to negate and assert during this type of access. The user is given four programming options described below.

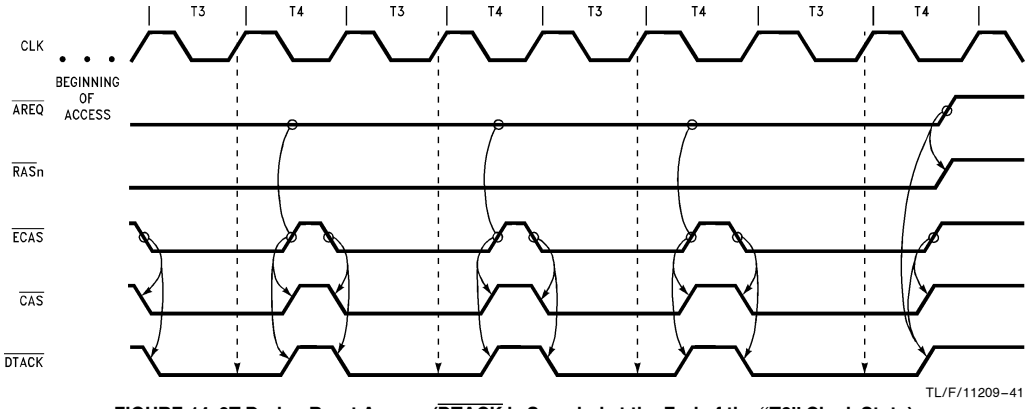
No Wait States (R5 = 0, R4 = 0): In this case, $\overline{\text{DTACK}}$ will remain asserted even if the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted as shown in *Figure 13*.




TL/F/11209–40

**FIGURE 13. No Wait States during Burst Access ($\overline{\text{DTACK}}$ is Sampled at the End of the "T3" Clock State)**

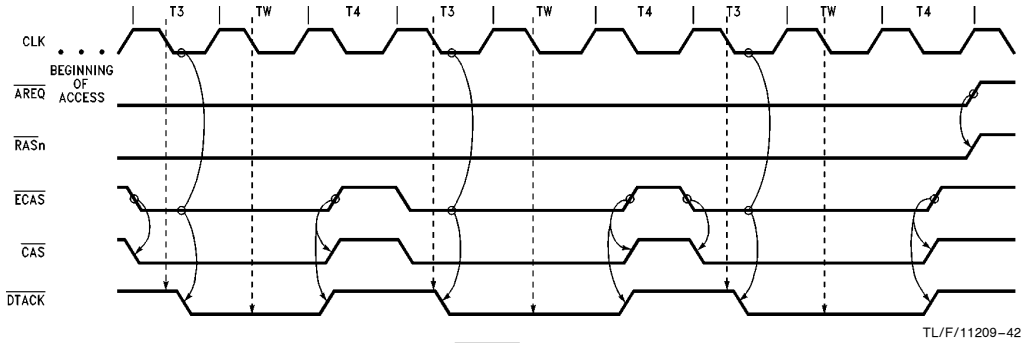
0T (R5 = 0, R4 = 1): $\overline{\text{DTACK}}$ will be negated when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. When a single or group of $\overline{\text{ECAS}}$ inputs are asserted again, $\overline{\text{DTACK}}$ will be asserted as shown in *Figure 14*.




TL/F/11209–41

**FIGURE 14. 0T During Burst Access ($\overline{\text{DTACK}}$ is Sampled at the End of the "T3" Clock State)**

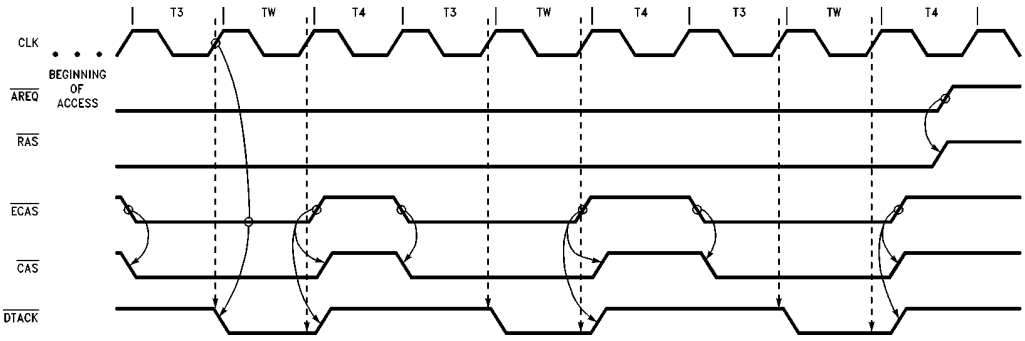
½T (R5 = 1, R4 = 0): $\overline{\text{DTACK}}$ will be negated when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. When a single or group of $\overline{\text{ECAS}}$ inputs are asserted again, $\overline{\text{DTACK}}$ will be asserted from the first negative level of CLK after the single or group of $\overline{\text{ECAS}}$ are asserted as shown in *Figure 15*.




TL/F/11209–42

**FIGURE 15. ½T during Burst Access ($\overline{\text{DTACK}}$ is Sampled at the "T3" Falling Clock Edge)**

1T (R5 = 1, R4 = 1): $\overline{\text{DTACK}}$ will be negated when the $\overline{\text{ECAS}}$ inputs are negated with $\overline{\text{AREQ}}$ asserted. When a single or group of $\overline{\text{ECAS}}$ are asserted again, $\overline{\text{DTACK}}$ will be asserted from the first positive edge of CLK after the single or group of $\overline{\text{ECAS}}$ are asserted as shown in *Figure 16*.




TL/F/11209–43

**FIGURE 16. 1T During Burst Access ($\overline{\text{DTACK}}$ is Sampled at the "T3" Falling Clock Edge)**

When starting $\overline{\text{DTACK}}$ from a negative level of CLK: If the $\overline{\text{ECAS}}$ are asserted while CLK is high, then $\overline{\text{DTACK}}$ will assert from the negative edge of CLK. If the $\overline{\text{ECAS}}$ are asserted while CLK is low, then $\overline{\text{DTACK}}$ will assert from the $\overline{\text{ECAS}}$ asserting.

When starting $\overline{\text{DTACK}}$ from a positive edge of CLK, the positive edge of CLK that $\overline{\text{ECAS}}$ is set up to, can be thought of as 1T.

**CONCLUSION**

By inserting wait states the normal CPU access cycle is increased and all signals associated with the access are extended. A CPU access cycle can be increased by one or by multiple CPU clock periods so that the memory cycle can be successfully terminated. Extending the access cycle allows slower memories to have the necessary extra time to respond in a reliable way to the CPU. The insertion of wait states will ensure that data from the DRAM will be present when the CPU reads or that data has been written into the DRAM before the CPU terminates cycle.

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