DP83950EB-AT IEEE 802.3 Multi-Port Repeater Evaluation Kit

National Semiconductor
Application Note 781
Imad Ayoub
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1.0 INTRODUCTION

The DP83950EB-AT is a three board kit (Main board, Display Assembly board and Backplane board) that forms an IEEE 802.3 Section 9 Repeater. The Main board has twelve 10Base-T ports and one AUI port and up to four Main boards can be cascaded using the Backplane board to form a larger hub.

The Main board contains the DP83950 Repeater Interface Controller (RIC™), which fits into an IBM PC-AT and compatible computers. The Main board repeats packets, provides management information, updates the Status LEDs, and can be cascaded to other Main boards. The Display Assembly board provides a full set of status LEDs for monitoring the repeater activity, and it provides a breakout to convert the 50-pin connector (with the cable coming from the Main board) to twelve ISO8877 (RJ45) phone connectors. The Backplane board is used for cascading two or more Main boards or to connect to a modified DP839EB-ATS System Oriented Network Interface Controller (SONIC™) Network evaluation board or the new SONIC Network evaluation board, the DP83932EB-AT.

Using the evaluation software the user can read or write to the RIC registers and counters, change the configuration options, enable and disable several features of the RIC, and display graphics of the RIC activities. There are several switches and jumpers on the Main board that configure the board to avoid conflicts with other adapters already installed on the AT bus.

2.0 MAIN BOARD OVERVIEW

The block diagram for the Main board is shown in *Figure 1.* The Main board allows the user to exercise all the functions of the RIC while using the twelve 10Base-T ports and the AUI port (the 10Base2 option of the RIC cannot be exercised).

The Main board is designed to perform Mload (refer to the RIC Data Sheet for more information on Mload) through either the Mload Logic (hardware Mload), or through the AT Bus Interface (software Mload). The switches SW1, SW2 are used during the hardware Mload.

The Inter-RIC Arbitration Logic performs the arbitration when there are two or more boards cascaded using the Backplane board. The arbitration is performed when two or more RICs have reception to determine which Main board (i.e., which RIC) is higher in the arbitration chain. The result of the arbitration will be used by the main state diagram of the RIC to determine which port within the RIC has PORT N (or PORT M), as described in the RIC Data Sheet.

The board was designed to allow for choosing between serial and parallel arbitration, and performs the arbitration function accordingly. In the Serial arbitration mode, the RIC logic performs all the arbitration (no additional logic is needed). In the parallel arbitration mode external PALs and logic are required (see Section 2.1.2).

The Inter-RIC BUS Transceivers are used to interface the RIC to the Backplane BUS. The Backplane BUS includes the Inter-RIC signals (IRC, IRD, IRE), the Management signals (MRXC, MRXD, MCRS, PCOMP), the Arbitration and Control signals (ACKI, ACKO, ACTN, ANYXN, COLN) as well as the parallel arbitration vector ARB(3:0). The transceivers are an example of how to perform the transmitting and receiving function over a backplane Bus and interfacing to drive and sense pins on the RIC. The BTL transceivers used allow for long bus applications due to their fast propagation delays and separate bus grounds.

The External Decoder is an example of how the RIC can be configured to run with an external decoder. The Received Manchester data is passed on to the external decoder through the RXM pin, and the decoded NRZ data is sent back from the decoder to the RIC through the Inter-RIC pins IRE, IRC and IRD.

The LED information is sent to the Display board through a driver and a 25-pin ribbon cable.

The 10Base-T Interface includes the buffers, resistors, filters and transformers necessary to interface the RIC ports to the external TP media.

The AUI Interface includes the necessary isolation and resistors to interface to the AUI cable.

In order to enable using up to 16 boards in a PC without using an excessively large address space, all boards can be mapped to a single address block. A separate register is used to enable each individual board. This register is called the Global Register. The Global Register contains other control bits as shown below:

D6	D5	D4	D3	D2	D1	D0
EA2	EA1	EA0	RID3	RID2	RID1	RID0

Each board in a system is assigned a unique number by setting SW3. When the same number is loaded into the Global Register RID(3:0) as is set by SW3, the RIC Main board is enabled and the RIC's registers can be accessed.

The EA(2:0) bits are used to perform various functions on the selected board in the following manner:

EA2	EA1	EA0	Function
0	0	0	Normal Operation
0	0	1	Issue CDEC to All Boards
0	1	0	Issue CDEC to Selected Board
0	1	1	Issue MLOAD to All Boards
1	0	0	Issue MLOAD to Selected Board

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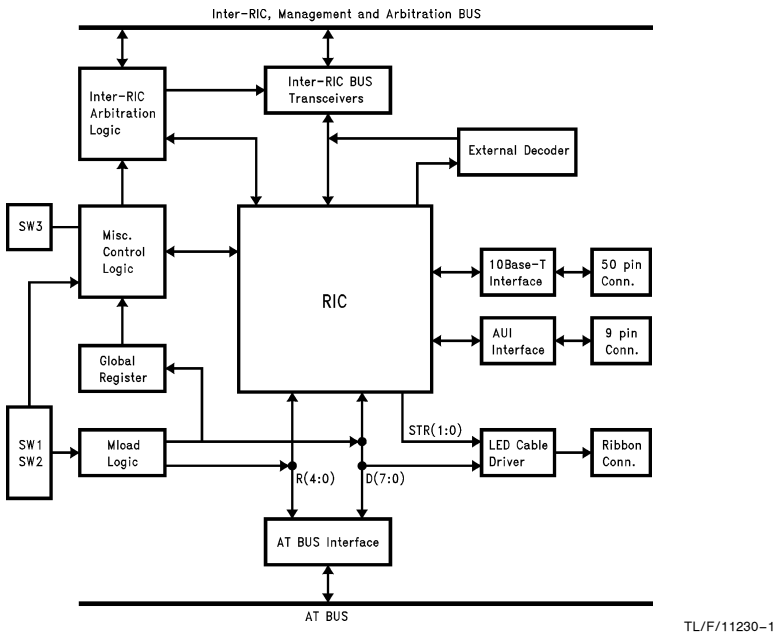

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FIGURE 1. Main Board Block Diagram

All 32 RIC registers and the Global register are IO mapped and can be relocated by setting BA(1:0) in SW1 as follows:

BA1	BA0	RIC Registers	Global Register
0	0	100 h–11F h	200 h
0	1	120 h–13F h	220 h
1	0	140 h–15F h	240 h
1	1	160 h–17F h	260 h

2.1 Detailed Description

2.1.1 Mload and AT Bus Interface

To perform the Mload pin configuration the board has the capability to load the D(7:0) and R(4:0) pins by either software or hardware.

Hardware Mload is done by the Mload Logic, which interfaces to pins D(7:0) and R(4:0) on the RIC to configure the RIC upon power up. Switches SW1 and SW2 allow for hardware setting of the Mload pin configuration. An RC network is used to provide a pulse (RSTB) at power up which will be used by a PAL (U41) to assert the Mload signal to the RIC. The PAL is needed to control the enables for the buffers for choosing between the hardware and software Mload.

Software Mload is implemented by passing the D(7:0) and R(4:0) signals from the PC-AT bus through the AT Bus Interface and onto the RIC pins.

When a Global Register write operation is performed by the PC-AT, it is written to a flip-flop (U44) which passes, first, the bits RID(3:0) to a comparator (U38), second, the bits EA(3:0) to the one of the control PALs. The comparator asserts a ''RICHIT'' if the Global Register RID matches the board *number*. This will enable the control PALs to perform the operation required by the Global register.

The ELI and RTI pins from the RIC can be passed onto the AT BUS to one of four interrupt request lines on the AT BUS (IRQ(15), IRQ(12), IRQ(11) or IRQ(10)) by selecting the appropriate jumper settings (JB1 and JB2, refer to schematic).

Three PALs (U36, U41, U43) are used to control the AT Bus Interface for software Mload and register Read/Write, and to enable the various buffers required for hardware Mload and the Global register decode. The PAL equations listings for all the PALs are included in Section 5.0 of this document.

U43 decodes the AT BUS address bits SA(9:0) and BA(1:0) to determine if the software operation is addressed to this board. A Global hit (Ghit) is asserted when a match occurs with the Main board's global *address*. A Base hit (Bhit) is asserted when a match occurs with a RIC *register.*

The AT BUS signals IOW, IOR, and AEN, and the Global register bits EA(2:0) are decoded by the PALs U36 and U41, resulting in the various control signals for the Mload buffers, the Read, Write and CDEC signals, the CHRDY signal to the PC-AT BUS, and the *receive* enable signals for the Inter-RIC and the management BTL transceivers (U4, U5).

2.1.2 Inter-RIC Arbitration Logic

Since there is no central arbiter, each Main board using the Inter-RIC BUS needs a way to tell if it owns the bus. This implementation uses one of two methods: serial or parallel arbitration (by setting JB3, refer to schematic).

In the serial arbitration method the RIC signals ACKI and ACKO are passed to and from the Backplane BUS directly (as SACKI and SACKO) without further arbitration. Therefore the serial arbitration is done by the RIC logic itself. A high level on ACKI tells the RIC that it can take the bus.

Therefore, the physical position of the board controls its priority in the chain. To participate properly in the chain the RIC will pass a high ACKI to ACKO if it does not want to transmit, but will force ACKO low if it does wish to transmit. In addition, ACKO needs to be held low if a low ACKI is seen, in order to tell the boards further down in the chain that they cannot take the bus.

The drawback for serial arbitration is that it requires all the Main boards to be inserted at all times, otherwise the SACKI/SACKO chain will be broken. The Backplane board is equipped with a jumper to connect these signals to continue the arbitration chain.

In the Parallel arbitration mode the SACKI/SACKO signals are controlled by two PALs according to the ACKI, ARBWIN and ENARB state machines shown in *Figures 2, 3* and *4.* A priority number is assigned via a set of dip switches SEL(3:0), where a higher number corresponds to a higher priority. Each board that wants to use the bus asserts this vector onto the bus. The bus is ''wired-OR'', so that only the board with the highest priority will see its own vector reflected back from the bus.

By monitoring the RIC signals and the arbitration vector, the parallel logic controls ACKI, so that normal functionality is maintained and the board's priority is independent of its physical location.

The arbitration takes place whenever a RIC is trying to take the bus, i.e., ACTNd is asserted, or when the RIC is experiencing a transmit collision, i.e., ANYXNd is asserted *(Figure 2).* When either the ACTNd or ANYXNd are asserted the ENARB signal *(Figure 4)* is asserted enabling the arbitration BTL transceiver (U2).

A counter state machine is used in another PAL (U33) to give some delay for the arbitration to be completed, and asserts the arbitration done signal ARBDONE *(Figure 3).* Based on the ACKI state machine the ACKIRIC signal is asserted to the RIC.

ACKI STATE MACHINE

Inputs: ACTND~, ANYXND~, ARBDONE, ARBWIN

Output: ACKI

~ = Active Logic Low

! = Inactive

eg: !ACTNB~ = Inactive or Logic High

!ARBWIN = Inactive or Logic Low

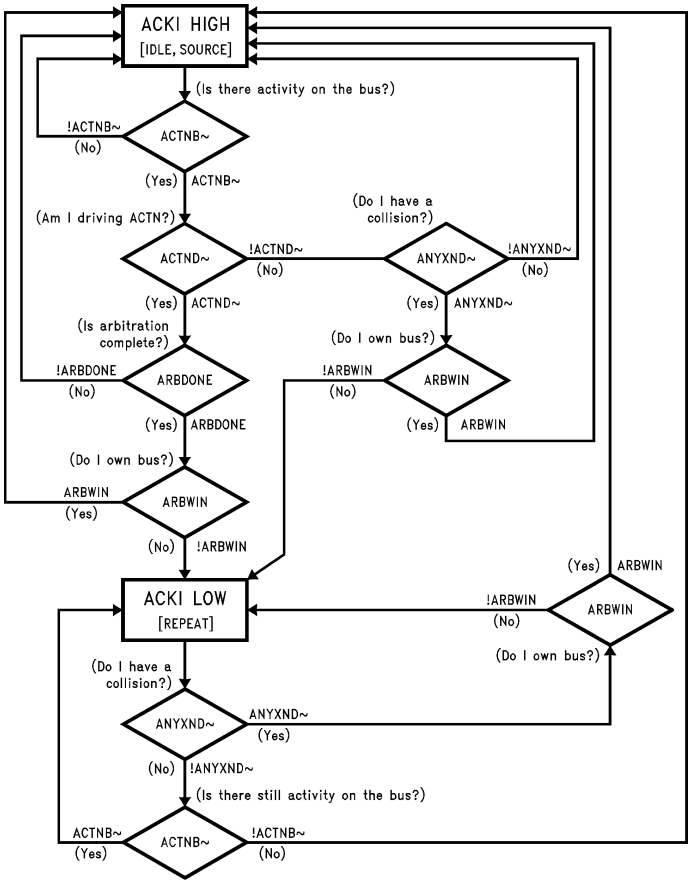

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FIGURE 2. ACKI State Machine

ARBWIN STATE MACHINE

Inputs: ANYXND~, ENARB, ARBDONE, BUSWIN~

Output: ARBWIN

~ = Active Logic Low

! = Inactive

eg: !ANYXND~ = Inactive or Logic High

ANYXND = Active or Logic Low

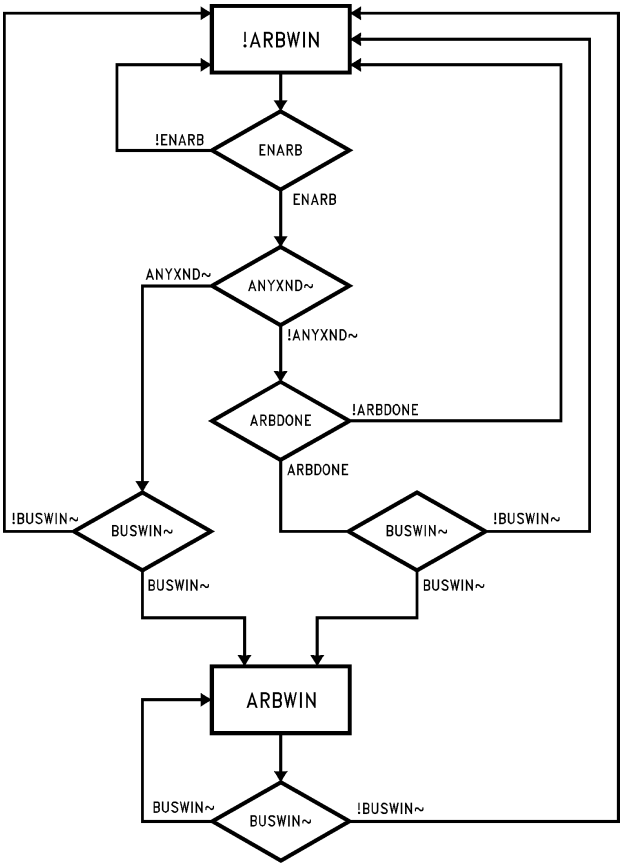

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FIGURE 3. ARBWIN State Machine

ENARB STATE MACHINE

Inputs: ACTND~, ANYXND~

Output: ENARB

ENARB = ACTND~ # ANYXND~

~ = Active Logic Low

! = Inactive

eg: !ACTND~ = Inactive or Logic High

ACTND~ = Active or Logic Low

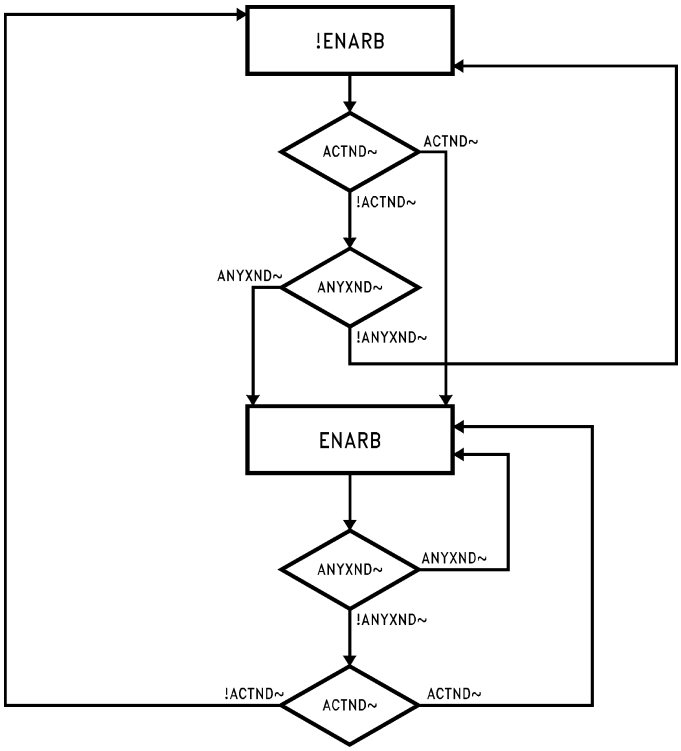

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FIGURE 4. ENARD State Machine

2.1.3 Inter-RIC Bus Transceivers

To form a 10Base-T HUB with more than 12 Twisted Pair ports, up to four Main boards can be cascaded using the Backplane board (up to 16 Main boards can be cascaded with an extended Backplane board). The Backplane board can also be used to pass management information, as specified in the Hub management specification, from the management bus of the RIC to a modified DP839EB-ATS SONIC network evaluation board or the new SONIC Network evaluation board, the DP83932EB-AT.

To assure good speed and signal quality over the backplane bus four BTL (Turbo Transceivers) are used (U2, U3, U4, U5). The required BTL terminations are done on the Backplane board. Tying all the Ground pins of the BTLs together is not the optimum way to use these transceivers, however, it was necessary to assure proper operation when the Main board is in stand alone mode and the backplane board is not inserted. In a typical application were the Backplane BUS is always terminated these grounds would not be grounded together.

High level of assertion for the bidirectional ''wired-OR'' signals (ACTN, ANYXN, COLN, IRE, MCRS) of the RIC is required for proper operation with the inverting BTL transceivers. This makes these signals asserted low on the BUS side of the transceivers.

The parallel arbitration vectors ARBI(3:0) and ARBO(3:0) are transmitted and received over the BUS through one BTL Transceiver (U2). The receive enable for U2 is controlled by the stand alone (SLN) bit set during Mload. The drive enable for U2 is controlled by the enable arbitration (ENARB) signal from the arbitration PALs.

Another PAL (U3) transmits and receives the ACTN, ANYXN, and PCOMP signals onto the Backplane BUS. On the BUS side of U3, ACTN and ANYXN are bidirectional signals. They are asserted when any RIC asserts its ACTNd or ANYXNd signals. On the RIC side of U3, ACTN is split into ACTNd and ACTNs, and ANYXN is split into ANYXNd and ANYXNs. PCOMP is a unidirectional signal that is asserted onto the BUS by a separate controller board that can gather management statistics (or a modified DP839EB-ATS SONIC-AT board). The Drive enable for U3 is always enabled, allowing the ACTNd and ANYXNd signals to assert the BUS ACTN and ANYXN signals directly. The Receive enable is disabled only when the Main board is in the stand alone mode (i.e., there are no other Main boards in the HUB).

The RC network included on the ANYXNs signal is recommended (see Application Note #671 in the Interface Data Book for design details using BTL Transceivers).

A third PAL (U4) is used to transmit and receive the IRC, IRD, IRE and COLN signals. The COLN signal, which signals a receive collision, has no significance in the TP media. It is included here for completeness. These signals are bidirectional, however they are unidirectional at any one time. When the RIC is the receiving RIC, it asserts the packet enable signal PKEN signal which is used as the drive enable for U4. PKEN will be asserted as long as the RIC is the receiving RIC. The receive enable ENPKEN is asserted when the Main board is not in stand alone mode, and the PKEN signal is not asserted.

A fourth PAL (U5) is used to transmit the management bus signals MRXC, MCRS and MRXD. The MRXC and MRXC signals are unidirectional RIC output signals, while the MCRS is a bidirectional. The RIC senses the MCRS signal while the RIC is not the receiving RIC to assure the Interframe gap limit set in the RIC Inter-Frame Gap Threshold Select Register is not violated before sending another packet onto the Management BUS. The Management BUS information can be received by a SONIC, connected to the management bus. When the RIC is the receiving RIC, it asserts the management enable signal MEN, which is used as the drive enable for U5. MEN will be asserted as long as the RIC is the receiving RIC. The receive enable ENMEN is asserted when the Main board is not in stand alone mode, and the MEN signal is not asserted.

2.1.4 External Decoder

The RXM External pin decoder allows using the RIC with an external decoder. The RXM pin outputs the received Manchester Data from the RIC. This data is sent to the DP83910A decoder, which is decoded and passed onto the IRD, IRC and IRE BUS signals through a buffer back to the RIC. The buffer is enabled by PKEN, and a jumper is used to disable the buffer when using the internal decoder mode.

2.1.5 TP Interface

The interface is shown for one port in *Figure 5* below:

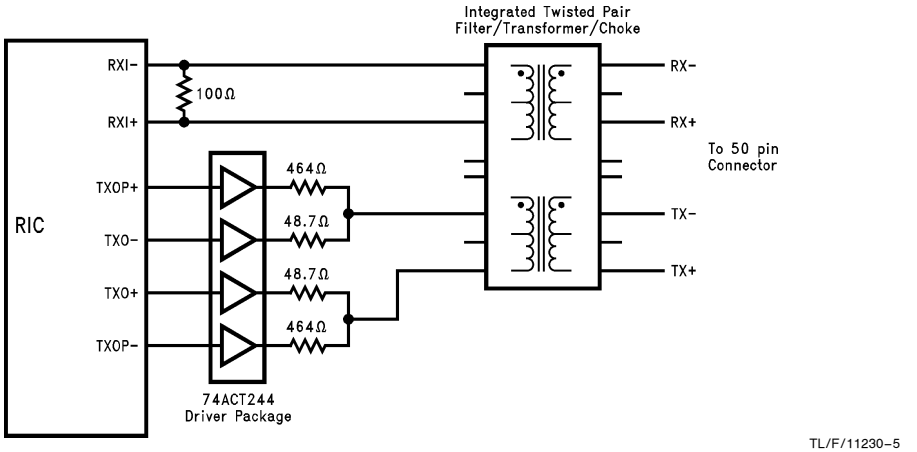

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FIGURE 5. TP Interface

To drive the transmitted signal through 100 meters of Twisted Pair cable, the RIC requires external buffers. The resistor network on the transmit path shows the values used on the Main board. A more optimized network, which allows for better amplitude control is described in the TP Parametrics Evaluation document. The Filter/Transformer/Choke package used here is the PE65431 from Pulse Engineering. Other packages have been evaluated, and those results are described in the TP Parametrics Evaluation Document.

2.1.6 AUI Interface

The AUI includes the proper terminations and pulldowns, and the isolation transformer. A 9-pin connector is used instead of the standard 15-pin AUI connector (due to space limitations). A 9-pin to 15-pin special adapter cable is used to attach to the MAU.

3.0 DISPLAY BOARD DESCRIPTION

The Display board allows for the display of Maximum mode or Minimum mode LED configurations. The LED display address and data information RD(7:0), and the strobe signals STR(1:0) signals are received from the Main Board through the 25-pin ribbon cable and driver. The data is driven to two arrays of addressable latches and one flip-flop.

In the Maximum LED display mode all 66 LEDs are functional. Five sets of Latches are used and are arranged into five sets, with two latches per set. Each set controls one of the following groups of LEDs: Receive (REC), Collision (COL), Partition (PART), Good Link (GDLINK), and Bad Polarity (BDPOL).

The address bits for the latches are obtained from the RD(7:5) signals. On the top half of the array address 0 corresponds to the ''any port'', address 1 corresponds to the AUI port, and addresses 2 to 7 corresponds to ports 2 through 7. The top array is enabled by the STR0 signal. The bottom half is enabled by the STR1 signal, and addresses 0 through 5 correspond to ports 8 through 13.

The data is obtained from the RD(4:0) signals as follows: RD(0) for LINK, RD(1) for Collision, RD(2) for Receive, RD(3) for Partition, and RD(4) for Polarity.

In the Minimum LED display mode four LEDs are displayed: Any port collision (ACOL), Any port reception (AREC), Any port jabbering (JAB) and Any port partitioned (APRT), which indicate any activity on any of the RIC ports. In this mode the flip-flop ('ALS374) should be inserted into the socket (U6), which is left blank (default for the Maximum display Mode). The flip-flop passes the four LED signals to port 13, and STR0 is used as the clock.

4.0 BACKPLANE BOARD DESCRIPTION

This board forms the Backplane BUS for the HUB. There are four types of signals that are passed on this BUS.

1. The Inter-RIC BUS signals: IRE, IRC, IRE. These signals are passed from the Receiving RIC to all the other RICs in the HUB. They can also be used by a modified DP839EB-ATS SONIC board to allow the SONIC to transmit to the network through all the RICs on the HUB.
2. The Arbitration and Control signals: SACKI, SACKO, ACTN, ANYXN, COLN. These signals are passed between all the RICs on the HUB to assure the proper operation of the HUB per the IEEE802.3 state diagrams. When a board is inserted into a slot on the Backplane board, a jumper is removed to allow for the SACKI-SACKO signals to pass to and be asserted by the Main board. If there is no Main board inserted in a slot, that jumper should be inserted to short SACKI to SACKO, in order to complete the arbitration chain.
3. The Management BUS signals: MRXC, MRXD, MCRS, PCOMP. The MRXC, MRXD and MCRS signals are used to pass the management information from the receiving RIC to a SONIC board. PCOMP is a unidirectional signal that is asserted onto the BUS by a separate controller board that can gather management statistics to compress the data portion of the management information. The MCRS signal is also used as an input to the RIC as described in Section 2.1.3).
4. The Parallel arbitration vector, ARB(3:0), required for parallel arbitration (as described in Section 2.2.2).

Each of the BUS lines is terminated by approximately 20Ω (two 39Ω resistors in parallel).

5.0 PAL LISTINGS

```
U43  device 'p16L8';module RIC_DEC
title     'decode AT addresses


"inputs

sa0       pin  11;
sa1       pin  9;
sa2       pin  8;
sa3       pin  7;
sa4       pin  6;
sa5       pin  5;
sa6       pin  4;
sa7       pin  3;
sa8       pin  2;
sa9       pin  1;
ba0       pin  16;
ba1       pin  17;
aen       pin  18;
iow       pin  13;
ior       pin  14;

"outputs

ghit      pin 19;
bhit      pin 12;
io        pin 15;
base0 =  !aen & !sa9 & sa8 & !sa7 &  !ba1 & !ba0;
base1 =  !aen & !sa9 & sa8 & !sa7 &  !ba1 & ba0;
base2 =  !aen & !sa9 & sa8 & !sa7 &  ba1 & !ba0;
base3 =  !aen & !sa9 & sa8 & !sa7 &  ba1 & ba0;

low   =  !aen & sa9 & !sa8 & !sa7 & !sa4 & !sa3 & !sa2 & !sa1
       & !sa0;

equations

!ghit     =  low & !ba1 & !ba0 & !sa6 & !sa5
           # low & !ba1 & ba0 & !sa6 & sa5
           # low & ba1 & !ba0 & sa6 & !sa5
           # low & ba1 & ba0 & sa6 & sa5;

!bhit     =  !sa6 & !sa5 & base0
           # !sa6 & sa5 & base1
           # sa6 & !sa5 & base2
           # sa6 & sa5 & base3;

!io       = !iow # !ior;

END  RIC_DEC;
```

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```
U36  device 'p20L8';ric_ctrl1
title 'ric control and some AT interface'

"inputs

     mloaddly  pin  23;
     ior       pin  14;
     iow       pin  13;
     rstdrv    pin  11;
     bufen     pin  10;
     rdy       pin   9;
     ea2       pin   8;
     ea1       pin   7;
     ea0       pin   6;
     richit    pin   5;
     ghit      pin   4;
     bhit      pin   3;
     io        pin   1;

"outputs

     chrdy     pin  21;
     ireg      pin  20;
     rd        pin  19;
     wr        pin  18;
     iorb      pin  17;
     dens      pin  16;
     cdec      pin  15;
     den       pin  22;

     norm      = !ea2 & !ea1 & !ea0;

equations

     !chrdy    = 1;

     enable chrdy  = !bhit & richit & rdy & !io;

     !dens     = !io & (!ghit # (!bhit & richit));

     !ireg     = !ghit & !iow;

     !rd       = richit & norm & !bhit & !ior;

     !wr       = richit & norm & !bhit & !iow;

     !iorb     = !ior;

     !cdec     = !ea2 & !ea1 & ea0 & !ghit & !ior
                 # !ea2 & ea1 & !ea0 & richit & !ghit & !ior;

     !den      = richit & !bhit & !bufen & norm & !io;


     end ric_ctrl1;
```

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```
U41  device 'p20L8';ric_ctrl2;
title  'ric control 2a

"inputs

     mloaddly   pin 23;
     ior        pin 14;
     iow        pin 13;
     rstdrv     pin 11;
     bufen      pin 10;
     rdy        pin  9;
     ea2        pin  8;
     ea1        pin  7;
     ea0        pin  6;
     richit     pin  5;
     ghit       pin  4;
     bhit       pin  3;
     sln        pin  2;
     pken       pin  1;
     rstb       pin 16;
     men        pin 17;

"outputs

     swen       pin 21;
     raen       pin 20;
     rst        pin 19;
     mload      pin 18;
     enpken     pin 22;
     enmen      pin 15;

equations

     !swen      = !mload & !mloaddly;

     !raen      = mload & mloaddly;

     !rst       = rstdrv # !rstb;

     !mload     = rstdrv
                # ea2 & !ea1 & !ea0 & richit
                # !ea2 & ea1 & ea0
                # !rstb;

     !enpken    = !sln & !pken;

     !enmen     = !sln & !men;


     end ric_ctrl2;
```

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```
U33  device 'p20v8r';module ric_ack
title 'ric arb state machine


"inputs

     enarb     pin  14;
     unused_1  pin  11;
     psel      pin  23;
     sln       pin  10;
     sacki     pin   9;
     actn_s    pin   8;
     actn_d    pin   7;
     anyxn_d   pin   6;
     unused_3  pin   5;
     unused_4  pin   4;
     unused_5  pin   3;
     match     pin   2;
     clk       pin   1;

"outputs

     ackiric   pin  15;
     arbwin    pin  18;
     arbdone   pin  20;
     q1        pin  21;
     q0        pin  22;
     Q20M      PIN  17;

"counter states
     s0 = ^b00;
     s1 = ^b01;
     s2 = ^b10;
     s3 = ^b11;

"counter modes
     mode = [enarb];
     count = [1];
     clear = [0];

state_diagram [q1,q0]

     state s0: case (mode == clear): s0;
                    (mode == count): s1;
          endcase;

     state s1: case (mode == clear): s0;
                    (mode == count): s2;
          endcase;

     state s2: case (mode == clear): s0;
                    (mode == count): s3;
          endcase;
```

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```
     state s3: case (mode == clear): s0;
                    (mode == count): s3;
          endcase;

equations

arbdone = q1 & q0;

arbwin  = (!anyxn_d # arbdone) & match & enarb;

!ackiric = !sln & (psel & (ackiric & (actn_s & actn_d & arbdone &
          !arbwin # actn_s & !actn_d & anyxn_d & !arbwin)
          # !ackiric & (anyxn_d & !arbwin # !anyxn_d & actn_s))
          # !psel & !sacki);

!Q20M := Q20M;


end ric_ack;
```

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```
U1  device 'p20l8';module ric_arb
title 'arbitration pal


"inputs

     arbi0          pin  1;
     arbi1          pin  2;
     arbi2          pin  3;
     arbi3          pin  4;
     sel0           pin  5;
     sel1           pin  6;
     sel2           pin  7;
     sel3           pin  8;
     anyxn_d        pin  9;
     actn_d         pin 10;

"outputs

     match          pin 17;
     enarb          pin 22;
     arbo0          pin 18;
     arbo1          pin 19;
     arbo2          pin 20;
     arbo3          pin 21;

equations

     enarb    = actn_d # anyxn_d;

     match    = (!arbi3 # sel3) & (!arbi2 # sel2)
                & (!arbi1 # sel1) & (!arbi0 # sel0);

     arbo3    = sel3;

     arbo2    = sel2 & (!arbi3 # sel3);

     arbo1    = sel1 & (!arbi3 # sel3) & (!arbi2 # sel2);

     arbo0    = sel0 &(!arbi3 # sel3) & (!arbi2 # sel2)
                & (!arbi1 # sel1);


end ric_arb;
```

TL/F/11230–11

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998

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