Integrated Manufacturing Control Using the Data Quad Switch EEPROM—NM95C12

National Semiconductor
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INTRODUCTION

Manufacturing methods and testing techniques have become increasingly automated over the past few years. Of current interest are techniques which allow automated access to manufacturing information which, in turn, is used to tailor test and set up for individual manufactured assemblies. This note explores the application of the latest generation of memory devices to manufacturing control situations and integrating access schemes for test, in system programming and manufacturing control.

WHAT INFORMATION?

The first question raised in manufacturing control applications is what information needs to be accessable. In most cases information like serial number, date of manufacture, and revision number need to be written once during initial manufacture. Ideally, this information should be secure (i.e., read only). As a product passes through test additional data may be recorded such as calibration constants or configuration data. If an assembly should fail, the type of failure and number of recurrences may be recorded at the repair depot to determine, for example, if this assembly should be scrapped.

All of this data does not require a large memory device. National Semiconductor's family of serial access E^{2}PROMs are ideal candidates because of low cost, small footprint and ease of access.

SECURITY

The issue of data security is addressed by the 93CSXX family of devices. In these units a portion (or all) of the memory area may be set up to appear as ROM (once desired data has been loaded into the device). The amount of ROM vs PROM is determined by a value in the protection register which delimits the portion of the device that is write protected. For details refer to AN-507 — Using the 93CSXX MICROWIRE™ family.

Some of the synchronous bus devices (24CXX I^{2}C family) have write protection of the upper half of the memory space by bringing a control line (WP) high.

ACCESS

In the most basic form of automated manufacturing control, an E^{2}PROM is simply added to a circuit assembly as an isolated block. There may be no electrical connection between the memory and any portion of the circuit assembly. A means of accessing the pins of the memory device must be considered. This may involve adding extra contacts to a card edge, creating a separate pin-type connector area or simply providing BON (Bed Of Nails) access. The latter may prove impractical with the increased use of surface mount.

A more promising and efficient use of board resource can be realized if the memory device shares I/O pins and power supply with the host assembly. The number of access points required for varying applications schemes ranges from 2 (for synchbus with no security) to 5 (for microwire with full security).

To take maximum advantage of the E^{2}PROM it is often desirable to allow access both externally (like the isolated case) and internally by the system resident on the circuit assembly.

An example of shared functionality is given in *Figure 1* which allows the resident system to flag a fault condition. The unique feature of this is the fault flag will be valid even if system power is cycled on and off or the board removed from the system. The visible flag (an LED) allows a technician to quickly identify a problem board. Additional information (i.e., a fault code) can be written into the E^{2}PROM as well. The module, when returned for repair, contains all the traditional manufacturing information as well as the fault code.

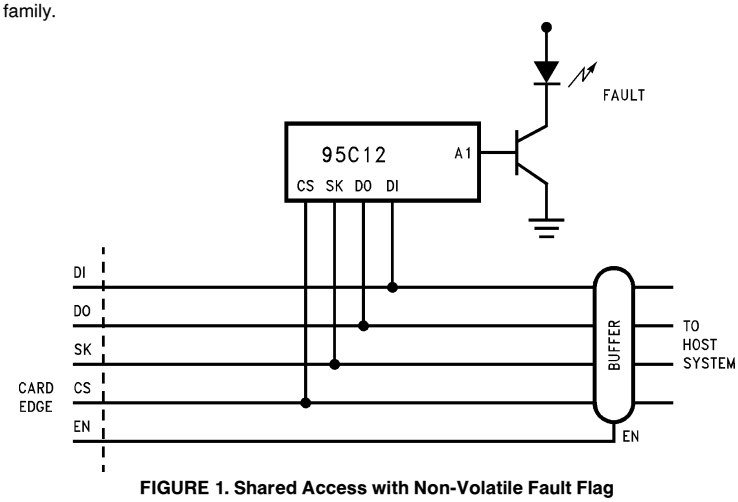

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FIGURE 1. Shared Access with Non-Volatile Fault Flag

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INTEGRATION WITH OTHER FUNCTIONS

The trend towards more electronics in smaller packages has led to the acceptance of surface mount technology. Traditional test access methods (BON) has become impractical at present density levels and virtually impossible when SMD's are mounted on both sides of the board.

To facilitate surface mount board testing, electronic rather than mechanical techniques have evolved. The solution often consists of boundary scan and some form of built in self test (BIST).

JTAG (Joint Test Action Group), sponsored by the IEEE P1149-1 Working Group, has defined a boundary scan standard which has become widely endorsed. This JTAG standard specifies that each conforming IC have a Test Access Port (TAP) which allows devices to be connected in series and minimizes interconnect overhead *(Figure 2)*. The boundary scan register (double buffered) gives access to the device pins for testing. The rest of the structure provides an instruction decode, a bypass function and any product specific requirements through additional registers (shown in dashed lines).

Surveying current programmable logic trends, GAL type devices are extremely popular to replace small blocks of random logic. One disadvantage is that traditionally each different ''pattern'' would have to be programmed, tested and identified prior to being installed on the assembly. With SMT versions of these devices, handling alone poses a significant inconvenience.

The concept of programming devices after they have been installed (ISP — In System Programming) is beginning to attract interest.

What do these test and ISP techniques have in common with manufacturing control? — serial board access.

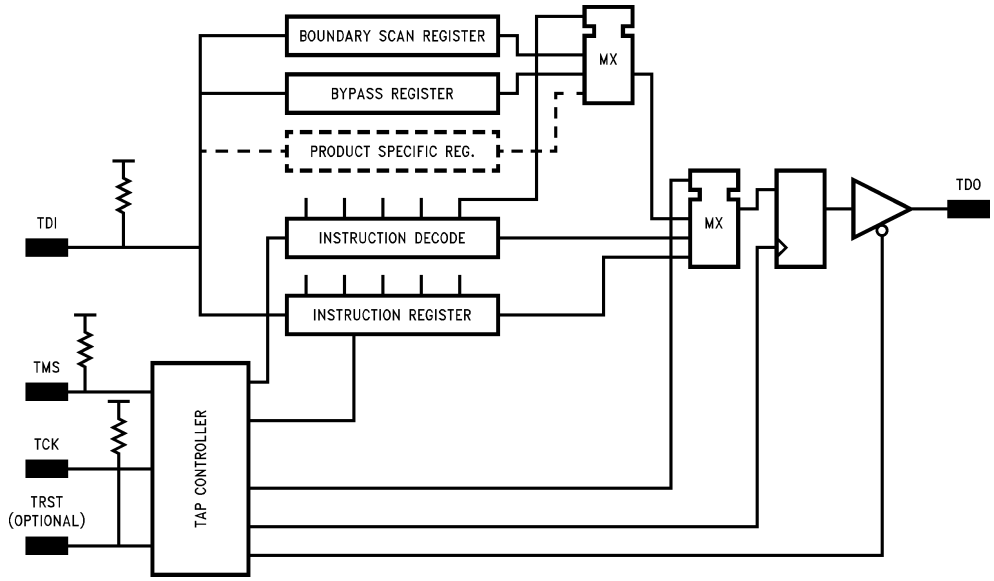

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FIGURE 2. JTAG Test Access Port

Let's consider a typical high density PCB assembly *(Figure 3)*. This assembly requires boundary scan testing, uses ISP GALS and implements a serial E^{2}PROM for manufacturing control data.

All 3 functions require a serial access scheme. If each is considered independently, a considerable number of pins would have to be dedicated to these functions (at least 12 connection points). One common bus and a common protocol to access management information, provide test access, and perform incircuit PLD programming would be ideal.

AN EXAMPLE COMMON ACCESS SYSTEM

The circuit of *Figure 3* uses a COP 822 microcontroller to create a JTAG to MICROWIRE converter with added support for an ISP PLD loop and an E^{2}PROM with security for manufacturing control. The combined test, manufacturing data and PLD programming requires only 5 access pins.

Because JTAG test access often requires high speed, this system has been broken down as two JTAG loops (hence two TMS pins), one high speed dedicted to the test loop and a slower speed loop dedicated to E^{2}PROM and PLD access through the COP 822. The speed of this JTAG loop is limited by COP processing speed in translation to MICROWIRE.

This approach represents a solution for common access using devices available today. As standards take hold (like JTAG) then non-volatile memories and ISP PLD's may appear supporting a **standard** serial protocol and further reducing the overheads in a common access scheme.

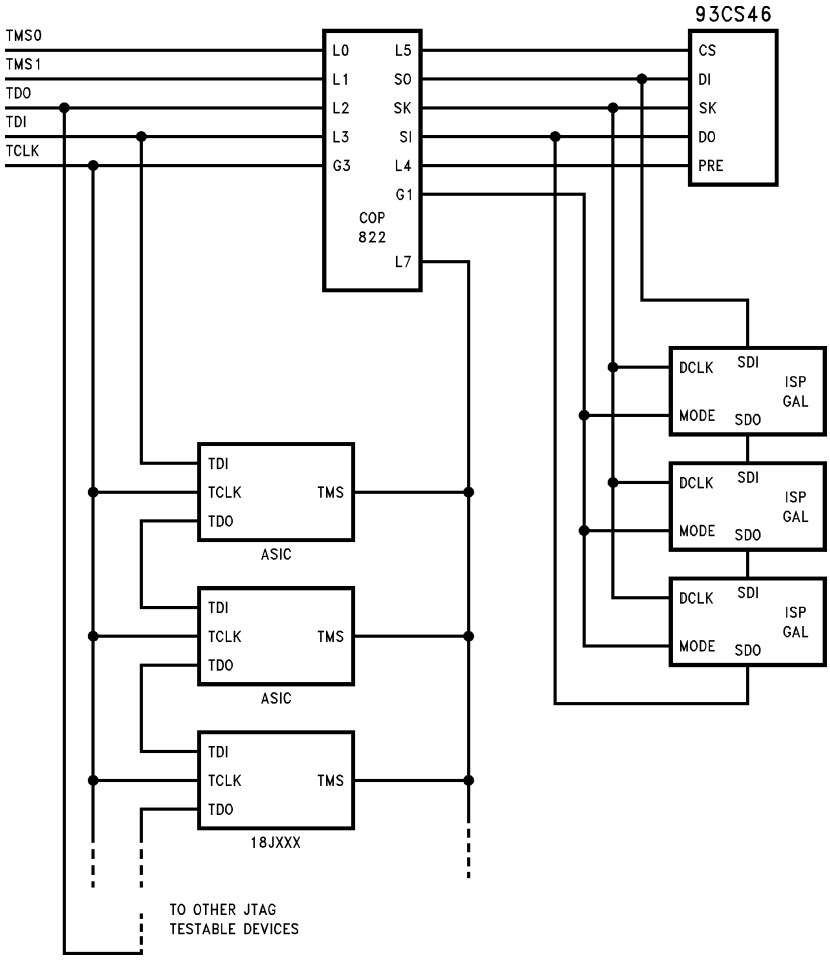

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FIGURE 3. Common JTAG Access for Test, ISP, and Manufacturing Control

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