

# NM95C12 EEPROM Controls Amplifier Gain

National Semiconductor  
Application Note 790  
Harry W. Lewis  
June 1991



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## BACKGROUND

Electrically Erasable PROM or EEPROM finds wide application in analog data acquisition. When using sensors, some possibilities include storing calibration constants (gain, nonlinearities, temperature effects and offset), the engineering units of measurements, and even keeping serial numbers. In *Figure 1* for example, after an A/D converter converts the analog sensor output, the processor can use correction factors from the EEPROM to get a final value. By keeping these corrections with the sensor assembly, one can effectively get a more accurate sensor.

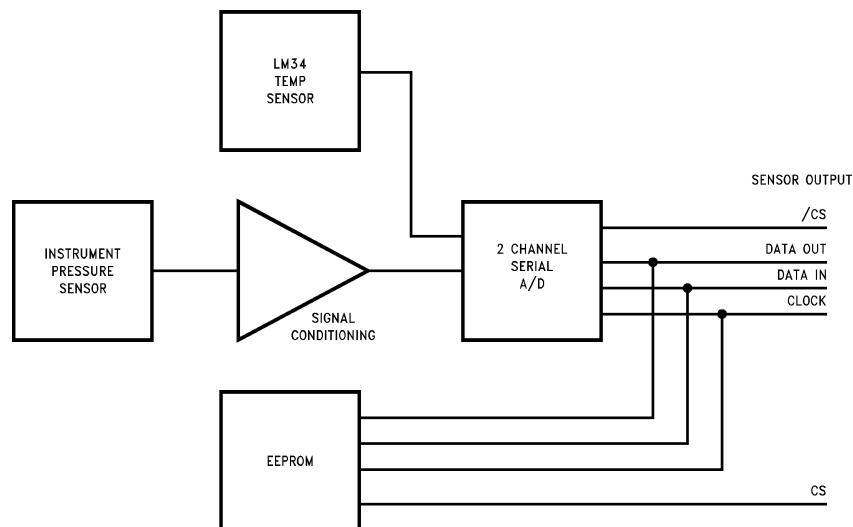
There are several ways to achieve a wide input range when required. One way is to use an A/D with more bits than needed and then use the extra bits for ranging. In other words, if 8 bits are needed for the output by using a 10-bit converter a full scale resolution of 8 bits is still provided even if the input range is only  $\frac{1}{4}$  of the converter range. This can get expensive quickly since the price of accurate A/Ds goes up substantially with the number of bits! Even so, with advances in audio parts of 16 to 18 bits, this could be viable in some instances.

A more common way to cover wide range inputs is to scale the incoming levels to close to the maximum rated input range of the A/D. If the input range is  $0 \rightarrow 0.2V$  and the

converter is rated  $0 \rightarrow 5V$ , a gain of 25 in front of the A/D will give the full resolution over the reduced range. Additionally, the input range can be offset from zero. While many A/Ds have range and offset options, there are limits if the accuracy is to be kept. A circuit to use both scaling and offset is *Figure 2*. The gain and offset are mostly determined by the reference and the resistor ratios.

$$V(A/D) = V_{IN} (1 + R3 * (R1 + R2)/(R1 * R2)) - V_{REF} * R3/R1$$

Common metal film resistors are widely sourced and have good temperature coefficients. Type RN55 T-2 are rated at  $\pm 50$  ppm/ $^{\circ}C$ . The difficulty comes with their resistance specification of  $\pm 1\%$ . Since most gain stages require at least 2 resistors to determine gain, the system accuracy is already reduced to, at best, 2%. Multiple stages and other error sources compound the problem. Some 10-bit serial A/Ds have 0.1% accuracy! Even the lowly 8-bit converter can be  $\frac{1}{2}\%$ . For the circuit in *Figure 2*, EEPROM is a very handy way to store the calibration of the low cost resistors to get more of the full accuracy capability of the A/D. Even when not using a sensor, EEPROM can be useful for calibrating a scaling and offset circuit. This is especially true now that low cost A/D converters have gotten so accurate.



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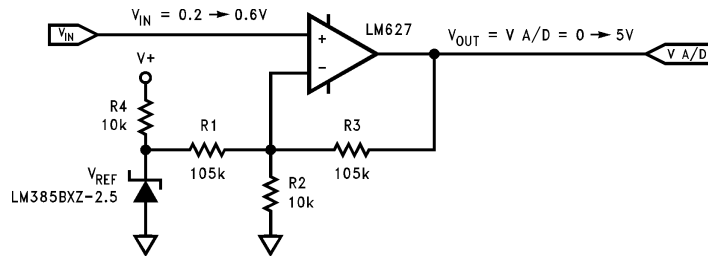
Full Scale (5V) = 4720 PSI  
Zero (0V) = -83 PSI  
Temp Coefficient = +0.2 PSI/ $^{\circ}F$   
Serial # = 184625  
Last Rev = F

FIGURE 1. Sensor with Digital Output and Correction Factors

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$$V_{OUT} = V_{A/D} = V_{IN} \left( 1 + \frac{R_3(R_1 + R_2)}{R_1 \cdot R_2} \right) - \frac{R_3}{R_1} V_{REF}$$

$$= 12.5 \cdot V_{IN} - 2.5V$$

FIGURE 2. Scaling and Offset Circuit

### DON'T BE A DIP

For storing data, EEPROM can generally beat DIP switches. However, there were some other things that DIP switches could do better. One case was having external access to logic levels without needing an additional port chip. Another area was switching analog voltages. To replace an analog DIP switch, a designer often had to add an output port and a separate CMOS or other switch to do the actual switching. The NMC95C12 1024-bit CMOS EEPROM with DIP switches attacks both these areas. When first glancing at the data sheet, the title "EEPROM with DIP switches" can conjure up visions of the data being stored in 1024 tiny levers on top of the package! Of course that is not the case, see *Figure 3* for the real block diagram. Actually the part has 61 words of 16 bits of EEPROM for general use. That totals 976 bits. The DIP switches referenced in the title are 8 pins with switch logic to allow several different modes of operation as controlled by the switch configuration register. There is a nonvolatile Initial Switch Setting Register of 16 bits. And, finally, a Switch Readback Register allows the pins to be used as a digital input port. Processor interface is by a serial MICROWIRE™ port.

### THE BIG SWITCH

Switches are the main difference between the NM95C12 and other EEPROMs. They can be thought of as four independent switches each having two pins, A and B. Each switch has four control bits labeled W, X, Y and Z to set it to one of its 14 modes. Table I shows all the modes. The Switch Configuration Register (SCR *Figure 4*) is 16 bits long to hold all four bits of each of the four switches. It is not made from EEPROM cells so it can be written faster and there is no wearout mechanism. Being volatile, the SCR is reloaded at each powerup from the EEPROM Initial Switch Setting Register.

### WHERE DID THE PARALLEL PORT COME FROM?

Switch modes 0-3 allow the 2 pins to be digital outputs. When bits Y and Z are set to 0, A = X and B = W. Other modes allow A and/or B to be TRI-STATE® for use as digital inputs or I/O. *Figure 5* shows the switches being used for

general input and output, to set gain controls, and to drive analog multiplexers. In *Figure 5*, the port of U4 selects the input channel of the A/D via the multiplexer U3. Input channel 7 has a selectable gain preamplifier (U1) whose gain is controlled by U2 selecting the proper feedback tap. The resistor values for R1, R2, R3 and R4 are standard 1% values. Ideally the values would be 48K, 12K, 3K and 1K. Although they are not quite correct for the gains desired, calibration values stored in the EEPROM can correct for this while fixing the other errors. One thing to keep in mind when selecting the standard values, make sure the A/D stays in its active range during the whole range of expected signal input. If the A/D needed to exceed the maximum count, the error generated is not correctable. This implies making the gains on the low side.

### MODES 12 AND 13?

Mode 12 is an open ( $10 + M\Omega$ ) between pins A and B. Mode 13 is an ANALOG short ( $200\Omega$  or less) between the same pins. In *Figure 6*, analog switches give variable gains and do analog multiplexing. Switches 1 and 2 select the input to the A/D. Switches 3 and 4 control gain. Although the pins used for a closed analog switch can not be read as an input, the input function of the Switch Readback Register will still work for the other pins, so mixed analog and digital operation is possible. Of course, errors in the amplifier gains will be corrected by storing calibration constants in the EEPROM section of the part.

### FINALLY!

The NM95C12 can accomplish what a DIP switch used to do without the extra parts. You have external access to logic levels and you can even switch analog voltages. All without needing additional port or multiplexer chips.



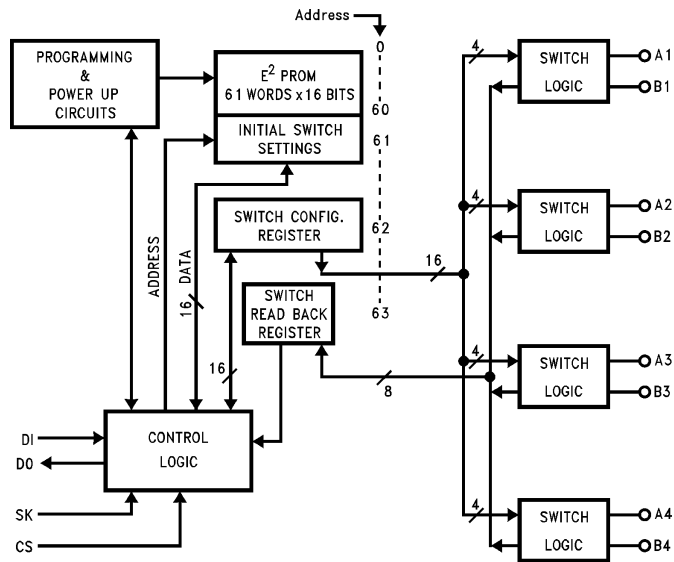
Table I. Switch Configurations

MODE*	Z	Y	X	W	SWITCH CONFIGURATION	COMMENTS
0	0	0	0	0		A = 0 , B = 0
1	0	0	0	1		A = 0 , B = 1
2	0	0	1	0		A = 1 , B = 0
3	0	0	1	1		A = 1 , B = 1
4	0	1	0	0		A = 0 , B = TRI-STATE
5	0	1	0	1		A = B
6	0	1	1	0		A = $\bar{B}$
7	0	1	1	1		A = 1 , B = TRI-STATE
8	1	0	0	0		A = TRI-STATE , B = 0
9	1	0	0	1		B = A
10	1	0	1	0		B = $\bar{A}$
11	1	0	1	1		A = TRI-STATE , B = 1
12	1	1	0	X		Analog Switch Open
13	1	1	1	X		Analog Switch Closed

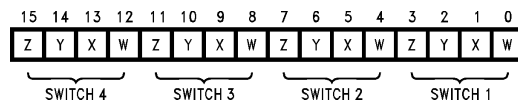
\*Modes 0 thru 11 are logic level functions. Modes 12 and 13 are Analog switch functions.

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**FIGURE 3. Block Diagram**



**FIGURE 4. Switch Configuration Register (SCR)**



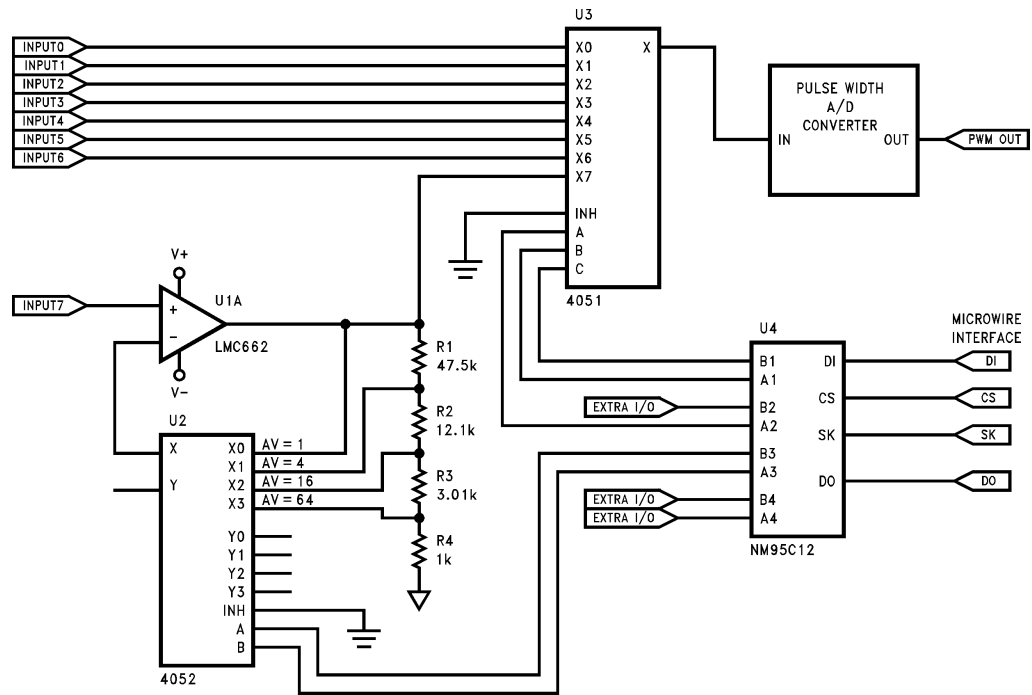
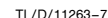


FIGURE 5. Using NM95C12 Switches as Digital I/O

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**FIGURE 6. Using NM95C12 Switches as Analog Switches**

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**National Semiconductor GmbH**  
Livry-Gargan-Str. 10  
D-82256 Fürstenfeldbruck  
Germany  
Tel: (81-41) 35-0  
Telex: 527649  
Fax: (81-41) 35-1

**National Semiconductor  
Japan Ltd.**  
Sumitomo Chemical  
Engineering Center  
Bldg. 7F  
1-7-1, Nakase, Mihama-Ku  
Chiba-City,  
Ciba Prefecture 261  
Tel: (043) 299-2300  
Fax: (043) 299-2500

**National Semiconductor  
Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semiconductores  
Do Brazil Ltda.**  
Rue Deputado Lacorda Franco  
120-3A  
Sao Paulo-SP  
Brazil 05418-000  
Tel: (55-11) 212-5066  
Telex: 391-1131931 NSBR BR  
Fax: (55-11) 212-1181

**National Semiconductor  
(Australia) Pty, Ltd.**  
Building 16  
Business Park Drive  
Monash Business Park  
Nottingham, Melbourne  
Victoria 3168 Australia  
Tel: (3) 558-9999  
Fax: (3) 558-9998