

Using an EEPROM— I²C™ Interface NM24C02/03/04/05/08/09/ 16/17

National Semiconductor
Application Note 794
N. Brian Underwood
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INTRODUCTION

National Semiconductor's NM24C EEPROMs are designed to interface with Inter-Integrated Circuit (I²C) buses and hardware. NSC's electrically erasable programmable read only memories (EEPROMs) offer valuable security features (write protection), two write modes, three read modes and a wide variety of memory sizes. Applications for the I²C bus and NM24C memories are included in SANs (small-area networks), stereos, televisions, automobiles and other scaled-down systems that don't require tremendous speeds but instead cost efficiency and design simplicity.

I²C BACKGROUND

The I²C bus configuration is an amalgam of microcontrollers and peripheral controllers. By definition: a device that transmits signals onto the I²C bus is the "transmitter" and a device that receives signals is the "receiver"; a device that controls signal transfers on the line in addition to controlling the clock frequency is the "master" and a device that is controlled by the master is the "slave". The master can transmit or receive signals to or from a slave, respectively, or control signal transfers between two slaves, where one is the transmitter and the other is the receiver. It is possible to combine several masters, in addition to several slaves, onto an I²C bus to form a multimaster system. If more than one master simultaneously tries to control the line, an arbitration procedure decides which master gets priority. The maximum number of devices connected to the bus is dictated by the maximum allowable capacitance on the lines, 400 pF, and the protocol's addressing limit of 16k; typical device capacitance is 10 pF. Up to eight E²PROMs can be connected to an I²C bus, depending on the size of the memory device implemented.

Simplicity of the I²C system is primarily due to the bidirectional 2-wire design, a serial data line (SDA) and serial clock line (SKL), and to the protocol format. Because of the effi-

cient 2-wire configuration used by the I²C interface compared to that of the MICROWIRE™ and SPI interface, reduced board space and pin count allows the designer to have more creative flexibility while reducing interconnecting cost.

OPERATING NATIONAL SEMICONDUCTOR'S NM24Cs

The NM24C E²PROMs require only six simple operating codes for transmitting or receiving bits of information over the 2-wire I²C bus. These fields are explained in greater detail below and briefly described hereafter: a start bit, a 7-bit slave address, a read/write bit which defines whether the slave is a transmitter or receiver, an acknowledge bit, message bits divided into 8-bit segments and a stop bit.

For efficient and faster serial communication between devices, the NM24C Family features page write and sequential read.

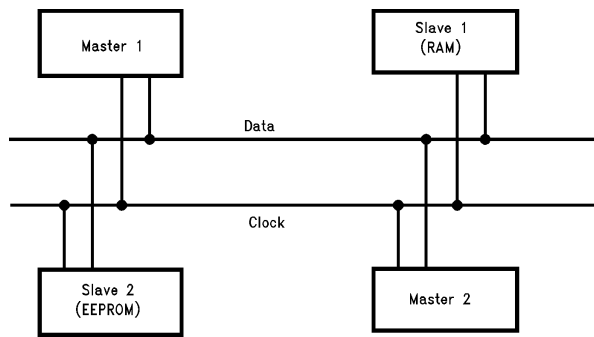
The NM24C03/C05/C09/C16/C17 Family offers a security feature in addition to standard features found in the NM24C02/C04/C08/C16 Family. The security feature is beneficial in that it allows Read Only Memory (ROM) to be implemented in the upper half of the memory to prevent any future programming in that particular chip section; the remaining memory that has not been write protected can still be programmed. The security feature in the NM24C03/C05/C09/C17 Family does not require immediate implementation when the device is interfaced to the I²C bus, which gives the designer the option to choose this feature at a later date. Table I displays the following parameters: memory content, write protect and the maximum number of individual I²C E²PROMs allowed on an I²C bus at one time if the total line capacitance is kept below 400 pF.

Code used to interface the NM24Cs with National Semiconductor's COP8 Microcontroller Family is listed in a latter section of this application note for further information to the reader.

TABLE I

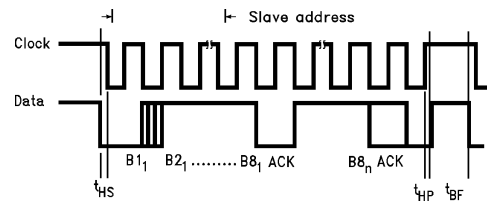
Part No.	Number of 256x8 Page Blocks	Write Protect Feature	Max. Parts
NM24C02	1	No	8
NM24C03	1	Yes	8
NM24C04	2	No	4
NM24C05	2	Yes	4
NM24C08	4	No	2
NM24C09	4	Yes	2
NM24C16	8	No	1
NM24C17	8	Yes	1

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FIGURE 1. I²C-Bus Configurations



TL/D/11268-2

FIGURE 2. I²C Bus Timing

Start Condition

- Clock and Data line high (Bus free)
- Change Data line from high to low
- After $t_{HS}(\text{Min}) = 4 \mu\text{s}$ the master supplies the clock

Acknowledge

- Transmitting device releases the Data line
- The receiving device pulls the Data line low during the ACK-clock if there is no error
- If there is no ACK, the master will generate a Stop Condition to abort the transfer

Stop Condition

- Clock line goes high
- After $t_{HP}(\text{Min}) = 4.7 \mu\text{s}$ the Data lines go high
- The master maintains the Data and Clock line high
- Next Start Condition after $t_{FB}(\text{Min}) = 4.7 \mu\text{s}$ is possible

START/STOP CONDITIONS

If both the data and clock lines are HIGH, the bus is not busy. To attain control of the bus, a start condition is needed from a master; and to release the lines, a stop condition is required.

Start Condition: HIGH-to-LOW transition of the data line while the clock line is in a HIGH state.

Stop Condition: LOW-to-HIGH transition of the data line while the clock line is in a HIGH state.

The master always generates the start and stop conditions. After the start condition the bus is in the busy state. The bus becomes free after the stop condition.

DATA BIT TRANSFER

After a start condition "S" one databit is transferred during each clock pulse. The data must be stable during the HIGH-period of the clock. The data line can only change when the clock line is at a LOW level.

Normally each data transfer is done with 8 data bits and 1 acknowledge bit (byte format with acknowledge).

ACKNOWLEDGE

Each data transfer needs to be acknowledged. The master generates the acknowledge clock pulse. The transmitter releases the data line (SDA = HIGH) during the acknowledge clock pulse. If there was no error detected, the receiver will pull down the SDA-line during the HIGH period of the acknowledge clock pulse.

If a slave receiver is not able to acknowledge, the slave will keep the SDA line HIGH and the master can then generate a STOP condition to abort the transfer.

If a master receiver keeps the SDA line HIGH, during the acknowledge clock pulse the master signals the end of data transmission and the slave transmitter release the data line to allow the master to generate a STOP-condition.

ARBITRATION

Only in multimaster systems.

If more than one device are potential masters and more than one desires access to the bus, an arbitration procedure takes place: if a master transmits a HIGH level and another master transmits a LOW level, the master with the LOW level will get the bus and the other master will release the bus; and the clock line switches immediately to the slave receiver mode. This arbitration could carry on through many bits (address bits and data bits are used for arbitration).

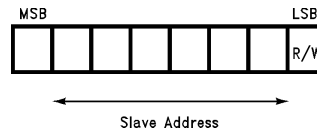
FORMATS

There are three data transfer formats supported:

- Master transmitter writes to slave receiver; no direction change
- Master reads immediately after sending the address byte
- Combined format with multiple read or write transfers.

ADDRESSING

The 7-bit address of an I²C device and the direction of the following data is coded in the first byte after the start condition:

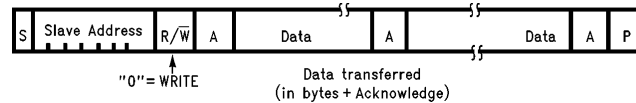


TL/D/11268-3

A "0" on the least significant bit indicates that the master will write information to the selected Slave address device; a "1" indicates that the master will read data from the slave.

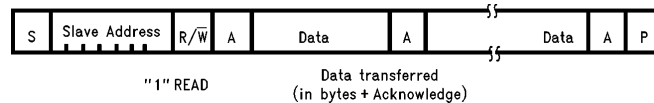
Some slave addresses are reserved for future use. These are all addresses with the bit combinations 1111XXX and 0000XXX. The address 00000000 is used for a general call address, for example, to initialize all I²C devices (refer to I²C bus specification for detailed information).

Master Transmits to Slave, No Direction Change



TL/D/11268-4

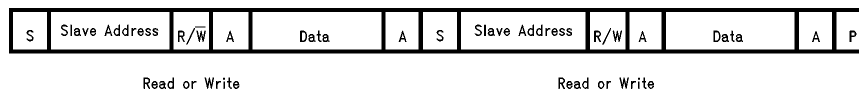
Master Reads Slave Immediately after First Byte



TL/D/11268-5

The master becomes a master receiver after first ACK

Combined Formats



TL/D/11268-6

n bytes Data + ACK n bytes Data + ACK
S = Start Condition A = Acknowledge P = Stop Condition

FIGURE 3. I²C-Bus Transfer Formats

TIMING

The master can generate a maximum clock frequency of 100 KHz. The minimum LOW period is defined as 4.7 μ s; the minimum HIGH period width is 4 μ s; the maximum rise

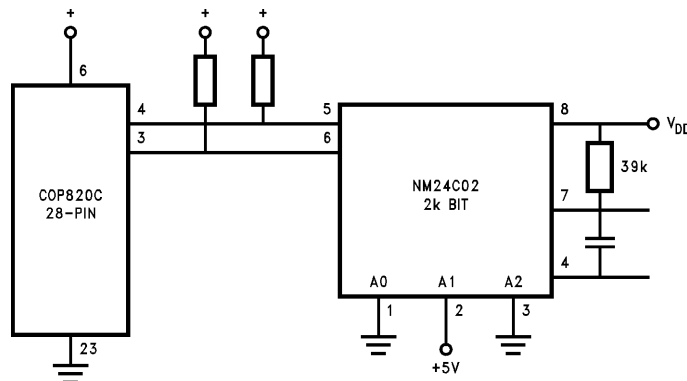
time on SDA and SCL is 1 μ s; and the maximum fall time on SDA and SCL is 300 ns.

Figure 4 shows the detailed timing requirements.

Symbol	Parameter	Min	Max	Units
f _{SCL}	SCL Clock Frequency	0	100	kHz
t _{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		μ s
t _{HD; STA}	Hold Time Start Condition. After this Period the First Clock Pulse is Generated	4.0		μ s
t _{LOW}	The LOW Period of the Clock	4.7		μ s
t _{SU; STA}	Setup Time for Start Condition (Only Relevant for a Repeated Start Condition)	4.7		μ s
t _{HD; DAT}	Data in Hold Time	5 0*		μ s μ s
t _{SU; DAT}	Setup Time Data	250		ns
t _r	Rise Time of Both SDA and SCL Lines		1	μ s
t _f	Fall time of Both SDA and SCL Lines		300	ns
t _{SU; STO}	Setup Time for Stop Condition	4.7		μ s

*Note that a transmitter must internally provide at least a hold time to bridge the undefined region (max. 300 ns) of the falling edge of SCL.

FIGURE 4. I²C-Bus Timing Requirements



TL/D/11268-7

FIGURE 5. I²C Bus EEPROM/μController Configuration Used for Sample Code

SOFTWARE TASKS

- Write fixed values to E2PROM cells
- Read values back from E2PROM and save in RAM locations from COP

Note: I²C Bus Modes Used:

Master Transmitter SDA → Slave Receiver
 SCL →
 Master Receiver ← SDA Slave Receiver
 SCL →

REMARKS

- The I²C bus, 2-wire serial interface generally requires a pull-up resistor on the SDA line and the SCL line, depending on whether TTL or CMOS hardware interfacing exists.

- I²C bus compatible μ C's or peripherals have OPEN DRAIN outputs at SDA and SCL.
- COP800 does not have OPEN DRAIN outputs, but the "bus requirements" can be met by switching SDA and SCL connections into TRI-STATE® for the following cases:
 - The bus is not accessed
 - A slave has to send an acknowledge bit.
- MICROWIRE can not be used for I²C bus operations.
- Current sink capability on SDA and SCL must be 3 mA to maintain "Low Level" (an I²C bus spec.).

```
.TITLE IIC - EEPROM  ROUTINES'
.INCLD COP800.INC
.CHIP 840
.LIST X'21
```

```
***TASK RELATED RAM - DECLARE***
```

```
EEADR          = 002      ; ADDRESS OF EEPROM
EEWRD          = 003      ; WORD ADDRESS EEPR.
EEDAT1         = 004      ; DATA TO EECCELL
EEDAT2         = 005      ; SECOND BYTE
FLAG           = 010      ; FLAG-WORD
EEREAD         = 012      ; READ-DATA FROM EE
               = 013      ; SECOND BYTE
               = 014      ; THIRD BYTE
               = 015      ; FOURTH BYTE
BITCO          = 0F0      ; COUNTER FOR BITSHFT
```

```
INIT:
```

```
LD SP,          #06F
LD B,           PORTLD      ; INIT LS, L3 FOR EE-
LD [B+],        #00C      ; OPERATIONS
LD [B],         #00C
LD B,           #EEDAT2    ; INIT RAMS
LD [B-],        #034      ; FIXEED VALUES FOR
LD [B-],        #012      ; EEWRITE (2 BYTES)
LD [B-],        #0A0      ; MIRROR OF #05
LD [B],         #025      ; MIRROR OF "A5"
```

```
*****
; EXAMPLE: IF ADDRESS BYTES IS "1010 010X THEN *
; STORE: "X010 0101 *
; INTO RAM (X=0/1; WRITE/READ) *
*****
```

```
LD PSW,         #00      ; LOAD PSW
LD CNTRL,       #00      ; AND CNTRL REG.
LD FLAG,        #0
.FORM
```

```
*****
; ***** DO WRITE TO EE-PROM *****
*****
```

```
; (2 BYTE SUCCESSIVE WRITE)
```

```
SBIT 0,         FLAG      ; SET FLAG FOR WRITE
LD B,           PORTLD    ; POINT LPORT DAT REG.
               ; TO MODIFY "SDA, SCL"
RBIT 2 [B],     ; PREPARE FOR START
JSR STACON      ; CONDITION.
JSR WAIT        ; AFTER WRITE TO EE.
               ; WAIT FOR > THAT 40
```

TL/D/11268-8

```

*****
; ** DO THE START CONDITION **
; ** AND SHIFT OUT ADDRESS - **
; ** BYTE AND WORD-ADDRESS **
*****

STACON:
  RBIT 3,
  LD B,

  PORTLD      ; FINISH START COND.
  #EEADR      ; PREPARE TO CLOCK
              ; OUT ADDRESS.

LOPA:
  LD BITCO,

  #008        ; DO SETS OF 8 BITS

LOPA 1:
  IFBIT 0, [B]
  JP ONE,
  RBIT 2,
  JP CLK

  PORTLD      ; SWITCH SDA BEFORE
              ; SCL
              ; SET BIT LEVEL "0"

ONE:
  SBIT 2,
  JP CLK

  PORTLD      ; SET BIT LEVEL "1"
              ; ENSURE SAME BIT
              ; LENGTH

CLK:
  SBIT 3,
  NOP
  NOP
  RBIT 3,
  RBIT 2,
  .FORM

  PORTLD      ; DO CLOCK PULSE
  PORTLD
  PORTLD      ; ENSURE > 4USEC
  PORTLD      ; SWITCH ALSO SDA LOW

  LD A, [B]
  RRC A,
  X A, [B]
  DRSZ BITCO
  JP LOPA1,
  LD A, [B+],
  IFBIT 1,
  JMP,

  FLAG
  GETDAT      ; ROTATE BYTE ONE
              ; BIT POS. RIGHT
              ; AND SAVE
              ; CHECK IF 8 BITS
              ; SHIFTED
              ; DECREMENT 8
              ; CHECK IF READ
              ; 3RD BYTE IS NEXT?
              ; IF SO, THEN READ.
              ; GET ACKNOWLEDGED
              ; WHEN 8 BITS ARE
              ; SHIFTED.

  JSR ACK,

  FLAG
  #04         ; CHECK IF READ
              ; OR WRITE OPERATION.
              ; ON READ (HERE)
              ; IF NOT 2 BYTES YET
              ; AFTER EE-ADDRESS AND
              ; WORD ADDRESS ARE SHFT.

  IFBIT 0,
  JP CEC1,
  IFBNE
  JMP LOPA,
  RET

CEC1:
  IFBNE,
  JMP LOPA,

  #06        ; 1ST AND 2ND DATA-
              ; BYTE (3RD + 4TH)

```

TL/D/11268-9

TL/D/11268-14

```

STP:
    SBIT 3,
    NOP,
    SBIT 2,
    RET,
    .FORM

                                PORTLD    ; ESTABLISH STOP-
                                PORTLD    ; CONDITION

                                *****
                                ; ** GET 8BIT OF DATA FROM EE-PROM **
                                *****

GETDAT:
    JSR ACK,
    LD B,
    JP

                                #EEREAD   ; GET ACKNOWLEDGMENT
                                GETDT1    ; POINT FIRST READ RAM
                                           ; AND READ IN

GETDAT:
    JSR ACK,
                                           ; ACKNOWLEDGMENT TO EE-
                                           ; PROM WHEN 8 BITS
                                           ; ARE SHIFTED IN.

GETDAT1:
    LD BITCO,
    RBIT 2,
    RBIT 2,

                                # 0 0 8   ; INIT BIT COUNTER
                                PORTLC    ; BEFORE READING, PUT
                                PORTLD    ; 'SDA' INTO HIGH-Z.

LOPB:
    SBIT 3,
    RBIT 7, [B]
    IFBIT 2,
    SBIT 7, [B]
    RBIT 3,
    DRSZ BITCO,
    JP SHFT
    LD A, [B+],
    IFBNE
    JMP GETDT,
    SBIT 2,
    JMP STP

                                PORTLD    ; DO CLOCK HIGH
                                PORTLD    ; READ IN EEDATA
                                PORTLD    ; IN SETS OF 8 BITS

                                PORTLD    ; DO CLOCK LOW
                                           ; CHECK IF 8 BITS
                                           ; ARE SHIFTED
                                           ; INCREMENT B
                                # 0 6     ; CHECK IF 4 BYTES
                                           ; ARE SHIFTED IN?
                                PORTLC    ; PUT L2=0
                                           ; WHEN TRUE, DO STOP
                                           ; CONDITION AND
                                           ; RETURN

    .FORM

SHIFT:
    LD A, [B],
    RRC A
    X A, [B]
    JP LOPB

                                ; ROTATE BITS ONE
                                ; POSITION RIGHT

                                *****
                                ; ** SIMPLE ROUTING TO DO 40 MSEC DELAY **
                                *****

```

TL/D/11268-12

WAIT:		
LD 0F1	#0.20	; SIMPLE WAIT LOOP
LOPD:		
LD 0F2,	#OFF	; TO PRODUCE > 40MSEC ; TIMEOUT
LOPC:		
DRSZ 0F2,		; TO PROPERLY PROGRAM
JP LOPC,		; EEPROM. TIME REQUIRED
DRSZ0F1,		; TO ERASE/WRITE
JP LOPD		; THE EEPART.
RET		
ACK1:		
SBIT 2,	PORTLC	; INDICATE TO EE-PROM
JP ACLK,		; (PUT DATA LINE LOW)
ACK:		
RBIT 2,	PORTLC	; PUT DATA-LINE HI-Z
ACLK:		
SBIT 3,	PORTLD	; AND GET ACKNOWLEDGE
NOP		; 8 BITS ARE SHIFTED,
NOP		; DO A DUMMY CLOCK
NOP		
RBIT 3,	PORTLD	; (FOR ACKNOWLEDGE)
SBIT 2,	PORTLC	
RET		
.END		

TL/D/11268-13

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livny-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527849
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998