Futurebus + Chip Set Pin Connections

National Semiconductor
Application Note 833
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October 1991

This applications brief describes pin connections of NSC transceivers and controllers to the Futurebus + connector as specified in Profiles B, A and F.

The pin connections assume that a board compliant to the Futurebus +, Profile B, will be implemented. The data path is 64 bits wide and the address width is 32 bits. Both central (required) and distributed (optional) arbitration schemes will be shown. The Profile B optional features for serial bus, tag byte, and full arbitration bus message system will also be shown. The packet mode data transfer option uses the transceiver devices in the same way shown, however, the Protocol Controller can not be used for packet mode transfers.

The components shown here are all pin numbered for the PLCC package. Using the PLCC package, it is difficult to meet the Profile B specification for maximum stub length when devices are mounted on a single side. The specification is 25 mm maximum, measured from the connector via to the center of the transceiver pin surface mount pad. Components can be mounted on both sides of the board and need to be for compliance to max stub length using 9-bit wide data transceivers. A recommended topographical layout is not included in this article. An experienced, talented layout person can experiment with component positioning to attain the shortest stub length with the tools and technology available for board manufacture. The solution to the stub length problem for the PLCC package is much more difficult than the PQFP package. The smaller PQFP package can easily meet the stub length specification by mounting the components on both sides of the board.

The interface has 15 transceiver devices, and 2 controllers.

1—DS3885 Arbitration Transceiver,

4—DS3884A Handshake Transceivers,

10—DS3883A or DS3886A Data Transceivers.

LOGICAL INTERFACE FUTUREBUS + ENGINE Protocol Controller (not included in this drawing), DS3875 Arbitration Controller.

A 0.1 μF capacitor is recommended for each package. The capacitor should be located as close to the package as possible. Additional protection against high frequency noise can be provided by a 0.001 μF capacitor in parallel with the recommended capacitor.

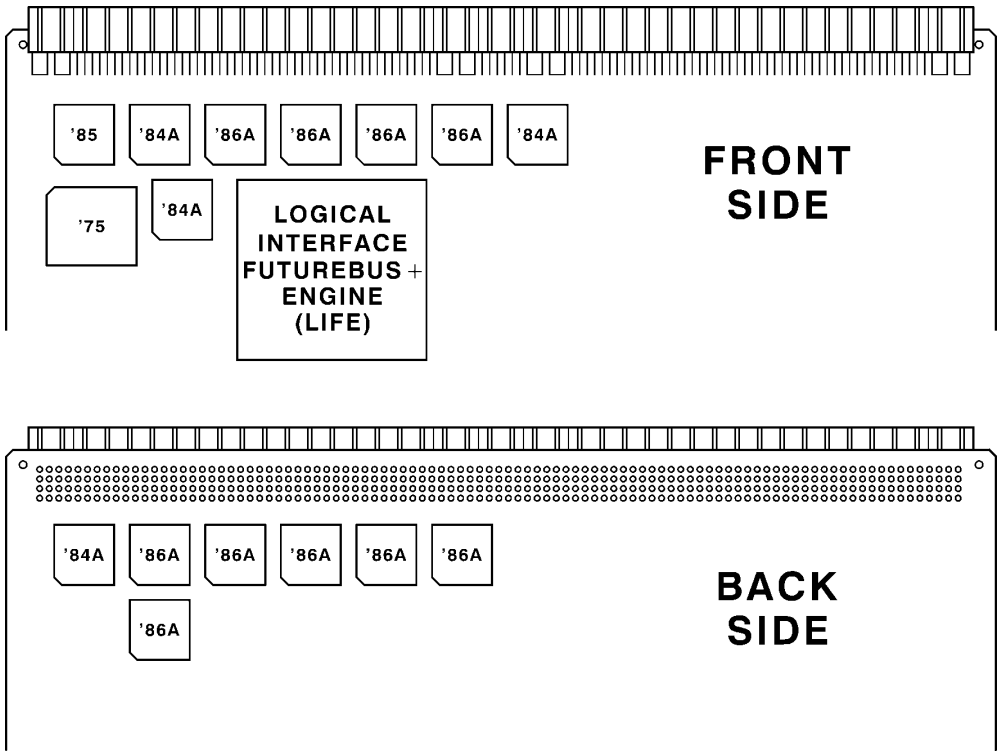

FIGURE 1. Layout for PLCC packages. Central and distributed arbitration, and 64-bits of address and data are supported. The LIFE is in a PQFP package.

  RRD-B30M66/Printed in U. S. A.

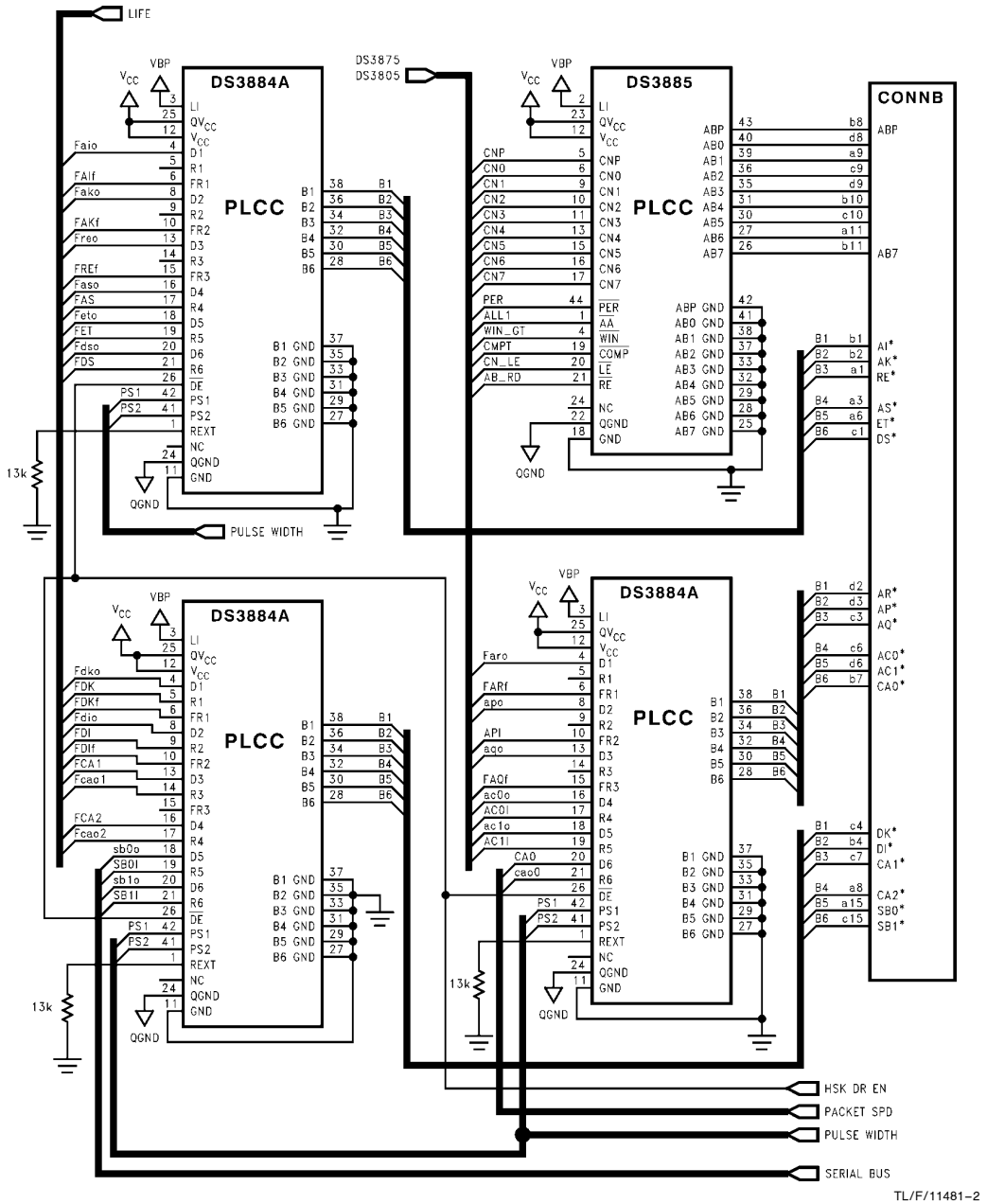

FIGURE 2. Arbitration and Handshake Transceivers

The DS3885 Arbitration Transceiver is used for message passing in the central arbitration scheme and for arbitration competition and message passing in distributed arbitration. In both arbitration schemes, it is connected to the bus exactly the same. In central arbitration, the DS3875 can be used to facilitate message transfers. It should be explained that the DS3885 preliminary data sheet pin names have been modified to match the pin names on the DS3875. This is reflected in the drawing by the preliminary names remaining on the device, while the new names (without the *) are on the signal lines at the device.

Three DS3884A Handshake transceivers are used for the data synchronization, address synchronization and arbitration synchronization strobe signals. The additional channels on the handshake transceivers are used for control signals. The signals are divided between the 3 transceivers so the required signals will have the filtered receiver outputs. The DI* and DK* signals do not require filtering in Profile B, but are shown here on filtered channels to reflect the necessity of filtering these signals in a profile that does use Broadcast/Broadcall transactions. The remaining transceiver channels are distributed with consideration for the shortest possible stub length. The synchronization signals should be given primary consideration for shortest stubs due to the low skew required between strobe and address/data signals.

If the filtered receiver outputs of the DS3884A are not used, the REXT pin should be unconnected. For the same reason, the pulse width selection pins should be tied low. All unused driver inputs should be tied low to prevent oscillation. Unused receiver outputs need not be connected.

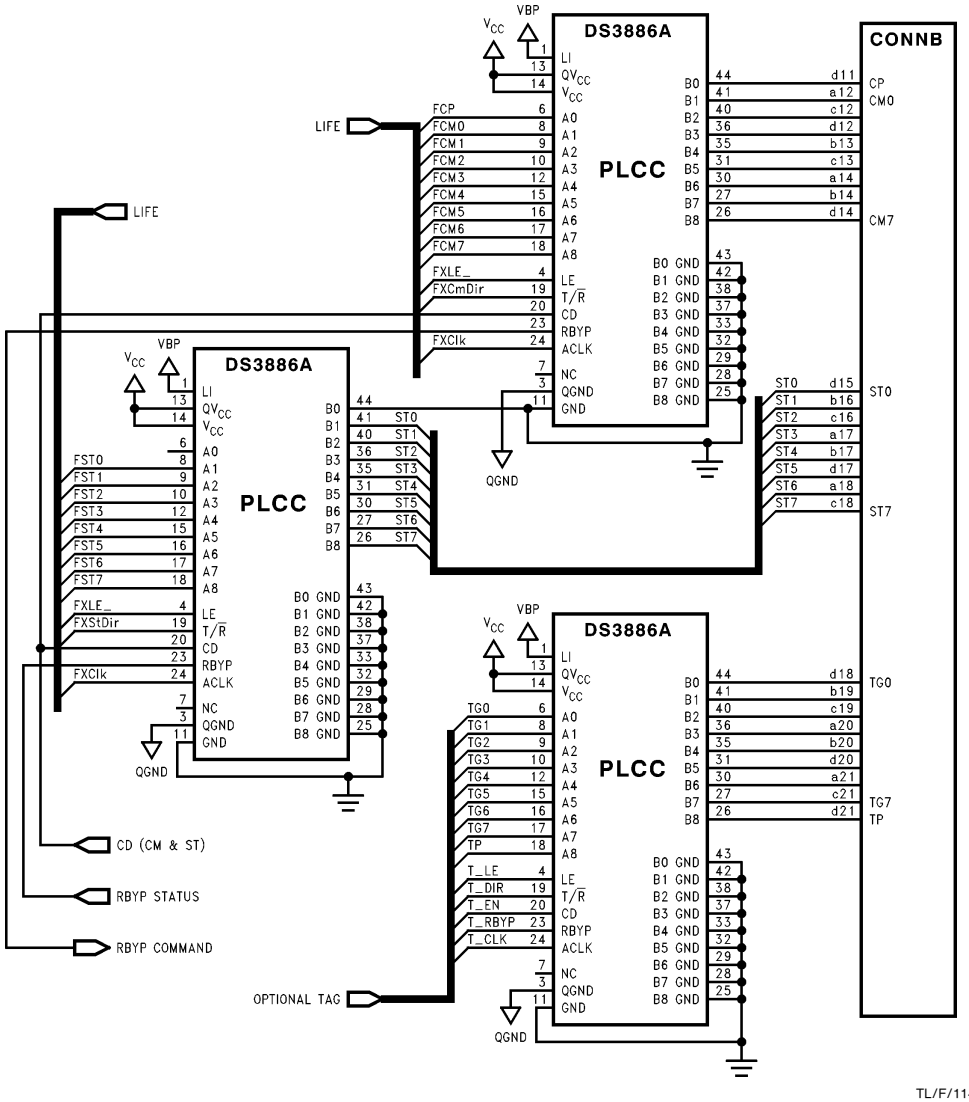

FIGURE 3. Command, Status and Optional Tag Byte Transceivers

The DS3886A Latched Data transceiver is used for the Command byte and the Status byte. The command and status signals are linked to the LIFE. The control lines for the transceivers are generated by the Protocol Controller. The Chip Disable pins are connected together for all transceivers. Chip Disable control then depends on live insertion level supported and user preference (a separate article will cover this topic). Register bypass control lines can be used as the system designer feels necessary. The optional tag byte transceiver is shown but it is completely system dependent as to the further implementation of this transceiver.

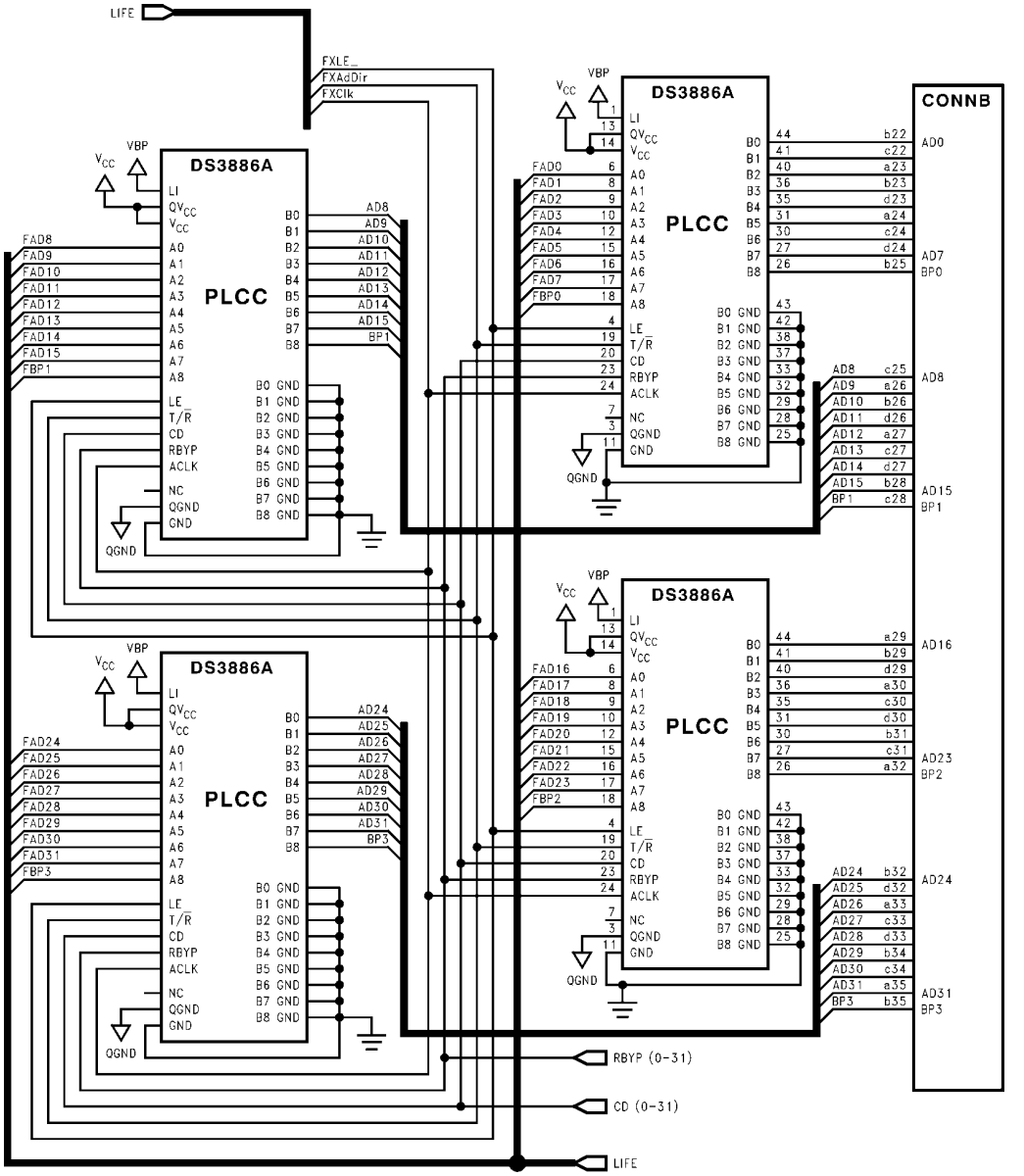

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FIGURE 4. Address and Data [0 . . . 63] Transceivers

The Address and Data Transceivers for all 8 bytes are shown. The ''A'' port and the control lines are connected to the LIFE.

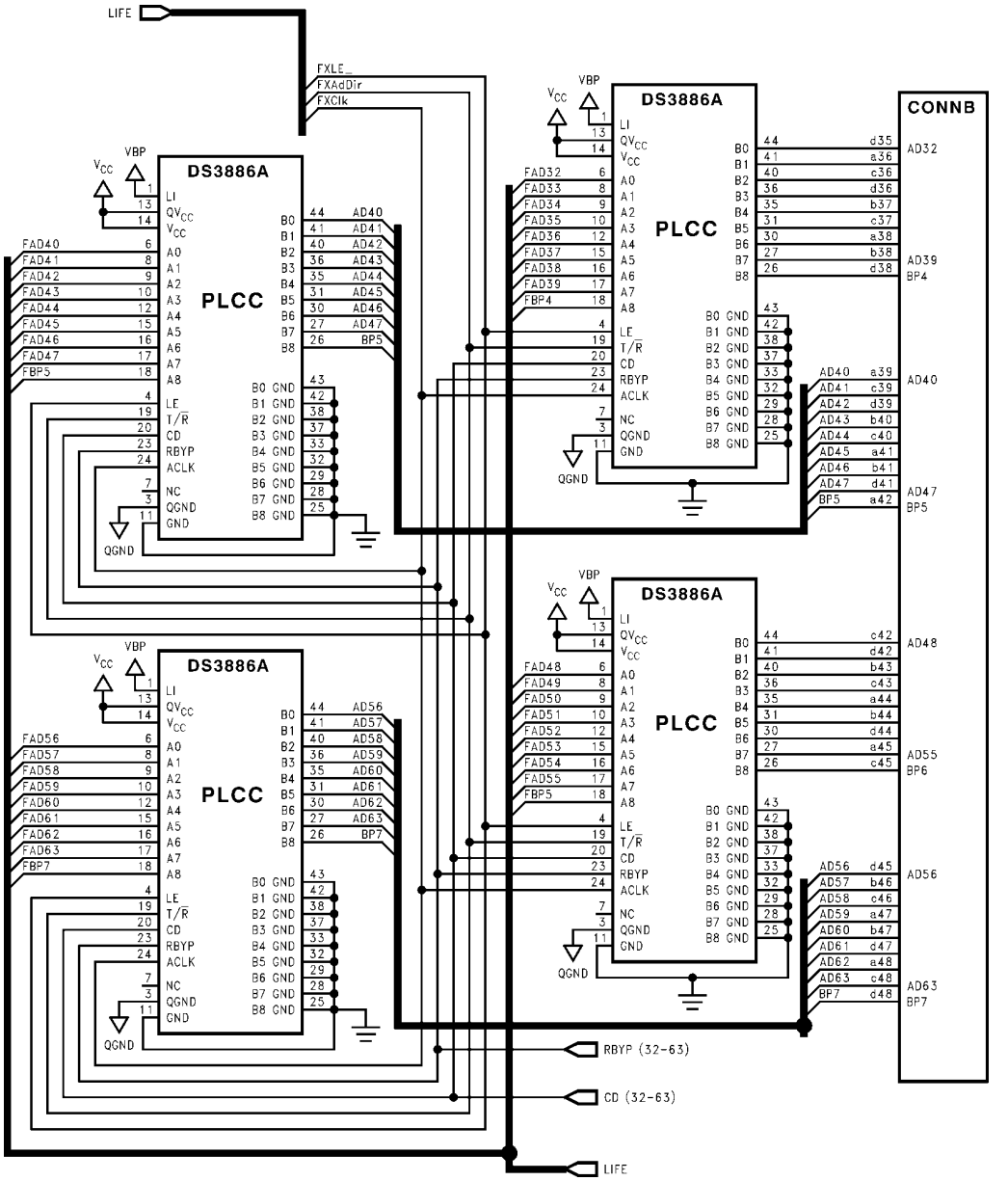

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FIGURE 5. Address and Data [32:63] Transceivers

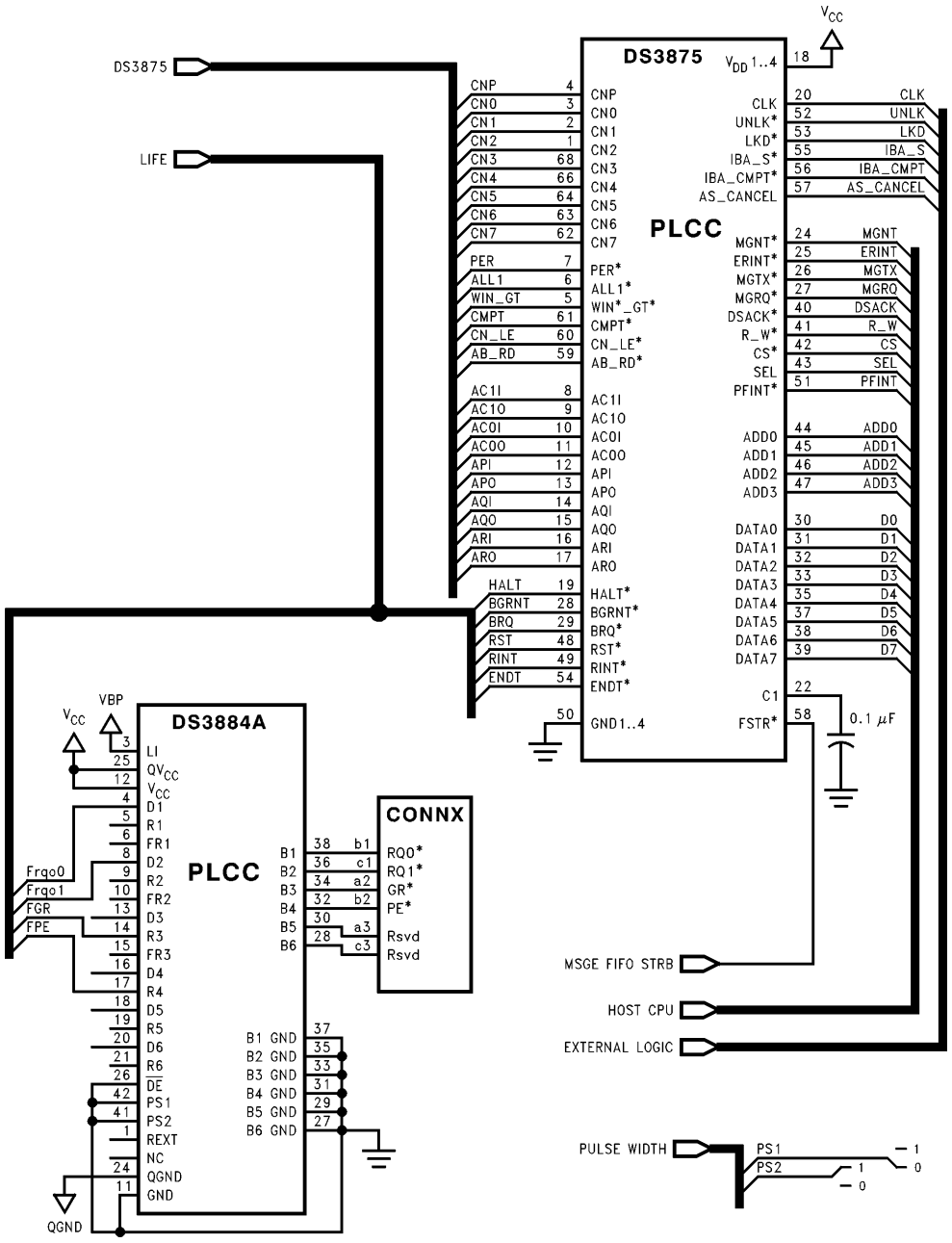

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FIGURE 6. Distributed ARB Controller, Central ARB, X Connector

One DS3875 Arbitration controller is included as an option for a distributed arbitration board. It will also be possible to use the Arbitration controller as the message handler in the central Arbitration board. The signals on the controller are broken into groups for ease of identification.

The fourth Handshake transceiver is used for the central arbitration signals at the X connector. A handshake transceiver is chosen because there are 2 input lines and 2 output lines on each board. The receivers of the DS3884A are always on and the driver enable pin is tied low. The other two channels can be connected to the reserved bus connectors since these signals are required to be bused by Profile B. Unused driver inputs should be tied low to prevent oscillation. Since the filtered receiver outputs are not used, the REXT pin should be unconnected to minimize power consumption. PS1 and PS2 should be tied low to prevent internal oscillations. These precautions should be followed whenever the filtered receiver outputs will not be used on a board (i.e., no support for broadcast/broadcall transactions).

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