Live Insertion with BTL Transceivers

National Semiconductor
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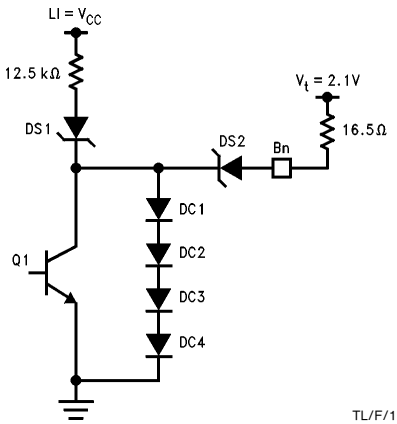
This paper investigates the possible glitches caused by inserting a board or module into a powered Futurebus+ backplane. The signal lines on the backplane will be in one of three states; high—when the bus is released, low—when the bus is asserted, and the transition state. In the transition state the bus will be going from a high to a low state or vice versa. The bus will spend the majority of the time in the high or low state. The glitch during live insertion will be investigated for the high and low state.

The LI (live insertion) pin on the Futurebus+ Transceivers helps minimize the loading on the bus during live insertion and after the board has been plugged into the backplane.



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When LI is connected to V_{CC} and the output is in the released state, the output Schottky diode (DS2) remains reversed biased thereby minimizing the output capacitance as shown below. Reducing the capacitance at the output will minimize bus loading.

The measurements were taken from a 10 slot backplane with 1″ slot to slot spacing. The lines were terminated with 39Ω resistors to 2.1V at each end. This is not a Profile A/B/F compliant Futurebus+ backplane. A standard backplane will have 30 mm (1¼″) slot to slot spacing, 14 slots and 33Ω terminations. The board was provided by Hybricon and uses the DS3884A Futurebus+ 6-bit transceiver offered by National Semiconductor. The live insertion glitch taken on this backplane will be similar if taken on a standard Futurebus+ backplane. The measurements were taken directly on the backplane (the rear side of the backplane was probed using a high impedance 2 GHz scope) unless otherwise specified.

The Futurebus+ backplane has two stages of contact. Stage one is when the power pins between the board and the backplane mate. Stage two is when the rest of the signal pins make contact. These two stages are implemented by having short signal pins and long power pins on the backplane. As the board is inserted into the backplane the backplane power pins (VBP and ground) make contact with the board sooner than the signal pins as shown on *Figure 1*. Stage two, when the signal pins make contact with the backplane, will be the subject of this paper.

Live insertion was tested using this basic set-up. Some of the testing done included a 1 MΩ pull-up or pull-down resistor to V_{CC} or ground, respectively.

Test done with device and connector excluding the board differs in that QV_{CC}, V_{CC} and $\overline{DE}$ were not connected to 5V.

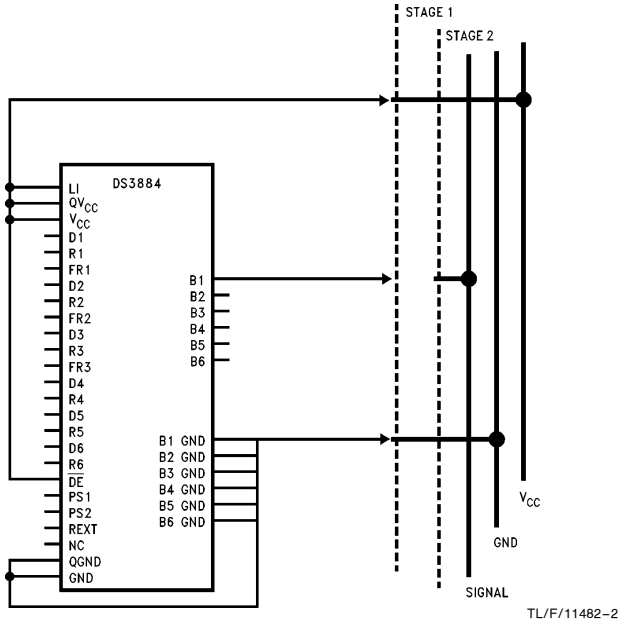

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FIGURE 1. Live Insertion Diagram

The waveforms shown on *Figures 2* to *7* are based on multiple board insertions. In each figure several waveforms are superimposed to show the various glitches observed. The waveforms shown were chosen from at least thirty that were taken for each case.

Case 1: All power pins connected—Prior to insertion all the power pins including LI and $\overline{DE}$ are connected together as shown on *Figure 1*. When the board was inserted into a backplane that was in a high state, the glitch had a maximum negative amplitude of 150 mV, as shown in *Figure 2*. The glitch reached an absolute minimum level of 1.94V. The noise margin below the glitch is about 320 mV. The noise margin is equal to the absolute minimum level minus V_{IH} min of the receiver which is 1.62V.

When the board was inserted into a backplane that was in a low state, no glitch was observed on the backplane as shown on *Figure 3*. The low state on the backplane is accomplished by having another board pull the bus low.

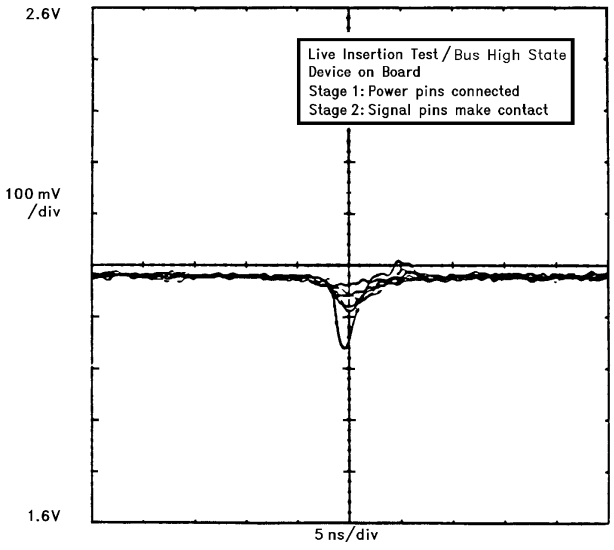

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FIGURE 2

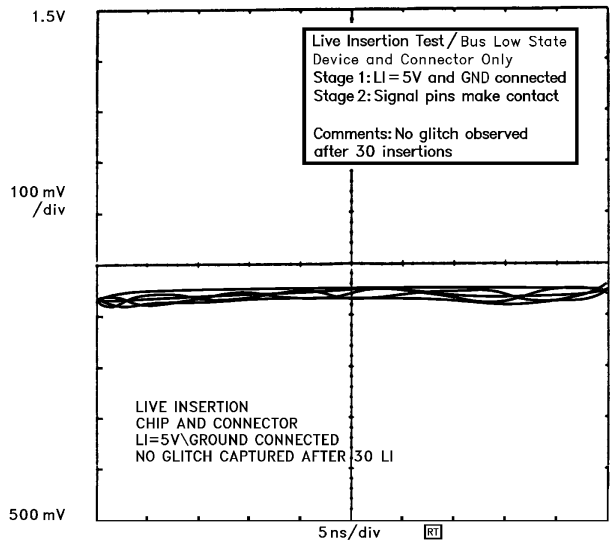

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FIGURE 3

Case 2: Live insertion pin connected—Prior to insertion. LI is connected to the power pins. LV_{CC}, QV_{CC} and $\overline{DE}$ are left floating. The device was directly soldered on a connector since the board was not re-configurable for this set-up. As shown on *Figures 4* and *5*, no glitch was observed when the backplane was high or low prior to insertion.

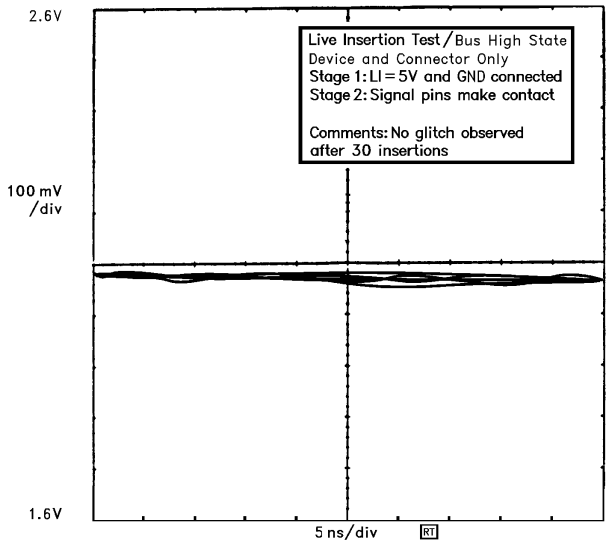

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FIGURE 4

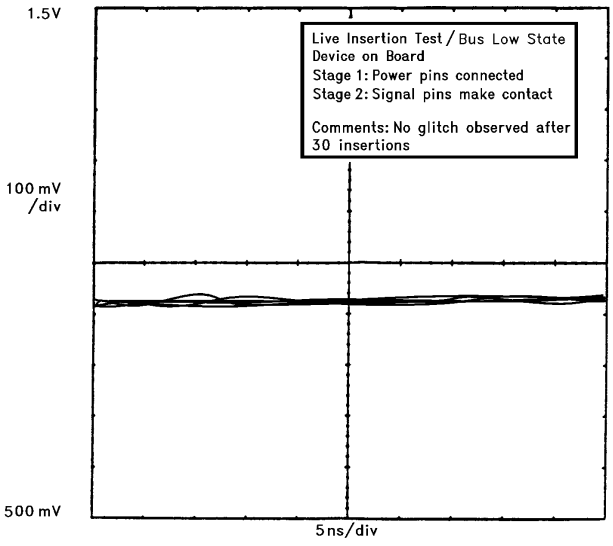

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FIGURE 5

Case 3: Live insertion pin connected to V_{CC} and B port has a 1 MΩ pull-up to V_{CC}. Case three was performed to insure that the test methodology in case two was correct. To intentionally cause a glitch during insertion, a 1 MΩ pull-up resistor was used to bias the output to V_{CC} before inserting the device into a backplane. The backplane was in a low state prior to insertion. The maximum amplitude of the glitch was 1240 mV as shown in *Figure 6*. The noise margin above the glitch was 230 mV where noise margin is equal to V_{IL} of the receiver (V_{IL} max = 1.47V) minus maximum amplitude.

Case 4: Live insertion pin connected to V_{CC} and B port has a 1 MΩ pull-down to ground. Case four was performed to insure that the test methodology in case two was correct. To intentionally cause a glitch during insertion, a 1 MΩ resistor was used to bias the output to ground before inserting the device into a backplane. The backplane was in a high state prior to insertion. The glitch reached a minimum level of 1.925V which was 325 mV away from V_{IH} of the receiver (V_{IH} min = 1.62V) as shown on *Figure 7*.

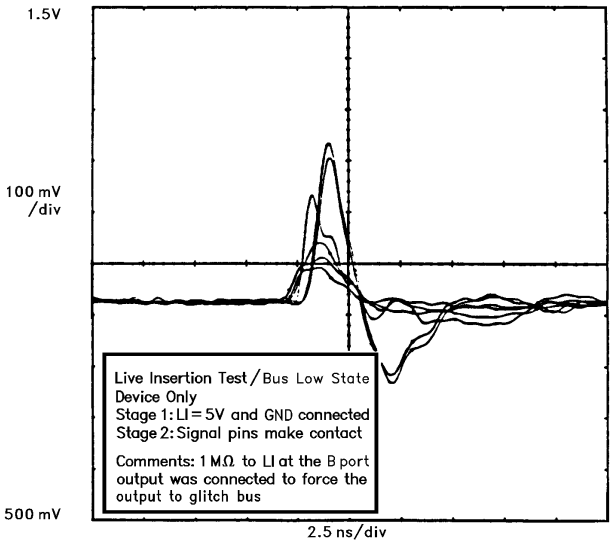

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FIGURE 6

SUMMARY

The live insertion pin LI for the Futurebus+ transceiver was designed so that the outputs could be reverse biased during live insertion prior to powering up the whole board. Reverse biasing the outputs will present minimum loading to the bus. Results showed that when LI was pulled up to V_{CC}, with QV_{CC} and LV_{CC} floating, prior to insertion no glitch was observed on the backplane. When all power pins (V_{CC}, LI, QV_{CC}) and driver enable ($\overline{DE}$) were connected to V_{CC} prior to insertion, the glitch never crossed threshold. This does not prove that there is no chance of a Live insertion glitch that may cross the threshold, but it does indicate the nature of that possible glitch. The investigations show that the glitch peak amplitude will be of short duration if it should cross the receiver threshold from either direction. If that should be the case, then National's BTL/Futurebus+ transceivers have a natural glitch rejection specified at 1 ns typical, in case a live insertion signal does cross threshold.

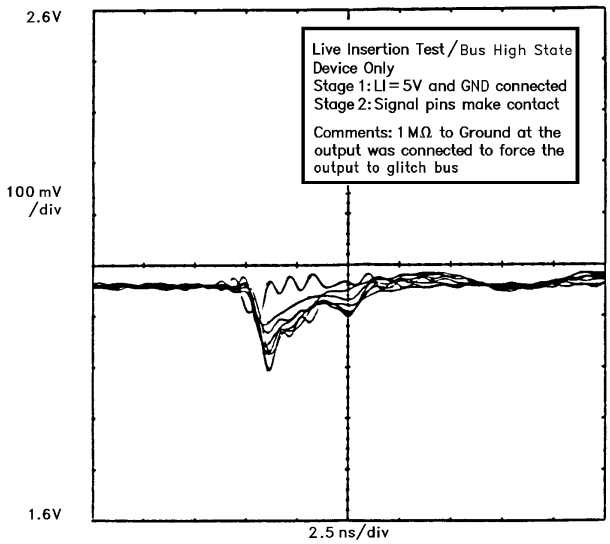

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FIGURE 7

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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