P1149.1A Extensions to IEEE-STD-1149.1-1990

National Semiconductor
Application Note 890
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1.0 ABSTRACT

Since publication of IEEE-1149.1-1990/ANSI[1, 2, 3], proposals for extensions and requests for clarifications have been considered by the IEEE 1149.1 Working Group. The original standard established a common, industry-wide methodology for the application of scan test access. Its rapid acceptance and use by semiconductor designers, by test engineers and by systems developers resulted in questions needing interpretation. Several additional optional instructions were proposed including two that were accepted: CLAMP and HIGHZ. The need for harmonious test integration with existing and proposed scan methodologies resulted in acceptance of a proposal for the subservience of 1149.1's Test Access Port (TAP) by a higher level static controller. (At the time that this was written IEEE had not yet approved P1149.1a.)

2.0 FEATURES OF THE ORIGINAL 1149.1

IEEE STD-1149.1/1990 resulted when the users of proprietary scan methods realized that no organization could afford to fully support its own scan technology. The growing use of standard product ICs to implement new systems, meant that the semiconductor industry could not support many proprietary scan access methods. Over a dozen different commercial scan methods were in use in 1985 when the European-originated Joint Test Action Group (JTAG) began the search for a common standard. This effort evolved into the IEEE sponsored 1149.1.

IEEE 1149.1 defines a dedicated 4-pin test access port with an optional fifth pin defined to disable the test logic. *Figure 1* shows its basic architecture. Test patterns are shifted into an IC using Test Data Input (TDI). Simultaneously, the most recent test results can be shifted out using Test Data Output (TDO). A Test Clock (TCK) synchronizes the test logic. Test logic control is provided by Test Mode Select (TMS) which sequences a 16-state finite state machine (FSM) in each IC.

The test logic in each IC has two major functions: the first to provide a protocol controlled interface between the component and the 1149.1 tester. This function is provided by the Test Access Port (TAP) Controller. Within the TAP controller is an instruction register that may be loaded from the TDI input. An instruction provides flexibility in test that is, in many cases, limited only by the designers imagination. The second function of the test logic is to provide scan accessible paths to I/O pins using the cells of the boundary-scan register but it also provides access to as many optional internal scan registers as the designer chooses to add.

IEEE 1149.1 defines three mandatory instructions and four optional ones. The most common application of 1149.1 has been to verify interconnections and to detect process defects in those interconnections. The three mandatory instructions support this application. The first instruction, SAMPLE/PRELOAD, can be used to preload a test pattern into a scan register. It can sample the system logic state on its system inputs. The sample capability places strict skew requirements between the test clock and the system clock. If these requirements are not met, then only the preload feature will be usable.

The second instruction, EXTEST, forces preloaded test vectors, or subsequent vectors onto an IC's output pins on the falling edge of one TCK edge. After waiting two and one-half TCK clocks, allowing the results to settle, EXTEST captures the results present on its system inputs into the boundary-scan cells. A series of EXTEST vectors is used to isolate interconnection defects. The third mandatory instruction, BYPASS, simply connects TDI to TDO with a one bit shift register called the Bypass register. When testing a cluster of other ICs on a module, test time may be reduced by placing an IC in Bypass mode. And, during normal system operation, that is during Test Logic Reset state, the bypass register may be connected between TDI and TDO.

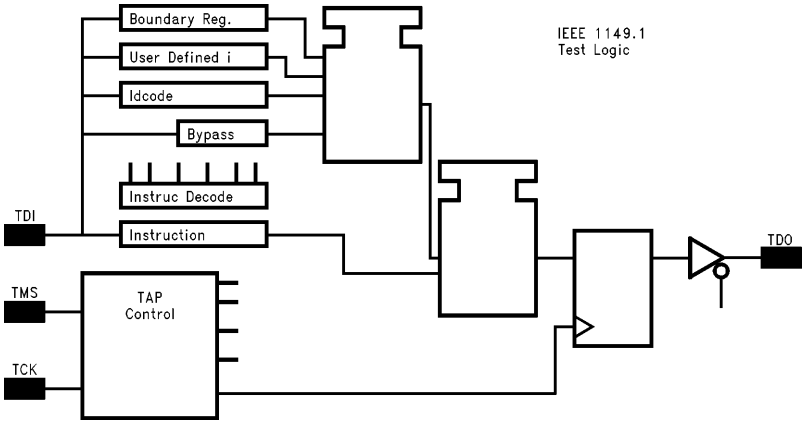

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FIGURE 1. Architecture—IEEE Standard Test Access Port and Boundary-Scan

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Additional, optional instructions were defined in 1149.1 to encourage a common test methodology by those who wanted to gain more benefit from the use of the standard. These optional instructions are IDCODE, USERCODE, INTEST and RUNBIST. IDCODE connects a read-only, 32-bit idcode register between TDI and TDO. The contents of the idcode register allow a test program to determine an IC's function, manufacturer and design revision. A similar function is provided by the field programmable USERCODE which is used to identify field programmed components.

INTEST is a companion to EXTEST but it was defined, not to test external interconnections, but to allow the boundary-scan register test patterns to be applied to test an ICs internal logic. INTEST has not always been included in the simpler ICs such as logic buffers because there is very little to test. And, at the upper end of the complexity spectrum INTEST has not been successful. The most complex ICs often have either high speed serial inputs or critical timing requirements which can not be met using a simple, static boundary register. The limitations of INTEST have resulted in increased interest in the final optional instruction, RUNBIST, which provides a standard method for concurrent testing of several ICs using their own internal self test features.

Additional user-defined commands are supported within the original 1149.1. When those commands might cause damage to a component, the designer is required to specify the hazardous instruction register codes. User-defined instructions provide not only a flexible application environment, but also a mechanism for defining and testing future extensions.

3.0 NEW OPTIONAL COMMANDS DEFINED IN 1149.1a

Among the user-defined commands, two have been added to 1149.1a. Both are simple to implement and widely used. They are CLAMP and HIGHZ. Recall that IEEE 1149.1 provides an electronic access replacement for bed-of-nails (BON) test access. During BON testing there may be large sets of test vectors which require that many printed wiring board (PWB) nets are held at constant logic states. When applying test vectors to a cluster of logic on a PWB using 1149.1 it was necessary to repeatedly reload the same pattern into some ICs. They might have been used to simply hold open data paths through which dynamically changing vectors would pass. They simply hold guarding levels. CLAMP and HIGHZ, the new instructions support the emulation of this kind of static test behavior. They speed test vector transmission by reducing the total number of scan cells in the module's scan ring.

To execute the CLAMP instruction a test pattern is shifted into the boundary-scan register and transferred to the update register. Because this pattern is not expected to change while the outputs of other ICs are delivering test vectors to other logic, the CLAMP instruction holds this vector, forces its value onto the system logic output pins and inserts its Bypass register as the path between TDI and TDO. Thus only a one-bit delay results. Other components that are, for example, executing the EXTEST instruction will behave as before but will be accessed more rapidly because some ICs are simply bypassed. Thus the active ICs will allow each test vector to be shifted through the boundary-scan register and delivered to their outputs during the Update__DR state. The results of the test will be captured during Capture__DR. However, the ICs executing CLAMP will not participate in the test. They will simply pass the test data through a one-bit delay.

CLAMP does not add significant new capability to 1149.1. Before CLAMP was included, the same tests could be performed. They just took longer as it was necessary to constantly reload the same test vectors into the components that were not actively involved in a test, but were being updated as a consequence of being in the same scan ring.

The other newly defined optional instruction, HIGHZ, serves to place all system outputs of an IC in a high impedance state. HIGHZ, like CLAMP, improves test efficiency. Once the HIGHZ instruction is loaded during the Update__IR state, like the CLAMP instruction, the Bypass register will be connected between TDI and TDO. The component will remain in this state until another instruction is loaded, or the test logic is reset. Again, other IC's might be delivering a series of INTEST or EXTEST vectors while all ICs executing the HIGHZ instruction are kept in a quiescent high impedance drive state.

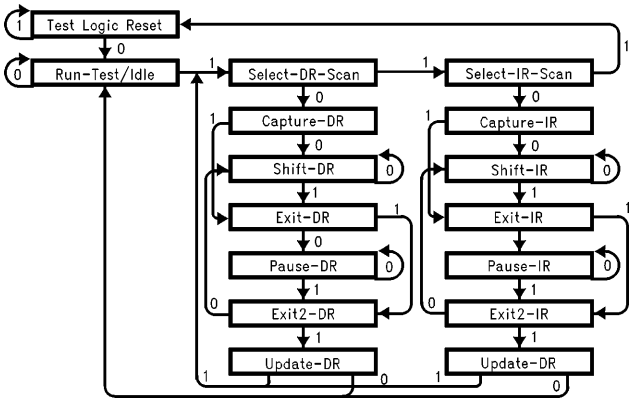

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FIGURE 2. TAP Controller State Diagram

HIGHZ also allows JTAG-compliant ICs to be safely removed from possible bus conflict during BON testing. Because all digital ICs do not yet support IEEE 1149.1, BON testers will continue to be used. In addition, analog and mixed signal ICs may require BON access to make analog in-circuit measurements. While such tests are being run HIGHZ can help isolate nets that are being driven by the BON tester. It should be noted that HIGHZ can be implemented in an IC that does not have a system logic high impedance control input pin.

4.0 SUBSERVIENCE OF 1149.1 TO HIGHER-LEVEL CONTROL

When 1149.1 was written, some assumed that 1149.1 would be the only scan test methodology needed. Some thought that it would provide all the test access needed for detecting digital interconnection faults and that other test methodologies would disappear. However, 1149.1 was written by users of a wide variety of proprietary scan methodologies. And while 1149.1 has gained support and commercial ICs almost exclusively support 1149.1, there remain within the founding organizations many preexisting test tools including software, testers and components. One of the best known is Level Sensitive Scan Design (LSSD) developed within IBM. These preexisting scan methods must at least coexist with 1149.1 until a conversion to the new standard is complete. This coexistence creates a need to define how a component might support both 1149.1 and another scan methodology.

IEEE 1149.1 may also need to coexist with some newer standards that are being defined by other IEEE Working Groups. The P1149.2 Working Group is defining a standard which is intended to allow lower cost ASIC testing than its advocates believe is possible using IEEE 1149.1. P1149.2 does not have a TAP interface. And the P1149.4 Working Group is defining a test framework for mixed-signal and analog ICs. The P1149.4 Working Group has stated that it will include a TAP as part of its test methodology, but it is expected to add analog test pins. The issue of the integration of 1149.1 with these and other, as yet undefined, IEEE standard test access methods has been addressed within 1149.1a.

Supporters of these other scan test methods have proposed a mechanism wherein a component might at one moment behave in a manner that conforms to 1149.1 and at a later moment it might not conform to 1149.1 but would meet the requirements of some other protocol. In each of these cases there is an assumed test master which can control components using 1149.1 or one of the other access methodologies. A simple mechanism is described in 1149.1a for converting a component from conformance to one standard to conformance to a different standard. One or more, static, non-sequential, control inputs on an 1149.1a-compliant IC may be used to turn off the TAP and enable another test methodology. It is permitted to simply convert the TAP pins into the function needed to support the other standard. Alternatively, a second test access port may be used. The input pins that convert a component from one protocol to another do not have boundary-scan cells.

5.0 CLARIFICATIONS TO 1149.1 WITHIN 1149.1a

The wide acceptance of 1149.1 has led to many questions for interpretation about the exact intent of the standard for applications that were not detailed in 1990. For example, field programmable logic and gate array master chips were not exhaustively defined in the original standard. This has resulted in some requests for clarification. Many clarifications were simply related to editorial clarity.

5.1 The Independence of System Logic and Test Logic

1149.1 defines dedicated test logic. It defines test methods that are not restricted by the features of a component's system logic. This independence means that test automation can be applied without understanding system logic. Prior to 1149.1 lengthy functional tests based upon a detailed understanding of the system logic were often used to test interconnections. 1149.1 was written to support automation for PWB and system interconnect test program generation without the need to understand how each IC functioned.

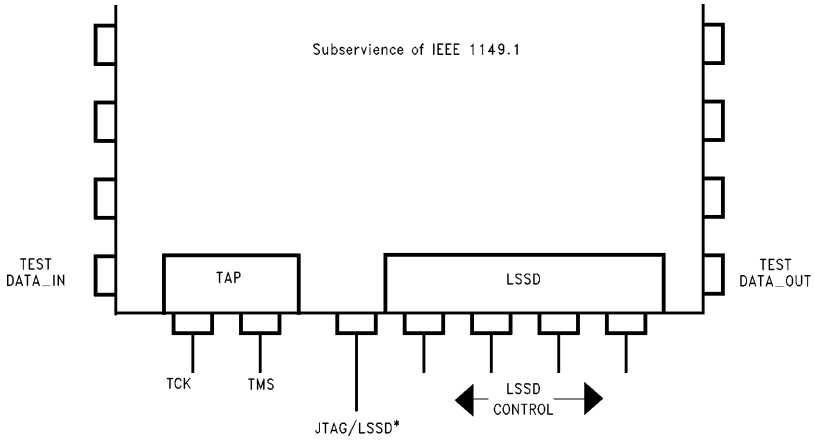

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FIGURE 3. A Possible Use and Configuration of a New Feature Defined in 1149.1a that Permits a TAP Controller to be Disabled while Another Scan Protocol, in this Case LSSD, is Activated

That is, the goal was to create board interconnect tests entirely from a description of the boundary-scan (B/S) cells and supporting test logic. Both HP and Teradyne have reported reducing the time needed to develop interconnection tests from six months to a few hours. A possibility because only a description of the structure of the test logic was needed to automatically create the tests.

A simple example wherein a knowledge of the system logic might be required if the test and system logic were not isolated can be shown with a bidirectional transceiver. During normal operation only one of the two output directions can be active at one time. Within the domain of 1149.1, however, both ports must be able to become active simultaneously. If the system logic that controls which port is active were not overridden by the test logic, then test software would need to be written around this restriction. Only knowledge of the component will reveal that only one port can be active at a time. In a more complex IC the relationship between different output buses is often more complex. Test programs are more easily written if outputs can be forced independently of mission function. This confusion has been clarified in 1149.1a.

A related test freedom is the need to control and to change all test outputs during each test cycle. Test pattern sequences must not be restricted based upon the normal operating characteristics of IC. This means that a test program must be free to drive all outputs of an IC to any arbitrary state from any other arbitrary state following one TCK clock edge. In many cases, this can create more crosstalk, ground bounce, and other noise during test than could be generated during normal operation. It also means that more current may flow into the power supply during test. To reduce noise from simultaneous switching, 1149.1a recommends adding small delays in the logic that updates the output registers during test mode. This will skew the time when each set of outputs switches which can reduce simultaneous switching noise.

5.2 Clarifications for Field Programmable Logic

Programmable logic is more common and more complex than when 1149.1 was written. In-system reprogrammable logic creates opportunity for system designers and it allows for interesting applications but it can complicate the already difficult test challenge. Field programmable logic allows system architectures to be changed after field installation. 1149.1a requires that this shall have no impact on the component's test logic. The basic test features of 1149.1 must be defined at the time the component is manufactured and they must not be reprogrammable after being embedded in a system. For example, if the test logic is programmed into a component by a user, then the manufacturer of that component can not claim conformance because there is no test logic when the component is built and a novice user could program non-conforming test logic. The test logic in a JTAG-compliant field programmable IC must be permanently defined and non-alterable in the field.

5.3 ASIC Master I/O Cell Clarifications

Mask programmable ICs may be provisioned with three boundary-scan cells per pin which would be adequate to implement bidirectional data flow on every pin. However, in a typical application many of the pins may be inputs and only requlre one of the three cells that are provided. Automated layout software might produce ICs with many of the unused boundary-scan cells connected in the scan ring. 1149.1a permits these redundant cells. They may be left in the boundary-scan register provided that their value is undefined and that test results are not impacted by the content of such cells.

Two Enable B/S Cells

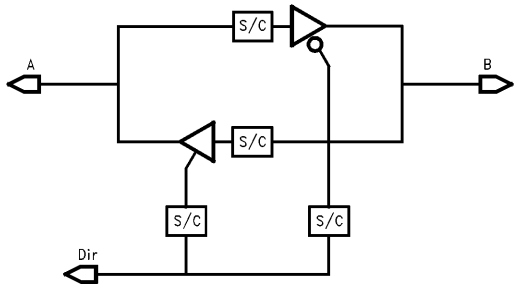

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FIGURE 4. Although in system mode, this transceiver can only drive in one direction, in test mode each output must have independent control. This is clarified in 1149.1a.

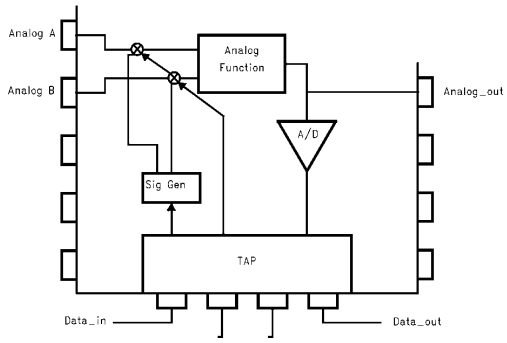

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FIGURE 5. Mixed-signal analog test has become one of the most exciting applications of the IEEE test access port. The P1149.4 working group is defining a standard method for its application.

5.4 Other Clarifications

A variety of other clarifications are included in 1149.1a. While most were made to minimize the possibility of confusion, some of the clarifications may be worth noting.

When testing is complete and a component is returned to normal operation, it is desirable for all components to return to normal operation at the same time. This will, for example, minimize the risk of bus contention. The TAP controller enters Test-Logic-Reset on the rising edge of TCK if the state machine is in the Select-IR state and if TMS is high on the rising edge of TCK. There are several times within Test-Logic-Reset when the IC might be returned to normal mode. This could occur asynchronously upon entry into the Test-Logic-Reset state as indeed it does if TRST* is asserted. But a requirement of 1149.1 is for all outputs to change on the falling edge of TCK. 1149.1a clarifies the return to normal mode by specifying that the component returns to normal operation on the first falling edge of TCK after entry to Test-Logic-Reset.

Following the execution of EXTEST, INTEST or RUNBIST, the state of the internal system logic was not clearly defined in 1149.1. The supplement specifies that the state of system registers will be indeterminate following these tests. A similar clarification is included to define the state of system output pins during INTEST and RUNBIST. Outputs must be determined solely by the contents of the boundary-scan register, not by the results of internal testing.

1149.1 permits stimulus to be applied during test mode that could not exist during normal operation. Although component damage may be unlikely, only the designer can protect a component from damage if potentially hazardous stimulus is applied. Therefore, 1149.1a assigns this responsibility to the component designer. The designer may choose to simply block external signals from being applied to internal logic or ''safe'' values may be forced instead.

If an IC has no system pins, as in the case of a JTAG-accessed memory or perhaps a JTAG-accessed temperature sensing component, then there is no need for boundary-scan cells. However, at least one bit is needed to resynchronize data shifting through a component. 1149.1a specifies that a cell shall be inserted between TDI and TDO and that it may be the Bypass register.

6.0 FUTURE ENHANCEMENTS TO SUPPORT BOUNDARY-SCAN

The popularity of 1149.1 has resulted in proposals for several new supporting computer languages including Boundary-Scan Description Language (BSDL)[4]. BSDL was first proposed at ITC 1990. Its wide use has made it a de facto standard. BSDL describes how the 1149.1 features within an IC are implemented. By reading the BSDL file for each IC and by reading a PWB netlist such as EDIF[5], commercial software tools are able to produce PWB test programs. It is likely that BSDL will become a part of the next revision, IEEE 1149.1b, within the next two years.

And too, hierarchical JTAG may soon be defined by the P1149.5[6] Working Group which has sent its draft to IEEE ballot. P1149.5 defines a fault tolerant, multidrop, addressable backplane bus. It was an outgrowth of the TM bus defined during the VHSIC program. Proposals have been presented to the P1149.5 Working Group for standard methods for interfacing 1149.1 to P1149.5.

Note: The opinions expressed in this paper are the personal opinions of the author and do not necessarily reflect those of the IEEE or the 1149.1 Working Group. At the time this was written, the proposed supplement 1149.1a had not been approved by the IEEE.

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John Andrews, a principal staff engineer at National Semiconductor, is a member of the IEEE 1149.1 and P1149.5 Working Groups. He has been granted six patents of IC designs. When not inspecting Maine's wilderness, he may be reached by e-mail at j.andrews@ieee.org.

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