Interfacing the PCM16C02 with Serial EEPROMs

National Semiconductor
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- EEPROM Programming Methodologies
- CIS Data Security

Note: This application note uses the following notation convention: hexadecimal numbers are represented with the prefix ''0x''; numbers with no prefix are decimal.

OVERVIEW

The PCMCIA's PC Card Standard requires, for basic compatibility, that each PC Card contain a small Card Information Structure (CIS), which starts at offset 0 of the card's Attribute Memory space. At a minimum, this structure contains basic information about the card's capabilities and capacities (size, speed, etc.). Ideally, this CIS data should be stored in non-volatile memory to prevent corruption. Other critical information, for example an Ethernet node ID on a LAN card, might also be stored in non-volatile memory on the card. Security of this sort of data is of highest importance; any corruption of this data may render the card useless. However, field-programmability of the CIS and other configuration data must be considered.

The PCM16C02 interfaces directly to 2k byte serial EEPROMs (16k bits), which conform to the MICROWIRE™ protocol. An example of this device is the National Semiconductor NM93C86 16k bit MICROWIRE serial EEPROM. The PCM16C02 includes all the necessary pins to interface cleanly to this device.

PCM16C02 ARCHITECTURE

The PCM16C02 contains 1k bytes of SRAM which ''shadows'' the lower 1k byte of data stored in the 2k byte serial EEPROM. The upper 1k bytes of EEPROM memory are not used by the PCM16C02. Because 1k byte EEPROMs are not commonly available on the market, the larger 2k byte EEPROM was chosen. At card insertion, or after a system reset, the PCM16C02 will automatically load the contents of the serial EEPROM into its internal SRAM. The use of fast internal SRAM minimizes system latency for attribute memory accesses. The PCM16C02 also has the ability to write the data stored in its internal SRAM and specific registers (in Attribute Memory locations 0x000 through 0x7FE, on even-byte boundaries) back to the EEPROM. This allows card manufacturers to ''burn'' the CIS into their cards after assembly and to accommodate CIS upgrades for the end user.

The Attribute Memory space in the PCM16C02 is broken down into five segments: the range from 0x0000 through 0x03E2 is SRAM which is intended for CIS storage. The range from 0x03E4 through 0x03FE is intended for PCM16C02 specific registers (only 0x3E4 through 0x3FC are implemented in PCM16C02, 0x3EC, 0x3EE, 0x3F2, 0x3F4 and 0x3FE are reserved for future use—''RFU''). These two segments cover 512 bytes. The third segment of Attribute Memory is 0.5 kbytes of SRAM from 0x0400 through 0x07FE. The fourth segment of the Attribute Memory space includes the PCM16C02-specific ID and EEPROM Control Registers and several RFU registers located from 0x1000 through 0x101E. The fifth segment includes all of the PC Card Standard compliant Configuration Registers in locations 0x1020 through 0x105E. Refer to Table I for a detailed Attribute Memory map of the PCM16C02, and to the PCM16C02 datasheet for register specifics.

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TABLE I. PCM16C02 Attribute Memory Map

Register Description	Register Type	Address (Hex)	Stored in EEPROM
Card Information Structure	**PC-Card CIS**	**0x000–0x03E2**	**Yes**
Pin Polarity Register	PCM16C02 Specific	0x03E4	Yes
PMGR and Clock Register	PCM16C02 Specific	0x03E6	Yes
CTERM 0 Register	PCM16C02 Specific	0x03E8	Yes
CTERM 1 Register	PCM16C02 Specific	0x03EA	Yes
Reserved for Future Use Registers	PCM16C02 Specific	0x03EC–0x03EE	Yes
Miscellaneous Register	PCM16C02 Specific	0x03F0	Yes
Reserved for Future Use Registers	PCM16C02 Specific	0x03F2–0x03F4	Yes
Wait State Timer Register	PCM16C02 Specific	0x03F6	Yes
NAND Flash (NM29N16) Config Register	PCM16C02 Specific	0x03F8	Yes
Host-Side DMA Register	PCM16C02 Specific	0x03FA	Yes
Watchdog Timer Register	PCM16C02 Specific	0x03FC	Yes
Reserved for Future Use Registers	PCM16C02 Specific	0x03FE	Yes
Card Information Structure	**PC-Card CIS**	**0x0400–0x07FE**	**Optional**
ID Register	PCM16C02 Specific	0x1000	No
EEPROM Control Register	PCM16C02 Specific	0x1002	No
EEPROM Security Register	PCM16C02 Specific	0x1004	No
Reserved for Future Use Registers	PCM16C02 Specific	0x1006–0x101E	No
Function 0 Configuration Option Register	PC-Card	0x1020	No
Function 0 Configuration Status Register	PC-Card	0x1022	No
Function 0 Pin Replacement Register	PC-Card	0x1024	No
Unused	PC-Card	0x1026	No
Function 0 I/O Event Register	PC-Card	0x1028	No
Function 0 Base A Register	PC-Card Extension	0x102A	No
Function 0 Base B Register	PC-Card Extension	0x102C	No
Unused	PC-Card Extension	0x102E–0x1030	No
Function 0 Limit Register	PC-Card Extension	0x1032	No
Reserved for Future Use Registers	PC-Card Extension	0x1034–0x103E	No
Function 1 Configuration Option Register	PC-Card	0x1040	No
Function 1 Configuration Status Register	PC-Card	0x1042	No
Function 1 Pin Replacement Register	PC-Card	0x1044	No
Unused	PC-Card	0x1046	No
Function 1 I/O Event Register	PC-Card	0x1048	No
Function 1 Base A Register	PC-Card Extension	0x104A	No
Function 1 Base B Register	PC-Card Extension	0x104C	No
Unused	PC-Card Extension	0x104E–0x1050	No
Function 1 Limit Register	PC-Card Extension	0x1052	No
Reserved for Future Use Registers	PC-Card Extension	0x1054–0x105E	No

In a card design using the 2k byte EEPROM, the first three segments of Attribute Memory will be stored in non-volatile memory upon an EEPROM write event. The other segments, including EEPROM Control Register and PC Card Configuration Registers are dynamically configured by the host after card insertion and interpretation of the CIS data by Card Services.

The PCM16C02's internal SRAM is organized as 8 bits on even byte boundaries only. This conforms to the PC Card Standard. Because the EEPROM is organized as 16 bits, the PCM16C02 stores data in the SRAM in low/high format in consecutive byte locations. For example, the low byte at word 0 of the EEPROM will be shadowed in Attribute location 0x0000 and the high byte will be shadowed at location 0x0002. The low byte at word 1 of the EEPROM will be shadowed at Attribute location 0x0004, and the high byte at 0x0006, etc. The PCM16C02's EEPROM interface circuit handles all of this data steering automatically. The PCM16C02 EEPROM controller automatically halts the read process after successfully reading byte 1023 (i.e., lower 1k bytes). Although the physical SRAM space used is the same size as the EEPROM space, the Attribute Memory space is double the size of the EEPROM. Odd-address accesses to Attribute Memory (HADDR(0) = 1) are invalid.

The PCM16C02 supports the following serial op-code instructions for the 93C series MICROWIRE EEPROM series: READ, WRITE, EWEN (Erase/Write ENable) and EWDS (Erase/Write DiSable). Since the 93C series of EEPROMs do not require a memory location to be erased before being written, the ERASE command is not supported. The ERAL (ERase ALL) and WRAL (WRite ALL) commands are also not used by the PCM16C02. EEPROM read sequences are initiated by a system reset (i.e., a valid high on the PCM16C02 RESET pin) or setting the ReadEEPROM bit in the PCM16C02's EEPROM Control Register located at offset 0x1002. EEPROM write sequences can only be initiated by executing the required EEPROM write security sequence. (See details below)

Since EEDI is multiplexed with EEDO on the PCM16C02, the DI and DO pins on the National NM93C86 EEPROM can be tied together, however, it is recommended that a resistor be placed between pins DI and DO on the serial EEPROM to reduce noise. (Refer to NSC Memory Databook, APPS Note AN-758, *Figure 6* .)

EEPROM PROGRAMMING METHODOLOGIES

The most efficient way to program the EEPROM is to use the PCM16C02 to write the EEPROM after the card is assembled. This is done by writing the CIS data to the SRAM and configuring the PCM16C02 Specific Registers (0x03E4 through 0x03FC) and then initiating an EEPROM write by writing the proper security sequence. This methodology allows the CIS to be written on the card during the normal single-insert card test phase.

An EEPROM write sequence may only be initiated when the PCM16C02 is configured as a memory-only interface, i.e., when neither ConfFunc bit is set in the Configuration Option Registers at offsets 0x1020 and 0x1040. When configured for memory-only interface, the PC Card signal IREQ is defined as RDY/BSY. The PCM16C02 will force the RDY/BSY signal low while the EEPROM is being written. The host cannot access the card while RDY/BSY is low. Most serial EEPROMs specify a maximum write cycle time of 1 ms to 10 ms per byte. For the 2k byte serial EEPROM, the total time needed to write the lower 1k bytes of the EEPROM could theoretically reach 10 seconds. In a lab setting at NSC, write times of 2 to 3 seconds were measured for the NM93C86 16k bit EEPROM in 16-bit organization mode. The EEPROM write sequence should rarely, if ever, be used by the end user.

The EEPROM could also be programmed externally, prior to assembly of the card. This requires standard EEPROM burning hardware, and requires an extra production step as compared to programming the EEPROM on the card.

CIS DATA SECURITY

At power-up, after a system reset, or at the completion of a write sequence, the PCM16C02's EEPROM controller automatically sends an EWDS (Erase/Write Disable) instruction to the EEPROM. This ensures that data stored on the EEPROM will not be destroyed during power transitions due to uncontrolled interface signals or noise on power supply lines. National Semiconductor serial EEPROMs power up in the Program Disable Mode[1]. The PCM16C02 will only generate an EWEN (Erase/Write enable) instruction when the following EEPROM Write sequence has been written to the following registers:

EEPROM Write Security Sequence

Register	Address	Data
EEPROM Control Register	0x1002	0x2E
EEPROM Security Register	0x1004	0xB7
EEPROM Control Register	0x1002	0x91

Failure to execute the exact sequence listed above will disable EEPROM writes and will require the full enabling sequence to be re-initiated before enabling EEPROM writes.

The sequence for correctly initializing the EEPROM and write-protecting the CIS on a card is very specific. A ''blank'' serial EEPROM will contain 1's in all locations. The method for initializing the EEPROM using the PCM16C02 is to write the CIS and other data (e.g., Ethernet node ID) to the PCM16C02 attribute memory SRAM and the PCM16C02 specific registers (at offsets 0x3E4 through 0x3FC) from the host system, and then kick off an EEPROM write sequence. In order to write the entire EEPROM (starting at address 0), the EEPROM Start Address field in the Miscellaneous Register must be 0x00. This is the value which will be stored in the EEPROM.

It should be noted that the EEPROM Start Address field in the Miscellaneous Register also affects EEPROM reads which are initiated by setting the ReadEEPROM bit (D6) in the EEPROM Control Register. In this case, the EEPROM Start Address field must be reset to all zeros in order to copy the entire EEPROM contents into the shadow SRAM. This is not an issue for reset-initiated EEPROM reads, since a reset clears the EEPROM Start Address field.

REFERENCES

[1] National Semiconductor Memory Databook, Application Brief 15

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