Interfacing the DP8441 and the NS32GX320

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INTRODUCTION

This application note assumes that the reader is familiar with the modes of operation of the DP8441 DRAM controller and the NS32GX320 microprocessor. The nature of this application note is to give the system engineer an idea of a possible memory configuration. After reading this application note, the system designer must do a thorough analysis for his particular application.

The design's operating frequency is 30 MHz and it supports page and burst accesses. The DP8441 will perform refreshes to the memory and it will guarantee precharge times after access and refresh cycles. The DP8441 will also arbitrate between access and refresh cycles. It inserts wait states into either cycle to allow one or the other to finish.

The design constitutes a complete 32 Megabytes memory system in a 2 bank configuration. The memory array uses 70 ns DRAMs in a 4 Meg $\times$ 4 architecture. The DP8441 supports byte, word or double-word writing. This is done through the $\overline{BE}$ outputs connected to the $\overline{ECAS}$ inputs which control the $\overline{CAS}$s to the DRAMs.

After resetting the DRAM controller, accomplished by keeping the $\overline{RESET}$ input low for at least 16 clock cycles, the DP8441 must be programmed before accessing the memory. Programming can be done by writing to an I/O address equal to the programming selection. Programming can also be accomplished during the first memory write, in this case the CPU writes to an address equal to the programming selection.

After $\overline{ML}$ negates to finish the programming cycle, the DP8441 enters a 60 ms initialization period. This period is when the Phase Lock Loop (PLL) locks into place. The system must wait at least 70 ms before accessing the memory. During this time the DRAM controller performs refreshes to the memory, this makes further ''warm up'' cycles unnecessary.

OPENING ACCESS

A memory access begins when the GX320 outputs a valid address and $\overline{ADS}$ is asserted low. For this design at 30 MHz, the row and column addresses, the B0 and the $\overline{ADS}$ inputs meet the set up times required by the DRAM controller. Three addresses lines are used to do DRAM $\overline{CS}$. The $\overline{CS}$ set up time is also met.

From the rising edge of clock 2 (refer to the waveform), the DP8441 will split the address from the CPU and will output the row address to the DRAMs. The appropriate $\overline{RAS}$(s), as decoded by B0, assert from that rising clock edge latching the row address into the DRAM. The programmed t_{RAH} will be guaranteed by the controller before switching the internal multiplexor to the column address. The controller latches the column address into the DRAM after meeting 0 ns minimum of t_{CSC}. The t_{RAH}, t_{CSC} and the time when the controller switches the row address to the column address is guaranteed by the on-board delay line based on the Phase Lock Loop (PLL).

The controller asserts $\overline{DTACK}$ after the programmed number of wait states to indicate to the CPU that the access can finish. In this design, $\overline{DTACK}$ asserts from the 3rd rising clock edge. The $\overline{DTACK}$ set up time required by the CPU is easily met. At the end of the fourth clock the GX320 will either latch the data into its registers in the case of a read cycle, or it will take the data of the bus in the case of a write cycle. For every access, $\overline{DTACK}$ asserts for one clock period, and $\overline{CAS}$ negates from the same clock edge that $\overline{DTACK}$ negates.

PAGE ACCESSES

Every access finishes when $\overline{DTACK}$ asserts. In this application note, the DRAM controller is programmed in page mode, thus when $\overline{DTACK}$ negates, only $\overline{CAS}$ negate while $\overline{RAS}$(s) stays asserted. When the CPU requests a new access (a new address and a new $\overline{ADS}$), if this new access is within the same page as the previous access (same row address), a page hit is detected by the on-board page comparator. In these cases $\overline{RAS}$ stays asserted and the controller outputs the new column address and asserts $\overline{CAS}$ from the rising edge of clock that $\overline{ADS}$ is set up to. In cases when there is a page miss, the DP8441 negates $\overline{RAS}$, meets the programmed number of clock cycles for precharge, and then asserts $\overline{RAS}$ to latch the new row address into memory. In either case, $\overline{DTACK}$ will assert and negate after the programmed number of wait states according to ''page mode'' or ''opening access'' (page hit or page miss).

BURST ACCESSES

The GX320 spects the addressed peripheral to indicate whether or not it can burst. The DP8441 can always burst, therefore the $\overline{BIN}$ input to the CPU is always asserted every time there is a memory access. When the GX320 detects $\overline{BIN}$ asserted and if the CPU wants to burst, the GX320 will assert the $\overline{BOUT}$ signal. $\overline{BOUT}$ is directly connected to the input $\overline{BSTREQ}$ on the DP8441. $\overline{BSTREQ}$ asserted makes the DRAM controller to increment the column address every time $\overline{DTACK}$ negates, and the DRAM controller will automatically assert $\overline{CAS}$ to latch the new column address into memory. The DP8441 will burst for as long $\overline{BSTREQ}$ is asserted. Every burst access finishes with the assertion and negation of $\overline{DTACK}$.

REFRESH AND PRECHARGE

The DP8441 will request a memory refresh every 15 μs. During refresh, $\overline{RAS}$ will be low for 3 clock periods. The controller will also guarantee precharge of 3 clock periods. These timings are enough for 70 ns DRAMs. If the controller is in the middle of a page mode access ($\overline{RAS}$ asserted but no real access may be in progress) the controller will keep track of all refresh requests. When there is an access out of page, the DRAM controller will burst refresh the memory of the number of refresh requests missed. If the in-page access is idle, and there is a sixth refresh request, the DRAM controller will automatically finish the access, meet the precharge time, and burst refresh the memory six times.

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PROGRAMMING BITS

TABLE I

R1, R0 0, 1	$\overline{RAS}$ Low and Precharge Time 3Ts
R3, R2 0, 1	$\overline{DTACK}$ during Opening Access will Assert after $\overline{RAS}$ 2Ts
R5, R4 0, 1	$\overline{DTACK}$ during Burst Access will Toggle with $\overline{CAS}$ 1T
R7, R6 0, 1	$\overline{DTACK}$ during Page Access will Assert after $\overline{CAS}$ 1T
R8, R9 1, 0	Page Size Select to 2048 for 4 Meg DRAMs
R11, R10 0, 1	Wrap Around Size Select 4. (00 01 10 11)
C3, C2, C1, C0 0, 1, 0, 1	Divisor Select for DELCLK to get Close to 2 MHz. 15. (30/15 = 2)
C5, C4 1, 1	B0 is not used. Staggered Refresh B1 = 0 ⟶ $\overline{RAS}$ 0,1 $\overline{CAS}$ 0,1,4,5 B1 = 1 ⟶ $\overline{RAS}$ 2,3 $\overline{CAS}$ 2,3,6,7
C6 0	Staggered Refresh Selected
C7 0	t_{RAH} = 10 ns
C8 1	Page Miss Output Selected
C9 0	CAS Precharge Time during Burst ½T during Read and 1T during Write
C10 0	RAS Only Refresh Selected
C11 0	15 μs Refresh Period
B0 1	DTACK Rising Edge Increments the Column Counter
B1 0	Page Mode Selected
ECAS0 0	Latch Mode Selected (To be able to increment the column counter during burst)
ECAS1 0	Burst Request Select is Active Low
ECAS2 0	CAS and DTACK Clock Edge Select is the Rising Clock Edge

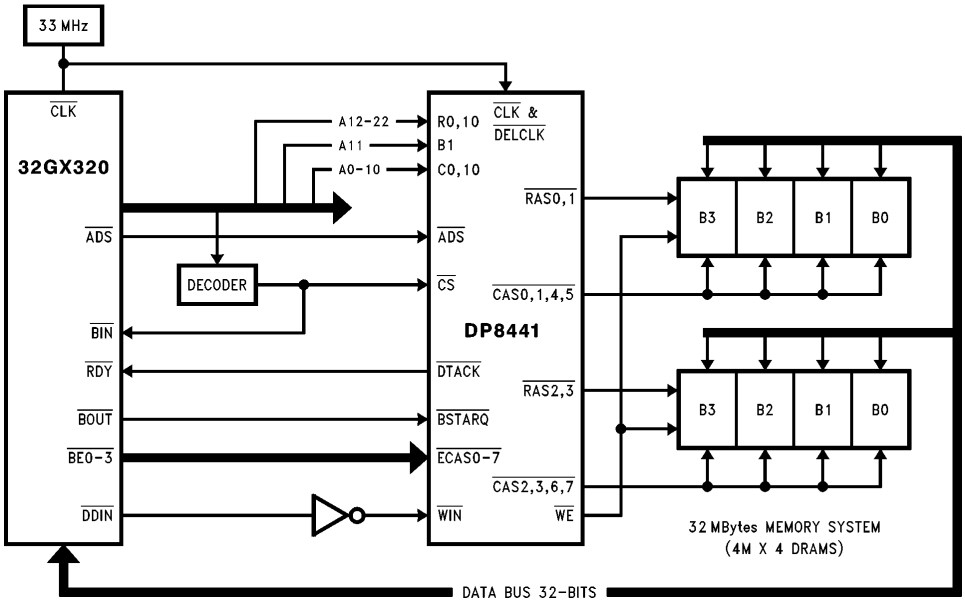
TIMINGS FOR INTERFACING THE NS32GX320 AND THE DP8441 DRAM CONTROLLER RUNNING AT 30 MHz

1. Minimum $\overline{ADS}$ Low Set Up Time to CLK High.
   1 CLK Period—CLK High to $\overline{ADS}$ Asserted (GX320)
   33.33 ns − 9 ns
   24.33 ns The DP9440/41 need only 6 ns
2. Minimum Address Valid Set Up Time to CLK High.
   1 CLK Period—CLK High to Address Valid (GX320)
   33.33 ns − 9 ns
   24.33 ns The DP8440/41 need only 10 ns
3. Minimum $\overline{CS}$ Asserted Set Up Time to CLK High.
   1 CLK Period—(CLK High to Address Valid + Decoder Delay)
   33.33 ns − (9 ns + 16 ns)
   33.33 ns − 25 ns
   8.33 ns The DP8440/41 need only 4 ns
4. Wait States Through $\overline{DTACK}$ during Opening Accesses.
   4a. Access Time from RAS
   1 CLK Period + CLK High to $\overline{RAS}$ Asserted (DP8440/41) + DRAM t_{RAC} + Data Set Up Time (GX320)
   33.33 ns + 15 ns + 70 ns + 8 ns
   126.33 ns ⟶ 4 CLK Periods (133.32 ns)
   4b. Access Time from $\overline{CAS}$
   1 CLK Period + CLK to CAS Asserted (DP8440/41) + DRAM t_{CAC} + Data Set Up Time (GX320)
   33.33 ns + 55 ns + 20 ns + 8 ns
   116.3 ns ⟶ 4 CLK Periods (133.32 ns)
   4c. Access Time from Column Address Valid
   1 CLK Period + CLK High to Column Address Valid (DP8440/41) + DRAM t_{AA} + Data Set Up Time (GX320)
   30.3 ns + 51 ns + 35 ns + 8 ns
   127.33 ns ⟶ 4 CLK Periods (133.32 ns)

   From 4a, 4b and 4c, $\overline{DTACK}$ should assert from the 3rd rising CLK edge. Therefore program $\overline{DTACK}$ during opening accesses as 2T.
5. $\overline{RDY}$ Set Up Time (GX320)
   1 CLK Period—$\overline{DTACK}$ Asserted from CLK High
   33.33 ns − 12 ns
   21.33 ns The GX320 needs only 12 ns
6. $\overline{CAS}$ Precharge during Burst Accesses
   Program the DP8440/41 for 1/2T of CAS precharge. It will guarantee a minimum of 10 ns before $\overline{CAS}$ asserts.
7. Wait States through $\overline{DTACK}$ during Burst Accesses
   CLK High to CAS Negated + Max CAS Precharge (1/2T) + DRAM t_{CAC} + Data Set Up Time (GX320)
   12 ns + 14 ns + 20 ns + 8 ns
   54 ns ⟶ 2 CLK Periods (66.66 ns)
8. Wait States through $\overline{DTACK}$ during Page Accesses
   1 CLK Period—(CLK High to CAS Asserted + DRAM t_{CAC} + Data Set Up Time
   33.33 − (12 ns + 20 ns + 8 ns)
   −6.66 ns ⟶ Needs 1 Wait State
9. $\overline{RAS}$ Low during Refresh
   Program the DP8440/41 for 3T of refresh to guarantee 70 ns t_{RAS}.

The AC timing parameters used in this application note were preliminary. The AC parameters have changed, and the reader should refer to the latest DP8440/41 datasheet.

Interfacing the NS32GX320 with the DP8441 DRAM Controller



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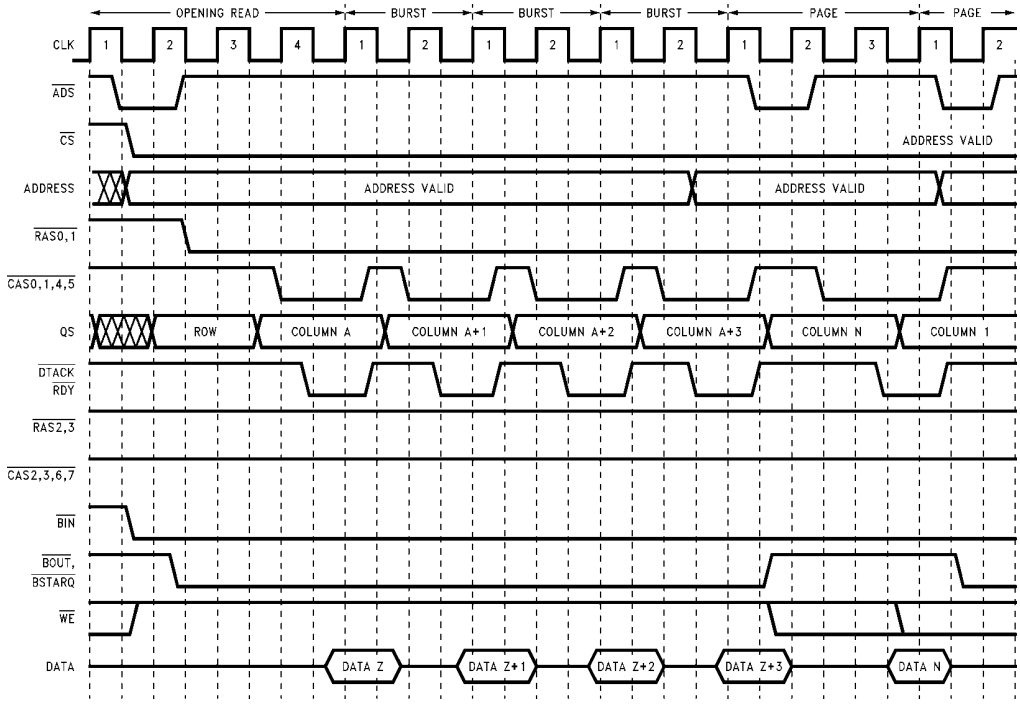
NS32GX320 Opening, Burst and Page Accesses. 4-2-2-2 and 3Ts



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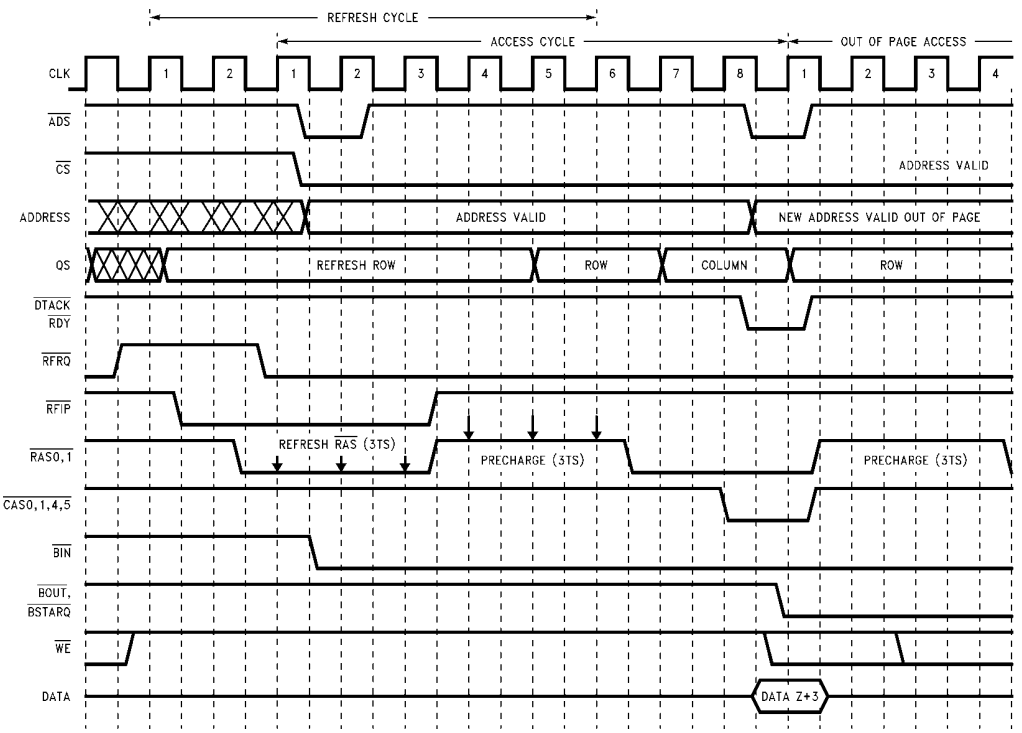
Refresh Cycle and Delayed Access



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