National Flash Memories—Hardware Design Guide

National Semiconductor
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P. Mohan Prasad
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National offers two types of Flash Devices, namely NOR type and NAND type. The device densities ranging from 1 Mbit to 16 Mbit, suited for various kinds of applications like BIOS code storage, Solid state file storage, Image file storage, etc. Some of the devices also feature Auto program/erase operations which aid in elegant, compact programming code.

This note describes the various hardware considerations that a system designer has to consider when using National's Flash devices.

ORGANIZATION

1. DEVICE CONSIDERATIONS

   This section addresses the various issues like programming voltage (V_{PP}) generation and control, V_{CC} considerations, etc.

2. NOR DEVICES

   The NOR Flash device section covers the individual design considerations for the following Flash devices

   NM28F010: 1 Mbit, byte wide device.

   NM28F040: 4 Mbit, byte wide device.

   NM28F044: 4 Mbit, byte wide device.

3. NAND DEVICE

   This section covers NAND type NM29N16 device, which is a 16 Mbit, 5V only device ideally suited for large file storage type of applications, like Solid state Disk, PCMCIA based Memory cards, etc.

4. ICP (In-Circuit Programming)

   Finally, this note also discusses the In-Circuit Programming (ICP) in general, and the various types of ICP configurations available today.

1.0 DEVICE CONSIDERATIONS

V_{PP} Specifications: National's Flash devices have ±5% tolerance specification on the 12V level that is required for V_{PP}. This specification is guaranteed by most of the off-the-shelf industry standard power supplies. In fact the PC-AT® system power supply has a +5% and −4% tolerance specification on the +12V level.

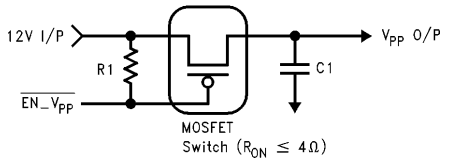

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FIGURE 1

The *Figure 1* represents a typical MOSFET Switch for the 12V line in the interface design towards Flash devices. MOSFET of the above configuration is available from a number of vendors, and MTD4P05 Motorola device is one good example. The only consideration is that the ON-RESISTANCE of the selected Switch should be low enough to keep the V_{PP} o/p within ±5% tolerance range.

The 12V V_{PP} programming voltage required for Programming/Erasing operations on the device is gated from the source (power supply's +12V TAP) through an enabling circuitry (e.g., a MOSFET Switch) to the Flash memory's V_{PP} pin. An enable signal from the system's control circuitry, say, "$\overline{V_{PP}\_EN}$" could then be used to switch ON/OFF the 12V path to the Flash memory's V_{PP} Pin.

Usage of this 12V Switch achieves two purposes:

1. Having the Switch turned off during power up ensures that V_{PP} voltage at the V_{PP} Pin of the device doesn't ramp up before the V_{CC} ramps to the required 5V level, which is a basic requirement for the Flash device.
2. In systems, especially laptop portables, having 12V supply enabled ON continuously is not a favourable choice in terms of the power drain of the Battery, since the need for 12V on the V_{PP} Pin is only during Programming/Erasing, etc. operations and not for the typical Read operation. Hence a Switch to turn on the 12V for V_{PP} only during the required limited times saves considerable power.

Additional Considerations: The *Figure 2* shows a typical circuit of a power control circuitry. This kind of a circuitry helps in improving the data integrity. The power sensing device in essence monitors the power supply's 5V output and

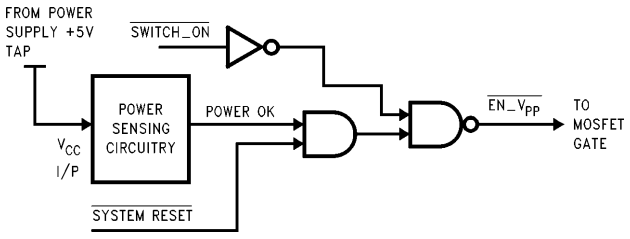

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FIGURE 2

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asserts a ''power OK'' signal only when the input V_{CC} is within the tolerance limits. When the input V_{CC} levels cross the tolerance level, the ''power OK'' signal is deasserted (driven low) which in turn switches off the MOSFET switch and thus disabling the 12V from reaching the V_{PP} Pin anymore. System's reset signal is also coupled along with this ''power OK'' signal to take care of power_up and warm reset conditions. ''Switch ON'' signal is an output from system control circuitry which determines when to apply 12V at the V_{PP} pins of the Flash device under normal operations.

V_{PP} Generation: In the above discussion it is assumed that the 12V ±5% supply is readily available in the system, but for systems where this tolerance requirement is not met or when the 12V ±5% supply is not available at all from the system power supply there are ample V_{PP} Generation circuits available which generally employ one of the following techniques.

1. DC to DC conversion.
2. Regulation from a higher voltage (Down conversion).
3. Voltage boosters (5V to 12V).

A number of solutions employing the above mentioned techniques are available from National Semiconductor. Please refer to the listing given at the end of this note for the source.

V_{CC} Specifications: NSC Flash devices have a tolerance specification of ±5% on the 5V V_{CC} line. Though most of the available Power supplies have a ±5% tolerance specification on their +5V line, variation of this voltage within this tolerance range is dictated by the system loading and switching frequency of the devices at any given instant of time. Proper consideration should be given in choosing a matched Power supply in terms of the Power wattage against the total expected maximum load on the 5V line. Also adequate powerline decoupling especially around the memory devices and high speed switching devices should be ensured, which would take care of the V_{CC} droop caused by device switching to be within the tolerant limits.

Power Sequencing: To protect the device against any data corruption during Power cycling the following power sequencing is required.

Power On Condition: V_{PP} must be applied only after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high.

Power Off Condition: V_{PP} must be turned off after V_{CC} stabilizes to within 5V ±5% and while $\overline{CE}$ is high. V_{CC} can only be turned off after V_{PP} has reached 0V.

The sample circuit shown in *Figure 2* employing a power sensing unit inherently takes care of the Power-Sequencing required, without any additional logic.

2.0 NOR DEVICES

1. NM28F010 (128k x 8)

The following note describes the In-circuit programming aspects for a system using National's NM28F010 Flash memory device.

NM28F010 is a 1,048,576 bit Flash Electrically Erasable and Programmable Non-volatile memory device. It features single command for typical operations like READ, CHIP ERASE and PROGRAM allowing ease of use for in-circuit programming from within a system.

Software Considerations: The following two tables depict the various modes of NM28F010 Flash device operation and the command definitions to set to a particular mode.

Mode Selection Table

Mode		Signals							
		$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Address	Data	V_{CC}	V_{PP}	Power
READ	Read	L	H	L	Read Address	Data Output	5V	0 ~ V_{CC} or 12V	Active
	Output Deselect	L	*	H	*	High Impedance			
	Standby	H	*	*	*				Standby
COMMAND INPUT	$\overline{WE}$ Control	L	⌝⌟	H	(Note 1)	Command Data	5V	12V	Active
	$\overline{CE}$ Control	⌝⌟	L	H	(Note 1)	Command Data			
PROGRAM/ERASE		*	H	H	H				
PROGRAM/ERASE VERIFY		L	H	L	(Note 1)	Data Output			
ID READ		L	H	L	0x0/0x1	Data Output			

*H or L

Note 1: Refer Command Definition Table

Command Definition Table

Function	No. of Bus Cycles	First Bus Cycle			Second Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	*	00H	NA	NA	NA
ID Read	2	WRITE	*	90H	READ	0x0H/0x1H	Mfg/Dev ID
Chip Erase	2	WRITE	*	20H	WRITE	*	20H
Erase Verify	2	WRITE	Byte Address	A0H	READ	*	EV Data
Program Setup/ Begin	2	WRITE	*	40H	WRITE	Byte Address	WR Data
Program Verify	2	WRITE	Byte Address	C0H	READ	*	WV Data
Reset	2	WRITE	*	FFH	WRITE	*	FFH

*H or L

Interface Block Diagram

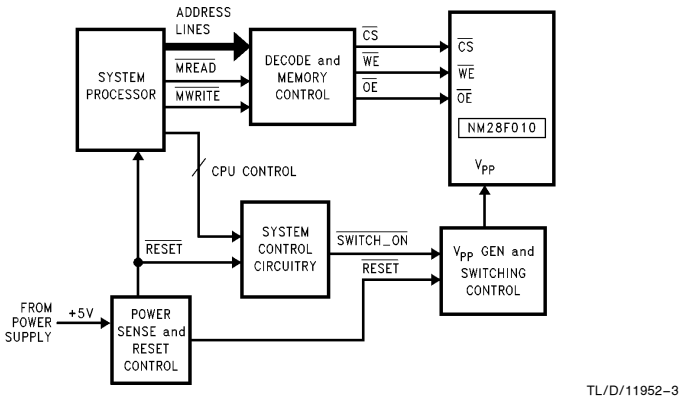

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FIGURE 3

Operating Modes: NM28F010 features seven modes of operation as shown in COMMAND DEFINITION TABLE. Setting the device to any particular mode is by writing an appropriate opcode to the Command register of the device. Note that the Command register by itself doesn't occupy any address range of the device and write to the Command register is enabled only when V_{PP} is at 12V level.

A detailed description of the various operating modes can be found in NM28F010 data sheets.

Figure 3 depicts a typical wiring diagram of control signals for a system using National's NM28F010 FLASH Memory with a block level specifications of the integral functional units discussed earlier.

Description: Interface to NM28F010 Flash memory is very much similar to that of conventional 27C010 EPROM except that the system's memory write enable $\overline{\text{MWRITE}}$ is also considered.

The DECODE and MEMORY CONTROL logic could be a simple combinatorial PAL®, like 16L8, which takes in the higher order address lines, memory read and memory write control signals as input and generates Flash memory chip select ($\overline{\text{CS}}$), output enable ($\overline{\text{OE}}$) and write enable ($\overline{\text{WE}}$).

2. NM28F040/NM28F044

NM28F040 and NM28F044 are 4,194,304 bit (512 x 8) CMOS Flash devices featuring single command for Read, Auto Chip erase, Auto Block erase and Auto Program/Verify allowing ease of use for in-circuit programming. NM28F040 is a 32 pin device whereas NM28F044 is a 44 pin device.

UNIQUE FEATURES

Block Mode Erase: These Flash devices can either be full chip erased or in terms of a specific block of 16 kbyte. This block mode erase feature allows ease of management of code blocks.

Auto Function: Both these devices feature a unique "AUTO-FINISH" facility for commands like Chip erase, Block erase and Program/Verify. Once after issuing any of the above commands to the device, all that is required is to sample the device data lines, D7 for operation completion (RDY/BUSY) and D4 for status of completion (FAIL/PASS). These devices have the necessary logic built-in inside the chip to do all of the iterative routines of the programming software. Looping through the same part of the code till operation proves to be a success or failure becomes unnecessary and all those iterative functions can now be removed from the code, resulting in a compact elegant programming algorithm.

Software Considerations: The following two tables outline the various operational modes and the command definition to set the various modes.

Mode Selection Table

Mode		Signals						
		$\overline{CE}$	$\overline{OE}$	Address	Data	V_{CC}	V_{PP}	Power
READ	Read	L	L	Read Address	Data Output	5V	0 ~ V_{CC} or 12V	Active
	Output Deselect	L	H	*	High Impedance			
	Standby	H	*	*				Standby
COMMAND INPUT		⌐⌐	H	(Note 1)	Command Data	5V	12V	Active
PROGRAM/ERASE		*	*	*				
PROGRAM/ERASE STATUS POLLING		L	L	*	DO ~ 3,5,6:Z D4-fail/pass D7-rdy/busy			
ID READ		L	L	0x0/0x1	Data Output			

*H or L

Note 1: Refer COMMAND DEFINITION TABLE

Command Definition Table

Function	No. of Bus Cycles	First Bus Cycle			Second Bus Cycle		
		Type	Address	Data	Type	Address	Data
Read	1	WRITE	*	00H	NA	NA	NA
ID Read	2	WRITE	*	90H	READ	0x0H/0x1H	Mfg/Dev ID
Auto Byte Program	2	WRITE	*	10H	WRITE	Byte Address	WR Data
Auto Chip Erase	2	WRITE	*	30H	WRITE	*	30H
Auto Block Erase	2	WRITE	*	20H	WRITE	Block Address	D0H
Reset	2	WRITE	*	FFH	WRITE	*	FFH

Operating Modes: Both NM28F044 and NM28F040 feature same modes of operation, viz., Read, ID Read, Reset, Auto Byte Program, Auto Chip Erase and Auto Block Erase.

The Read, ID Read and Reset modes of operation of these two devices are the same as that of NM28F010, however the Program and Erase modes are significantly different from NM28F010.

A more detailed description of the various operating modes can be found in the relevant device data sheets.

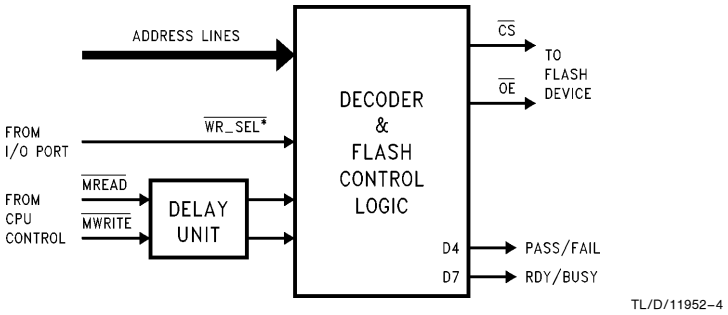
HARDWARE CONSIDERATIONS

1. NM28F044

Designing around NM28F044 is very much similar to NM28F010 which we discussed earlier, but with the following difference:

Two of the data lines, D7 and D4, signify the operation completion and status of completion respectively. Once after issuing any of the Auto Byte Program, Auto Chip Erase and Auto Block Erase commands to the device, all that is required is to do a read on the device after a specified time (depending on the command issued). A High (High logic level) on the data line D7 signifies that the operation for the issued command was completed. The data line stays at Low (Low logic level) if the operation is not completed yet. Similarly, when D7 has become high, a Low (Low logic level) on the D4 line signifies success of the operation and a High (High logic level) signifies failure.

2. NM28F040



(*"WR_SEL" signal could be same as "EN_V_{PP}" signal)

FIGURE 4

NM28F040 Flash device is different from NM28F044 Flash device in sense that it doesn't have a "WE" signal. The "CS" signal in this device acts as a multiplexed pin for both chip select (in the case of a read from the device) and write enable (in the case of a write to the device). Write mode is differentiated from the READ mode by the following conditions:

CS	OE	Operation on the Device
L	L	READ
*	H	WRITE

* → CS pulsing when OE is held high

But "CS" signal continues to behave like a chip select signal (read mode) as long as V_{PP} voltage remains below V_{CC}, no matter whatever operation (READ or WRITE) is done on the device. *Figure 4* shows one possible way of interfacing NM28F040 Flash device in a system.

"CS" Generation: The potential problem of chip select (CS) signal glitching and thus leading to the possibilities of corrupting any valid data in the Flash device can be easily surmounted with simple logic. Data corruption chances are possible in NS28F040 Flash device only when 12V power is enabled to the V_{PP} pin of the device and then there is an extraneous cycle happening on the bus (bus cycle to a device other than the Flash device).

Memory decode designs in general incorporate a mechanism of gating the decoded signal (from the address bus) with Memory control signals (MREAD and MWRITE) to generate a valid chip select to the memory. **Glitches become apparent when the total time for the address bus to get stabilized to valid logic levels (say, Tsb) and the time to decode the address lines (say, Td) is longer than the Memory control signal (MREAD or MWRITE) driven valid delay (say, Tv).**

In systems where both the Address lines and the memory control signals are driven simultaneously this "glitching" scenario is inherent and one common way of eliminating the glitches in the output (chip select) signal is to delay the memory control signal by an amount greater than **Tsb + Td** and using this delayed signal for gating purpose. Simple DELAY LINE devices can be used to delay the control signals, as shown in *Figure 4*.

Processors like I80486, output Address, Memory control (M/IO) and Read Write (PW/R) control signals all at the same instant whenever an external cycle is started on the system bus. In this scenario, generating the chip select signal from address and M/IO and PW/R control signals all gated together would have the output chip select signal glitching for a period equal to the above mentioned **Tsb + Td.** But by using a delayed (by an amount **Tsb + Td**) memory READ/WRITE signal for final gating, chances for glitches in the chip select signal is eliminated.

"WE_SEL" Signal: The "WE_SEL" signal shown in *Figure 4* is a signal from one of the available general purpose I/O ports. This signal in most cases is the same as the "EN_V_{PP}" signal which was discussed earlier.

Prior to doing any write operation on the Flash device, the V_{PP} circuitry must be turned on so that V_{PP} voltage at the V_{PP} pin is 12V. "EN_V_{PP}" is a signal generated for this purpose. The same signal can be used in the CS generation logic to gate the decoded address signal with either of the memory control signals (MREAD and MWRITE) which ever becomes valid during a particular Flash device access. The need for having to do this is due to the multiplexed nature of the chip select pin of the Flash device.

The following representative schematic *(Figure 5)* explains the above discussion.

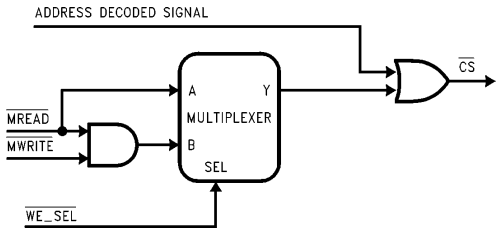


FIGURE 5

Common Considerations: In all the three Flash devices discussed so far, it is essential that proper command codes are entered in proper sequence. Inputting any command code other than those described could render an improper device functionality. Also accidental removal of V_{PP} supply during any Erase or Program operation in progress should be taken care of, for in some cases the valid data in the device could get corrupted. It's also essential to employ a POWER ON/OFF sequence as described earlier to safeguard the valid data against any corruption possibilities during power cycling.

3.0 NAND DEVICE

NM29N16 (2M x 8-Bit)

GENERAL DESCRIPTION

National's NM29N16 is 16.5 Mbit NAND Electrically Erasable and Programmable device. NM29N16 is a 5V only device, which does not require 12V for any of the Programming or Erase operations.

Organization: NM29N16 is organized as (256 + 8) bytes x 16 Pages x 512 Blocks. Programming is done in terms of a Page (264 Bytes each) while Erasing is done in terms of a Block or multiples of Blocks (16 Pages each). *Figure 6* depicts a conceptual organization of the Device.

NM29N16 is a byte__wide serial type of device in which the Address and Data are time multiplexed on the same I/O pins as there are no separate Address pins. Address in input as three bytes of Data during Address input cycles. The Program and Erase operations are handled automatically by the device, resulting in minimal Processor intervention and elegant programming code.

Additionally, the device aids in mapping out bad memory locations by providing an extra 8 bytes of redundant memory for every page in the device. This feature makes NM29N16 Flash device as an ideal candidate for SOLID STATE FILE STORAGE applications. Alternatively, this redundant 8 byte space per page can be used for normal storage resulting in extra capacity (16.5 Mbits instead of 16 Mbits).

Applications: NM29N16 is ideally suited for applications like,

1. Solid State File Storage
2. Voice Recording
3. Image File Storage, etc.

NM29N16 type of a device is the most sought after in Solid State File Storage where large data is stored and retrieved at a single access (Normally in terms of some specified Blocks Size). With the advent of PCMCIA based systems, Solid State Data Storage has become an intelligent form of Data storage and NM29N16 with its unique features is the ideal candidate for PCMCIA based Solid State Disk.

Device Specific Details: NM29N16 has the following control signals, whose combination, as depicted in the following truth table, signify the various operations that can be performed on the device. The control signals are **CLE** (command latch enable), **ALE** (address latch enable), $\overline{\textbf{CE}}$ (chip enable), $\overline{\textbf{WE}}$ (write enable), $\overline{\textbf{RE}}$ (read enable) and $\overline{\textbf{WP}}$ (write protect).

Truth Table

	CLE	ALE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{RE}}$	$\overline{\text{WP}}$
Command Input	H	L	L	⌐⌐	H	X
Data Input	L	L	L	⌐⌐	H	X
Address Input	L	H	L	⌐⌐	H	X
Address Output	L	H	L	H	⌐⌐	X
Serial Data Output	L	L	L	H	⌐⌐	X
During Programming (BUSY)	X	X	X	X	X	H
During Erasing (BUSY)	X	X	X	X	X	H
Program/Erase Inhibit	X	X	X	X	X	L

H: V_{IH} L: V_{IL} X: V_{IL} or V_{IH}

Operating Modes: The device supports the following modes of operation, viz., Read Mode-1, Read Mode-2, Status Read, ID Read, Auto Page Program, Auto Block Erase, Auto Multi-Block Erase, Suspend/Resume and Reset.

The device is set into any of the above modes by writing an appropriate opcode into the device Command Register. Then if needed the Address and Data registers are updated. Thus programming the device for any mode of operation involves anything from one step to four step process, depending on the mode. Various Command codes (opcodes) needed for those above mentioned modes are listed in the Command Table.

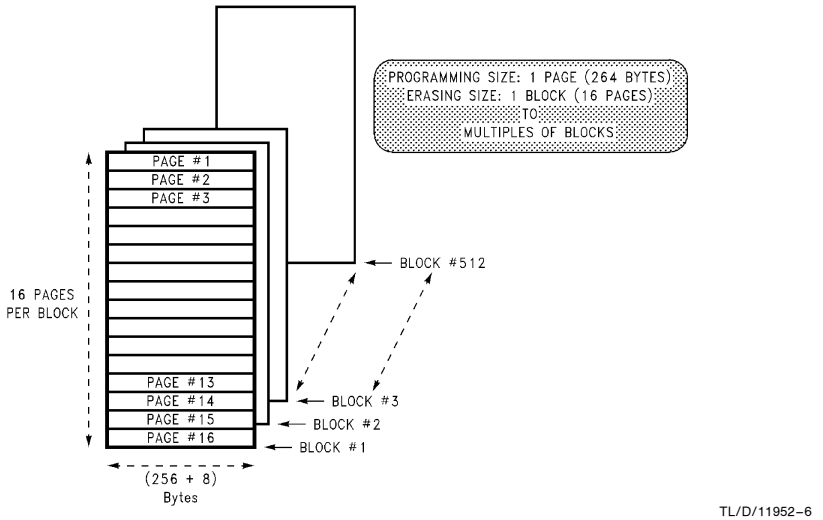


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FIGURE 6

Command Table

Modes of Operation	First Cycle (opcode)	Second Cycle #
Read Mode-1	00	
Read Mode-2	50	
Reset	FF	
Auto Program	80	10
Auto Block Erase	60	D0
Auto Multi Block Erase	60*	D0
Erase Suspend	B0	
Erase Resume	D0	
Status Read	70	
Register Read	E0	
ID Read	90	

Note: Second cycle shown above for the Program/Erase operations is a confirmatory cycle. The actual execution begins only after this command write. This feature is to safeguard against any inadvertent erasures, especially during Power Up.

*For Multi-Block erase operations, Command code (60) is repeated for every block to be erased. Typical sequence for a three block erasure would be, <OPCODE "60"> <Add of Block#1> <OPCODE "60"> <Add of Block #2> <OPCODE "60"> <Add of Block#3> <OPCODE "D0">.

DESCRIPTION OF OPERATIONS: There are basically two types of operations performed on the device, viz., READ and WRITE.

READ Type Operations: Read mode-1, Read mode-2, Status read, Register read and ID read are the operations which conform to Read type. For all these modes the appropriate command code is first written into the device Command register (first cycle). Then depending on the mode issued, address information is written into the Address register, which is essentially three write cycles following the Command input cycle. Then after a specified delay data is read off the Data register through a typical read cycle. Address information is not input for a Status Read operation. All these Registers, viz., Command, Data, Address and Status, do not occupy any of the device's memory location. They are indeed selected by the combination of logic levels of the control signals ALE and CLE. Note also that the Command Register cannot be read back for the contents.

The starting address is composed of 3 bytes, which are entered right after the command input in three successive write cycles. The format of the address is input as shown below:

	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	I/O8
First Address Cycle	A0	A1	A2	A3	A4	A5	A6	A7
Second Address Cycle	A8	A9	A10	A11	A12	A13	A14	A15
Third Address Cycle	A16	A17	A18	A19	A20	L	L	L

Note: I/O bits 6, 7 and 8 should be set to low level during the third address cycle.

A12 to A20 form the Block address (selects one out of 512 Blocks).

A11 to A8 form the Page address (selects one out of 16 pages) within a selected Block.

A0 to A7 form the column address (selects the starting address of the data transfer within a page).

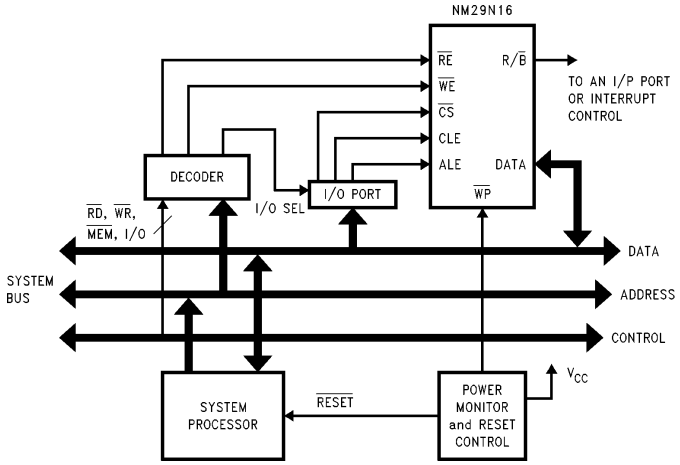

FIGURE 7

WRITE Type Operations: Operations like Program, Erase, Erase suspend, and Reset conform to Write type of command. Setting the device for these operating modes is similar to earlier described READ type operations. In these modes the device is updated with some new information.

A more detailed description of the various operating modes are found in the Device data sheets. Refer to the table given at the end of this note.

Hardware Interface: The *Figure 7* shows one of the methods of interfacing NM28N16 Flash device in a system. A generic Processor (Micro-controller) is assumed in this discussion. The external interface attributes (Bus Control Interface) of this generic processor is commonly found in almost all of the available Processors.

Types of Cycles: The cycle types that are typically performed on NM29N16 Flash device fall into three categories, viz., Command, Address and Data cycles. The following table explains the control signal configuration during these three cycles.

Cycle Types		CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$
Command	Input	H	L	L	⌇	H
Address	Input	L	H	L	⌇	H
	Output	L	H	L	H	⌇
Data	Input	L	L	L	⌇	H
	Output	L	L	L	H	⌇

The Input/Output cycles (in Address and Data cycles) are differentiated by $\overline{WE}$ and $\overline{RE}$ pulsing respectively with other being stable. In general all these three cycles happen either $\overline{RE}$ or $\overline{WE}$ pulsing during a stable window of the other control signals as shown in the above table.

I/O Port: Having an I/O Port type of interface is necessitated by the fact that the NM29N16 Flash Device control signals are not of the same type which are normally found in common Flash Devices. NM29N16 device is meant for large data storage applications (Memory cards, Solid state disk, etc.) where the device form factor is also crucial. In view of this, the device features an optimized Pinout, resulting in a compact device and yet with a much larger capacity. The control signals of this NM29N16 Flash device is not directly compatible to existing Micro-controller interface control. An I/O Port type of interface between this Flash device and any common Micro-controller normally considered for this type of an application, simplifies the interfacing task without any complex logic.

The I/O Port shown in the above diagram is any general purpose I/O port, normally found in a system. One such I/O port is availed to establish the key interface to the NM29N16 Flash device. Three control signals, viz., ''$\overline{CS}$'', ''CLE'' and ''ALE'' are driven by this I/O port as shown. Before doing an actual NM29N16 access, the system CPU initially writes to this I/O Port with the needed signal configuration for the type of the cycle (Command, Address or Data). Then a normal Read or Write cycle to the Flash device memory space would do an actual Read or Write cycle on the device.

Decoder: The decoder unit generates the Read/Write control signals for the Flash device. System address, memory control signals form the input to this unit. This unit could be a combination of discrete devices like 'LS139 or just a combinatorial $\overline{PAL}$ like 16L8 device.

Power Monitor: This unit basically monitors the V_{CC} power point for the required operating level. Whenever the system V_{CC} falls out of the $\pm 5\%$ tolerance range, this unit generates the system Reset as well as the write protect signal ($\overline{WP}$). This unit takes care of the POWERON condition also by keeping the system Reset and $\overline{WP}$ asserted till the system V_{CC} reaches the proper required level and thus protecting the data against corruption. Power monitor unit is available from numerous vendors in the form of a single device. One typical example of such a device would be Dallas Semiconductor component DS1231.

Ready/Busy Signal: This status output signal can be routed to an Input Port, which the CPU can keep polling for the status of operation completion or alternatively to the system's Interrupt control so as to generate an interrupt upon operation completion.

4.0 ICP (IN-CIRCUIT PROGRAMMING)

In-circuit programming (ICP) as opposed to device level programming is an efficient method of programming the most widely used programmable devices like, PROM, EPROM, PAL, PLD, Micro-controllers, FPGA, FLASH memory, etc. ICP is a means of programming these devices after they have been assembled into their target boards. There are broadly two categories of In-circuit programming, one being *Production oriented* and the other being *End user oriented*.

ICP Benefits: Obvious advantages of ICP over the traditional device-level programming are streamlined manufacturing flow, simplified handling, lesser inventory overheads and reduced production costs. ICP has become a preferred method of programming the device with the gaining usage of surface-mount devices (SMDs) and the Just-in-time production methods.

ICP Configurations: Different configurations are available today to achieve the programming of these devices in their target enclosure.

1. *Standalone In-circuit Programmers:* This is the Production oriented type of configuration and in this, the target (device assembled) board(s) get plugged on to slots assigned for programming purpose in the Standalone In-circuit Programmer, much like individual devices (ICs) getting plugged into the IC sockets of a Device Programmer. Then the relevant programming algorithm, resident in the In-circuit Programmer, is executed by the In-circuit Programmer to program the device with the proper data. A typical example of this kind of programmer would be DATA I/O's BoardSite. In this case the target boards usually have additional circuitry to isolate the programmable device(s) from the onboard's logic which is essential during the device programming. The level of complexity of this additional logic varies depending on the type of the device and the number of such devices.

This kind of configuration is well suited for production site programming where assembled boards are directly programmed for the devices present instead of programming the individual devices and house keeping them before assembly into a particular board.

2. *Programming via serial link:* In this configuration the target board has a serial link interface for the purpose of programming (or reprogramming) the device(s) on board. This target board is hooked to a conventional Device programmer via the serial interface, in which case the Device Programmer does the programming job as it would program an individual device.

Compared to the earlier discussed *Production type ICP*, this falls into *End-user type of ICP*, and this method eases the task of any code update at customer site without having to disassemble the target board from the system. But then a device programmer is required to be carried to the customer site to do any re-programming.

3. *In-System Programming:* In this configuration, typically a remote host downloads the software to be updated onto the target system through, say, a serial link. Then the target system executes the resident programming algorithm to program the mounted device. Instead of a serial link, a floppy diskette containing the updated code could be downloaded into the target system for programming purposes.

This approach of In-circuit Programming is preferred where frequent code change is involved, especially in customer field locations, where dismantling the whole system for device replacement purposes is not welcomed and it is not required to carry any device programmer to the customer site.

Flash Memory: An In-circuit Programmable device of particular concern here is a FLASH device which as byfar come in as a drop in replacement for the conventional EPROMs. Apart from delivering the ''functional compatibilities'', they feature a significant advantage over EPROMs in terms of Re-programming conveniences whenever a code__update is necessitated. Unlike EPROMs which have to be removed from the target board, Ultra-Violet erased, programmed with the new code and then plugged back into the target board, the FLASH devices are erased instantly and re-programmed with the new code all performed when the device is in the target board only, thus bringing all the benefits of ICP.

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998