PCB Layout and Decoupling for QR0001

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INTRODUCTION

Resolving layout and decoupling issues on printed circuit boards for high speed systems becomes more demanding as performance is maximized. This application note gives some general guidelines and recommendations for QR0001 in high speed designs.

Before discussing layout and decoupling, however, it is helpful to briefly review the port structure and power regions of the device. The QR0001 has 2 client and 2 ring ports. The client Tx/Rx Ports have a maximum speed of 50 MT/s, which is a 32-bit symbol every clock tick at 50 MHz, and the ring Up/Dn Stream Ports have a maximum speed of 350 Mb/s, which is 175 MHz.

The QR0001 has four distinct power regions, two for digital circuitry and two for analog circuitry.

1. $DV_{CC}1$: Core logic and client TX port power which together consumes about two thirds of the total I_{CC} current.
2. $DV_{CC}2$: Client RX port power, which consists of TTL drivers output.
3. $AV_{CC}3$: LVDS ring port power which consumes a constant 45 mA (approx.).
4. $AV_{CC}4$: PLL circuitry power which consumes a constant 24 mA (approx.).

PCB LAYOUT FOR QR0001

High speed circuits generally consume more power than similar low speed circuits as shown below in Table I.

At the system level, this means that (1) the power supply distribution system must be able to handle the larger current flow, and (2) the ground metal should cover as large an area as possible to reduce the length and inductance of the return path which can eliminate the ground noise. In order to minimize ground noise, and high-current devices should be as close as possible to the power entry point. The printed circuit board traces which carry high speed digital signals behave like transmission lines. The transmission line effects can cause reflection (ringing), distortion, and crosstalk between adjacent lines. Understanding this behavior is important for trouble-free board design. A basic rule of thumb is that PC board traces should be treated as transmission lines if the unloaded signal transition time at the driving end is equal or less than the round-trip propagation delay for the trace. Typically the transmission line delay is about 160 ps per inch, so, for example, if a signal transition time is 1.6 ns then a trace longer than 5 inches should be considered as a transmission line.

PC boards should be developed with transmission line impedances as constant and controlled as possible and data/clock lines or traces should be of equal length.

DECOUPLING FOR QR0001

Generally speaking, the decoupling method can be divided into two stages on the board level design: power entry decoupling and circuit (IC) level decoupling. With both methods, the decoupling capacitors deliver a quick response and large burst of stable energy without generating a noise pulse and voltage droop. They also isolate noise from power supply.

In a typical power distribution system, the power entry capacitor is a relatively large-valued capacitor near the power entry point on the printed circuit board. The purposes of the power entry decoupling capacitors are to: (1) Prevent transmission of PCB-generated noise to the backplane or motherboard and power supply. (2) Supply power so that the voltage at the PCB power entry point is maintained at V_{CC} (usually 5 VDC). (3) Suppress power supply backplane ringing resulting from inductance of the power supply and backplane.

In a high speed digital system, the circuit (IC) level decoupling capacitor is primarily used to eliminate high speed transient switching noise and to minimize troublesome high frequency clock harmonic components. Reducing the transient switching ''noise'' requires low inherent inductance within the decoupling capacitors and effective board design. When a capacitor is mounted on a board, the lead length and board traces (device V_{CC} to capacitor to ground) are a major source of inductance. This inductance must be minimized to obtain good decoupling performance under high speed transient conditions.

TABLE I. QR0001 I_{CC} Measurement Result for One Node Ring
(Test condition at room temperature and $V_{CC} = 5V$)

TXCLK/RXCLK/ RGCLK	I_{CC} at TXS_STREAM_1	I_{CC} at TXS_STREAM_2	I_{CC} at TXS_STREAM_3
15 MHz	116 mA	157 mA	187 mA
20 MHz	131 mA	185 mA	224 mA
30 MHz	166 mA	237 mA	294 mA
40 MHz	202 mA*	279 mA	371 mA**
50 MHz	235 mA	322 mA	495 mA

* 202 mA = 122 mA ($I_{CC}1$) + 14 mA ($I_{CC}2$) + 42 mA ($I_{CC}3$) + 24 mA ($I_{CC}4$)

** 371 mA = 230 mA ($I_{CC}1$) + 69 mA($I_{CC}2$) + 48 mA ($I_{CC}3$) + 24 mA ($I_{CC}4$)

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TEST RESULTS

All tests done with QR0001 33 MHz silicon. The results shown in Table II were obtained using a bench test board that was set-up for a one node ring test. The bench test board had the following specifications:

Layers: 8
Board Material: FR-4
Impedance Matched: 50Ω ±10%
Trace Length Matched: Yes
Thickness: 90 Mil.
Gold Body Board: Yes

The board had a common ground plane for all QR0001 GND pins. There were four separate power supply V_{CC} trace islands for the $V_{CC}1/V_{CC}2/V_{CC}3/V_{CC}4$ pins. The downstream ring ports were directly connected to the upstream ring ports (DnSS± to UpSS±). Ring traces were of equal length and surrounded by ground traces. The seven differential pair termination resistors (100Ω) were put as close as possible to the UpSS± pins.

For decoupling, 1.0 μF and 4.7 μF tantalum capacitors were used as the board level power entry capacitors at all of the four power islands input locations. MLC (multilayer ceramic) chip capacitors with values of 0.01 μF, 0.001 μF, and 82 pF were used for the V_{CC} pins.

The worst case working clock frequency was 45.4 MHz, this was with the most capacitors. The best case for STREAM__2 was 46.3 MHz with four fewer decoupling capacitors. The best overall performance in this test came from using 20 capacitors with values given in row 2. It is possible to lower total number of capacitors in region 1 and 2 without adversely affecting performance. For example, two of the 0.001 μF could be removed from each region.

TABLE II. QR0001 Working Frequency Relationship with Decoupling Capacitors

Total Cap Count		Decoupling Capacitor Set-Up	TXS_STREAM_1	TXS_STREAM_2	TXS_STREAM_3
20	8	Four pairs of $V_{CC}1$/GND1 pins with both .01 μF + .001 μF	47.2 MHz (21.2 ns)	45.6 MHz (21.9 ns)	45.8 MHz (21.8 ns)
	6	Six pairs of $V_{CC}2$/GND2 pins with one .001 μF			
	4	Two pairs of $V_{CC}3$/GND3 pins with both 82 pF + .001 μF			
	2	One pair of $V_{CC}4$/GND4 pin with both 82 pF + .001 μF			
20	8	Four pairs of $V_{CC}1$/GND1 pins with both .01 μF + .001 μF	48.1 MHz (20.8 ns)	46.1 MHz (21.7 ns)	46.5MHz (21.5 ns)
	6	Six pairs of $V_{CC}2$/GND2 pins with one .001 μF			
	4	Two pairs of $V_{CC}3$/GND3 pins with both 82 pF + .001 μF			
	2	One pair of $V_{CC}4$/GND4 pin with both .01 μF + .001 μF			
22	8	Four pairs of $V_{CC}1$/GND1 pins with both .01 μF + .001 μF	47.8 MHz (20.9 ns)	46.3 MHz (21.6 ns)	46.7 MHz (21.4 ns)
	4	Four pairs fo $V_{CC}2$/GND2 pins with one .001 μF			
	4	Two pairs of $V_{CC}2$ (29,69)/GND2 (27,66) pins with both .01 μF + .001 μF			
	4	Two pairs of $V_{CC}3$/GND3 pins with both 82 pF + .001 μF			
	2	One pair of $V_{CC}4$/GND4 pin with both .01 μF + .001 μF			
22	8	Four pairs of $V_{CC}1$/GND1 pins with both .01 μF + .001 μF	47.4 MHz (21.1 ns)	45.4 MHz (22 ns)	46.7 MHz (21.4 ns)
	4	Four pairs fo $V_{CC}2$/GND2 pins with one .001 μF			
	4	Two pairs of $V_{CC}2$ (29,69)/GND2 (27,66) pins with both .01 μF + .001 μF			
	4	Two pairs of $V_{CC}3$/GND3 pins with both 270 pF + .001 μF			
	2	One pair of $V_{CC}4$/GND4 pin with both .01 μF + .001 μF			
26	8	Four pairs of $V_{CC}1$/GND1 pins with both .01 μF + .001 μF	48.1 MHz (20.8 ns)	45.4 MHz (22 ns)	45.8 MHz (21.8 ns)
	12	Six pairs of $V_{CC}2$/GND2 pins with both .01 μF + .001 μF			
	4	Two pairs of $V_{CC}3$/GND3 pins with both 82 pF + .001 μF			
	2	One pair of $V_{CC}4$/GND4 pin with both .01 μF + .001 μF			

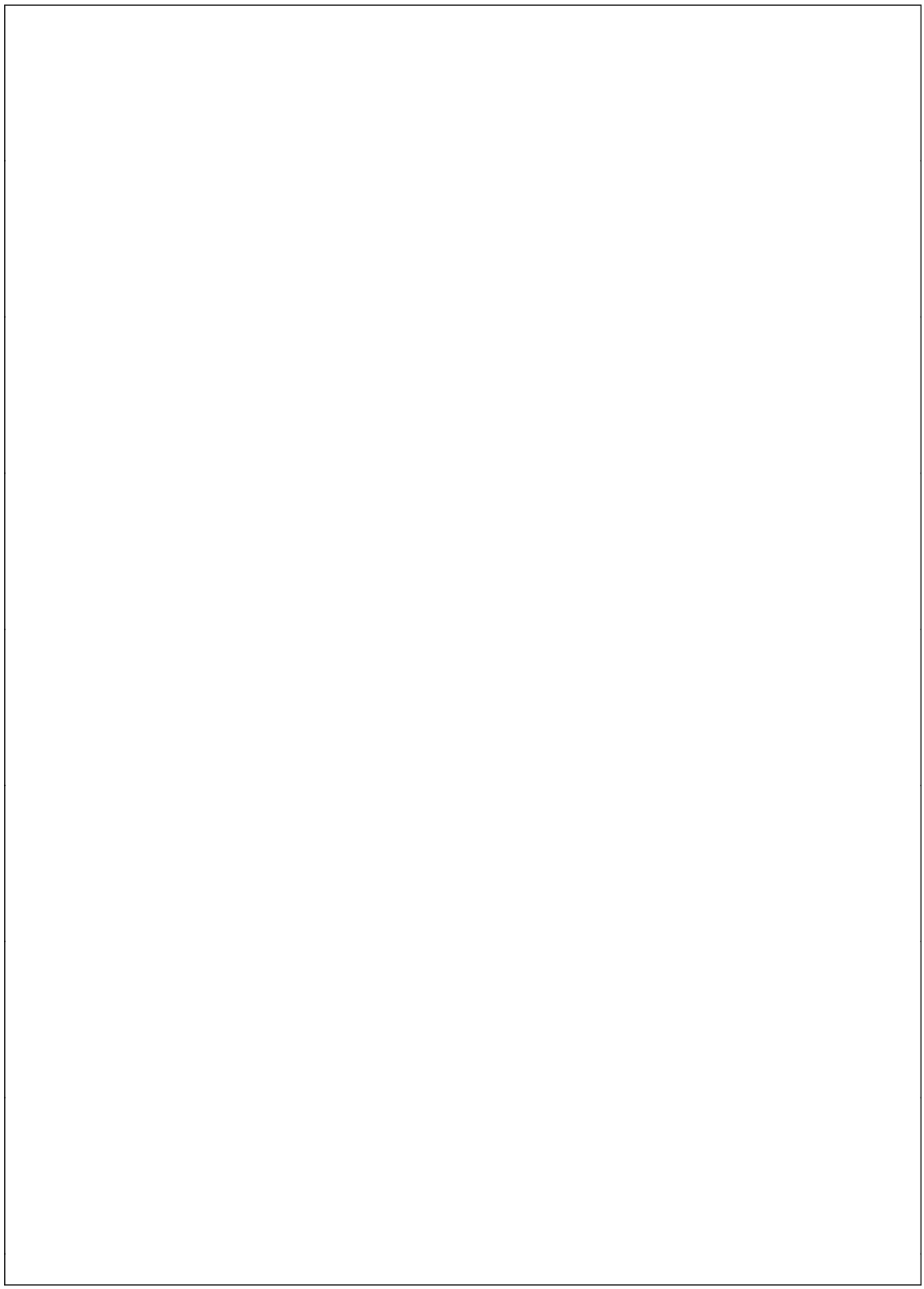
Note 1: Test condition at room temperature and V_{CC} = 5V.

Note 2: Refer to QuickRing™ application note of ''QR0001 Bench Test Methods and Practice''.

(1). TXS_STREAM_1: A simple counter pattern increased by one from 00000000 (Hex) to 0000008D (Hex).

(2). TXS_STREAM_2: The worst case data pattern.

(3). TXS_STREAM_3: The maximum power dissipation data pattern.



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