High Frequency QuickRing™ Interface Design

National Semiconductor
Application Note 943
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June 1994

QuickRing is the first product to use IEEE P1596.3 Low Voltage Differential Signaling (LVDS) for very high frequency data transfers. This signaling standard was created by the Scalable Coherent Interface (SCI) Extensions to enable low cost, standard process Integrated Circuits, to communicate at Giga Bytes per second. Since both the driver and receiver are low power, they are integrated directly onto the QuickRing part. The constant current LVDS driver allows for power consumption to be independent of frequency. The LVDS is also independent of power supply voltage because the voltage levels are low enough to be operated from a 2.5V power supply. This means that future low voltage parts will interoperate with the current 5V part.

The differential signals are created from two single ended signals as pictured in *Figure 1*. The VoA is commonly referred to as the ''true'' signal and the VoB as the complement. The equation given for the differential signal shows that Vod is derived from subtracting the complement from the true.

LVDS ADVANTAGES

The advantage to using low voltage swing, differential signals for high speed signaling are threefold. First, the signal is independent of common mode noise such as that created by power supply, ground bounce and externally coupled noise. The transmitted true signal does not rely on ground as a reference voltage, but carries a reference voltage, the complement, along with it to the signal destination. The reference is stable with respect to the true because it is generated from the same silicon under the same conditions of power supply and temperature and ideally travels an equivalent parallel electrical path. Common mode noise has little affect because the true and complement experience it simultaneously. The difference between the two signals is unaffected by the common noise and remains at a near constant amplitude throughout the transmission.

Second, the equal and opposite transitioning signals create equal and opposite electro-magnetic fields. These fields have a canceling affect on each other as they travel the electrical path to the receiver. Therefore, crosstalk and radiated signals are also cancelled. As a result, there is little noise generated.

The third advantage is the 400 mV, low current, signal swing causes very little electrical disturbance to power supplies and adjacent signal lines. This, along with the equal and opposite transitions, reduces the crosstalk problem for transmitted signals. In high frequency design, this is important to economically fabricating the transmission media. None the less, there are hints and guidelines that should be followed to make the reliable, economic transfer of signals occur.

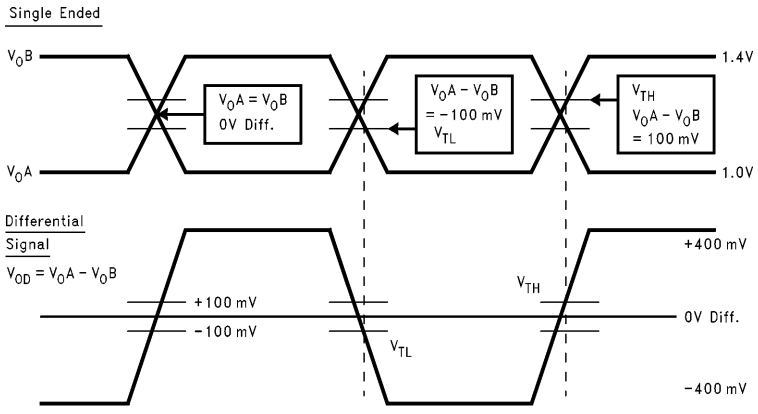

FIGURE 1. QuickRing LVDS Signals

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  RRD-B30M75/Printed in U. S. A.

EXTRA ADVANTAGES

There are some other features to QuickRing's LVDS that have been designed to accommodate transmitting high speed data. *Figure 2* shows how the high speed differential ring signals are connected point to point to form a ring. There are 6 data channels and 1 clock. The differential ring clock is operated at a maximum frequency of 50 MHz. During this 20 ns period, 7 subsymbols (SS) are sent over the 6 differential ring data channels. The sub-symbols each have a 2.86 ns bit width (20/7). This is 350 MBaud. However, since every transition of the signal is used, the maximum frequency is 175 MHz, and that only occurs when a differential channel is switching high and low states every transition. *Figure 3* shows how the UpCLK is used in conjunction with the PLL. The low to high transition triggers the PLL and then it creates the 7 sample edges from precision delay lines that capture the data. This data capture process is completely scalable, so the RGCLK can be operated anywhere between 25 MHz and 50 MHz. Since the same clock transmits the data and then travels in parallel to be used to generate receiver sample edges, the clock jitter problem is minimized because the data has approximately the same jitter.

LVDS TRANSMISSION

LVDS can be transmitted on PCB, cable, flex, or any impedance controlled conductor.

DESIGN CRITERIA

There are 3 electrical design criteria for a high speed QuickRing interconnect. They are;

1. Minimizing the skew between differential pairs and inside each pair
2. Maintaining signal transition integrity, and
3. Supplying adequate differential voltage amplitude to the receiver.

The quality of the interconnect media is measured using these 3 critera. It will affect how far and fast the signal can be transported. The correlation between the quality of the media, the transmitted distance, and the frequency of operation should be understood for best price/performance tradeoffs. Not an electrical criteria, but the applications for using twisted ring topology for the interconnect will be discussed in relation to the electrical criteria. Since these same criteria apply to both internal and external interconnect, they will be addressed simultaneously. When there is a difference in the criteria between the internal and external, such as EMI, then it will be highlighted.

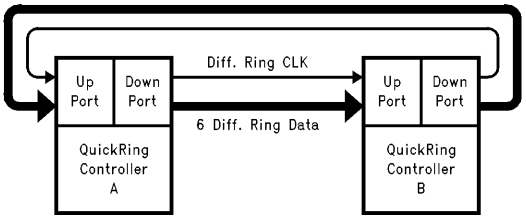

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FIGURE 2. The Simplest Ring, 2 Nodes

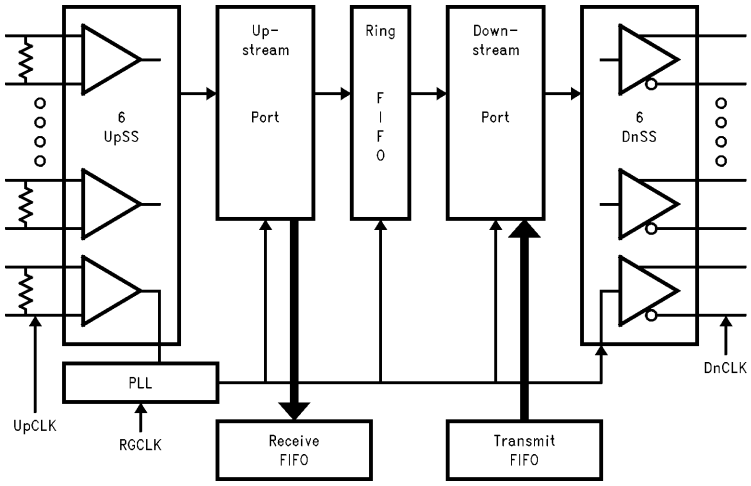

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FIGURE 3. The UpSS and UpCLK Signal Pairs Must Be Parallel Terminated with 100Ω Surface Mount Resistors

MINIMIZING THE SKEW

There are 2 types of skew that must be accommodated in the design. The skew between the pairs and inside the pairs are the critical design criteria. The skew between pairs will be called channel skew. The skew inside pairs will be called the differential skew.

First, the skew between the 7 parallel signal pairs or channel skew *(Figure 5).* The maximum 350 MBaud signals dictate a bit width of about 2.86 ns. The QR UpPort needs 2.36 ns of this bit width (including transitions) to successfully sample the value for each subsymbol. This allows for a total skew budget of 0.5 ns. The interconnect between DnPort and UpPort should be limited to 0.35 ns to provide 150 ps skew margin. This 350 ps is the total allowed for PCB traces, connectors, headers, cables and all other media used in the signal path. When a lower ring frequency is used, the allowed skew budget scales up. That means about 15% of bit width can be budgeted for skew.

In the case of internal connectors, the card to card connector should present very little skew due to the short length. That allows the PCB to use more of the budget. The twisted ring topology may use a bypass trace, pictured in *Figure 4*, as the path on the opposite side of the board from a QR device. Due to 4 layer board construction, this trace is typically implemented in a rainbow pattern which has the inside arc shorter than the outside arc. This eliminates the use of vias for equal length traces. This is an unavoidable skew on the PCB but can be done in less than 200 ps.

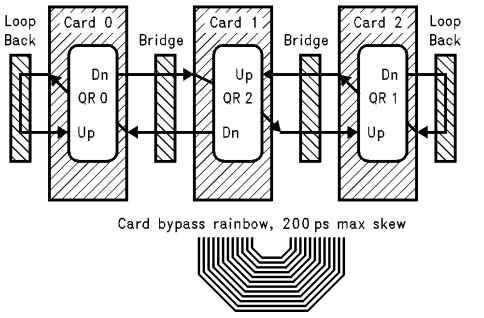

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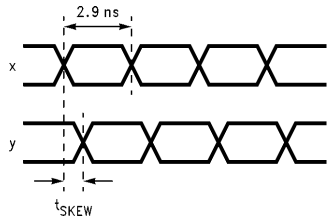
FIGURE 4. Twisted Ring Topology Eliminates Long Loop Back to Complete the Ring.



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Note: x and y are any two signals, including clock.

FIGURE 5. Channel Skew

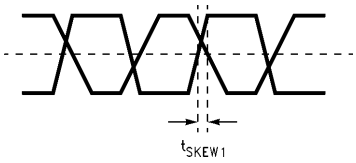
The amount of skew in an external cable depends on the type of cable and termination of cable to connector. A twisted pair cable may have more skew per unit length than a parallel pair due to inconsistency of twists. The connector termination can be one of 3 types, insulation displacement connector (IDC), soldered, or welded. The skew will be less controlled on IDC and best on the welded.

The implementation of an external ring can be in the twisted ring or straight ring topology. In a straight ring, the PCB UpPort and DnPort are the only PCB traces needed. There is no twisted ring bypass rainbow. This means that more skew budget is available for the cable. In the cable twisted ring, a bypass must be incorporated into each node. The reason for an external twisted ring is that it can look like a daisy chain to the user. There are two 7 channel links in one cable and boxes can be linked in a series. The ring is completed by loop backs. However, the twisted ring will have to use some of the total skew budget in the bypass implementation because skew in each cable adds into budget. This will limit the total node to node separation because skew in each cable adds into budget. This distance is limited in the twisted ring by the fact that 2 bridging cables have to be traversed by the signal.

TABLE I. A Sample Skew Budget for External Cable Connector

Signal Path	From	To	Skew Max
PCB	Driver Pins	Input to First Connector	40 ps
Connector	Input to First Connector	Output from First Connector	10 ps
Cable	Output from First Connector	Input to Second Connector	250 ps
Connector	Input to Second Connector	Output from Second Connector	10 ps
PCB	Output from Second Connector	Receiver Pins	40 ps
			Total = 350 ps

The skew within a pair needs to be controlled because of the Electro-Magnetic Interference (EMI) considerations, and how it affects the differential edge placement. The simultaneous and opposite transitions on paths within a pair create equal and opposing electromagnetic fields (emf) as the signal propagates. These emf, the source of EMI, serve to cancel each other thereby reducing EMI. The skew within a pair should be controlled so that the single ended emf remain temporally and spatially relevant to each other. This proximity promotes the canceling effect. Controlling this skew within a pair means the signal paths must be equal length, and have the impedance mismatches at electrically equal lengths. The mismatches occur at vias, connectors, headers, and even bends in a trace. Ideally, the differential pair of traces should be identical in placement of these mismatches and parallel in routing. In practice, automatic routers do not run parallel traces but they will do equal length. The auto routers usually result in one line being serpintine to get it equal length to the other. This violates the parallel principle. However, this layout has been tested and lab results are better than expected. The serpintine traces do not inhibit the differential signals at the frequencies used in QuickRing, 180 MHz maximum. The impedance mismatches that are in the paths; switches, connectors, etc., are at equal lengths. So, even though not parallel, this follows good design principles.



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Note: Any two complementary single ended signals.

FIGURE 6. Differential Skew

MAINTAINING SIGNAL TRANSITION INTEGRITY

The second subject is maintaining signal integrity. This means that the differential 0V crossing is singular, and at a constant slew rate, for each changing logical value. As shown in *Figure 1,* the differential signal makes a 0V crossing when the logical value changes. The receiver is specified to sense this transition somewhere between the ±100 mV values, typically at ±35 mV. The differential receiver works best when this signal passes unambiguously through the threshold region with a constant slew rate. The differential termination is the most important part of the physical transmission path design for maintaining the transition integrity.

Ideally, the differential termination is at the extreme end, just before receiver input, of the unidirectional transmission line. By perfectly matching the differential impedance, the reflection coefficient can be reduced to zero. This implies putting the termination resistor on the QuickRing silicon would be the best solution. However, the cost of doing this is prohibitive, but the alternative is very satisfactory. The alternative puts the external surface mount resistor as close to the ±UpCLK and ±UpSS[ ] pins as possible. *Figure 7* shows how this is an acceptable alternative.

Either position in *Figure 7* is a good place to put the termination resistance, R_t. In both cases, R_t should still be as close to the pins as possible. In the *Figure 7(b)* case, the transmission path between the termination resistor and receiver input consists of 5 segments.

1. The remaining trace to the pin solder pad,
2. package pin,
3. lead frame,
4. bond wire,
5. and bonding pad.

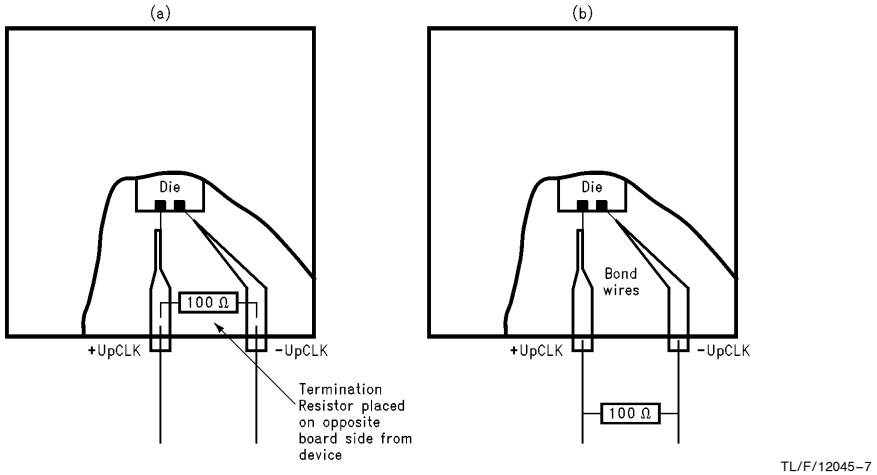

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FIGURE 7. Two Different Placements for Termination Resistor

The path is then terminated in the high impedance receiver input. This high impedance input causes a reflection coefficient of nearly 1 which would make reflections a problem if the electrical distance between the termination and receiver input were not small which will be explained later. Since R_t carries all the current, the path reactive parasitic inductance has little effect on the signal quality. This is because the Ldi/dt portion of the Ldi/dt relation that caused voltage variation is small. The package parasitic capacitance is very small and has less impact on the signal than the inductance.

Figure 7(a) presents a different transmission path analysis. Since the terminating resistor is after the traces going to the receiver input, the 5 segments act as a stub on the transmission lines. The stubs present a minor impedance discontinuity at that point due to the capacitive loading effect. The shorter the stubs, the less the loading and less signal distortion. As mentioned before, these discontinuities in impedance should be at equal electrical distances in the differential signal path so they distort the signal as little as possible.

There are drawbacks to each of these schemes. The *Figure 7(a)* scheme means putting additional vias in the path to get to the other side of the card. The *Figure 7(b)* scheme allows for the unterminated path from R_t to receiver input to exist where reflections could be a problem.

These termination schemes eliminate reflections resulting from transition energy hitting the receiver high impedance input structure, and then bouncing back into the transmission path. It is these reflections that can cause unequal transitions on each of the single ended signals. This may result in a differential signal that has poor quality transitions.

Small electrical distance in both schemes between the terminating resistor and pins is important. It means the signal delay due to this path should be less than ¼ of the transition time. The minimum transition time for QuickRings LVDS is 300 ps. At the average 150 ps/in. signal speed, the termination resistor should be no more than ½ in. from the receiver input on the die. The corner pins on the 160-pin PQFP are about 0.4 in. from the die. It is essential to position the termination for UpSS ± (0) and UpSS ± (1) as close to the pins as possible.

DIFFERENTIAL VOLTAGE AMPLITUDE

The third criteria is supplying good differential amplitude to the receiver input. (Even though the receiver is specified to ± 100 mV receiver threshold, it works best with an overdrive input voltage.) The receiver skew performance varies with the slew rate and amplitude of the input signals. To minimize the channel and differential skew, the amplitude for all 6 signals should be as nearly equal as possible. To achieve this, they must be carried on as identical transmission path as possible. This will ensure the amplitude on all lines is nearly equal. By doing this, the receiver skew should be minimized.

High frequency board layout is an art as much as it is a science. The variables are large and the interaction critical. For this reason, I have given a list of guide lines from which to begin. The QuickRing applications team is experimenting with a number of high frequency layouts. When you are ready for design, please contact the group to get the latest advice on how to proceed. There will be gerber files available for a standard PCB layout that has been used on the System Development Card.

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