Simplified Intelligent Port Design Using The 74ACT1284

National Semiconductor
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INTRODUCTION

Until recently a standard for parallel port data transfer has been missing in the industry. IEEE 1284, approved by the IEEE in March 1994, addresses the lack of a parallel port specification. The standard, entitled **"A Standard Signaling Method for a Bi-Directional Parallel Peripheral Interface for Personal Computers"**, will eventually displace the antiquated, slow, quasi-bi-directional method of transferring data between host and peripheral. Described within the standard is a high speed, fully interlocked bi-directional peripheral connectivity port which greatly improves performance while maintaining backward compatibility with systems which are IEEE 1284 non-compliant.

There are five operational modes described in the standard. The two truly bi-directional modes, the EPP (enhanced parallel port) and the ECP (extended capabilities port) provide for the greatest increase in port performance. The EPP and ECP modes allow half duplex data communication between the host and its peripheral at speeds greater than 100 times that of the SPP (standard parallel port). This translates to a remarkable speed upgrade of more than 2 Mbytes/sec. However, in order to realize the tremendous increase in speed and the advantages of true bi-directionality made possible by IEEE 1284, system designers must pay particular attention to the port interface circuitry.

There are key areas one needs to be concerned with when designing IEEE 1284 compliant systems. Of primary importance is ensuring data integrity at the high data rates made possible by the new standard. Another important consideration is the limitations peripheral ASIC controllers may have when attempting to directly drive the IEEE 1284 specified 10 meter cable lengths. These things serve to underscore the fact that port I/O drive and receive components must possess the capability for maintaining IEEE 1284 specified signal levels and timing.

NSC 74ACT1284

The 74ACT1284 provides the necessary low impedance drive for transmission of the control and data signals necessary for reliable intelligent peripheral and host interface communication. The device was developed in response to the IEEE 1284 standard and an anticipated expansion in the intelligent peripheral market. National Semiconductor design philosophy for the 74ACT1284 was to accommodate the IEEE 1284 standard and to provide system manufacturers a solution to the problems associated with using ASICs to drive the high bandwidth IEEE 1284 port. The 74ACT1284 meets or exceeds all IEEE 1284 specified parameters for driving and receiving signals over an intelligent peripheral interface port and addresses such critical design areas as high speed parallel port handshaking, low impedance cable driving, and increased ESD protection.

The 74ACT1284 device functions as a 7-bit bus transceiver designed for asynchronous two-way communication. As shown in the logic diagram, *Figure 1*, the IC contains four non-inverting bi-directional buffers and three non-inverting unidirectional buffers. The B port buffers can be configured either as open Drain or high drive outputs. The HD input pin enables the B ports to switch from open Drain to a high drive totem pole configuration, capable of sourcing and sinking 14 mA on all seven buffers. The DIR input determines the direction of data flow on the bi-directional buffers. The DIR control function implementation helps to minimize external timing requirements.

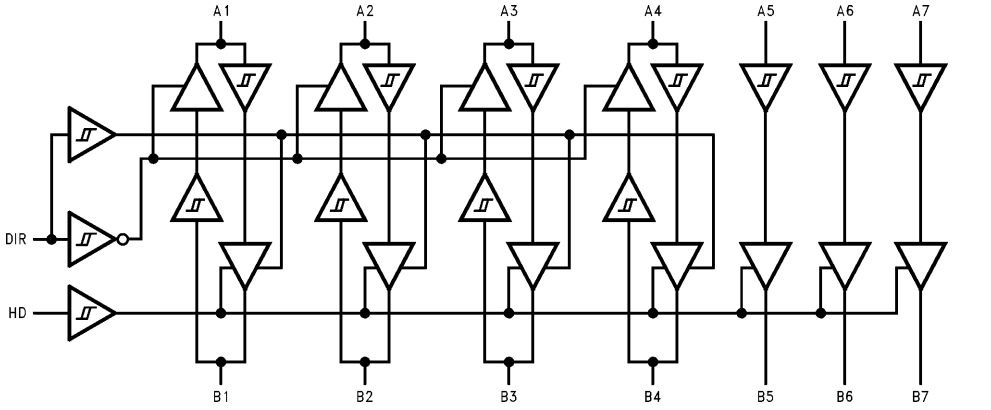

FIGURE 1. 74ACT1284 Logic Diagram

  RRD-B30M105/Printed in U. S. A.

The NSC 74ACT1284 gives the designer significant advantage when designing the port interface circuitry. System manufacturers who design to the IEEE 1284 standard using an ASIC controller to drive the parallel port directly may encounter problems. ASIC controller power and drive constraints become evident when attempting to drive lengthy, highly capacitive, low impedance cables. Consequently, IEEE 1284 specifications may not be met. When using the 74ACT1284, designers have an integrated solution which ensures that critical port interface signal properties are preserved.

Some advantages for using the 74ACT1284 at an IEEE 1284 compliant port are the following:

- Full IEEE 1284 specification compliance
- Provides a solution for easing controller power and drive design constraints
- Bi-directional Port buffering with input hysteresis
- Optimized printed circuit layout through localization of port drive circuitry
- Advanced CMOS technology for low power consumption
- Guaranteed class 3 ESD performance for protection of sensitive I/O signal controllers
- TTL and CMOS compatible input thresholds

HOST-SIDE APPLICATION OF THE 74ACT1284

Perhaps it is more likely that the 74ACT1284 function will be utilized at the intelligent peripheral port, however, there are benefits for its use at both the host and peripheral port interfaces. There are several important advantages for using the 74ACT1284 at the host as well as the peripheral. They are as follows: 1) adequate cable drive over the required IEEE 1284 data bandwidth 2) increased port ESD protection and most importantly 3) the assurance of full IEEE 1284 compliance.

An application example for using the 74ACT1284 at the host in ECP mode appears in *Figure 2*. In the figure, a generic host controller is shown with three 74ACT1284s (shown as one block) placed at the I/O port. The diagram denotes compatibility mode signals, with ECP mode signals shown in parenthesis, interconnecting the host and peripheral. 74ACT1284 devices are used here to drive and buffer signals between host and peripheral, insuring signal integrity and protection of the host controller from damage caused by noise spikes should the peripheral be powered down or arbitrarily disconnected.

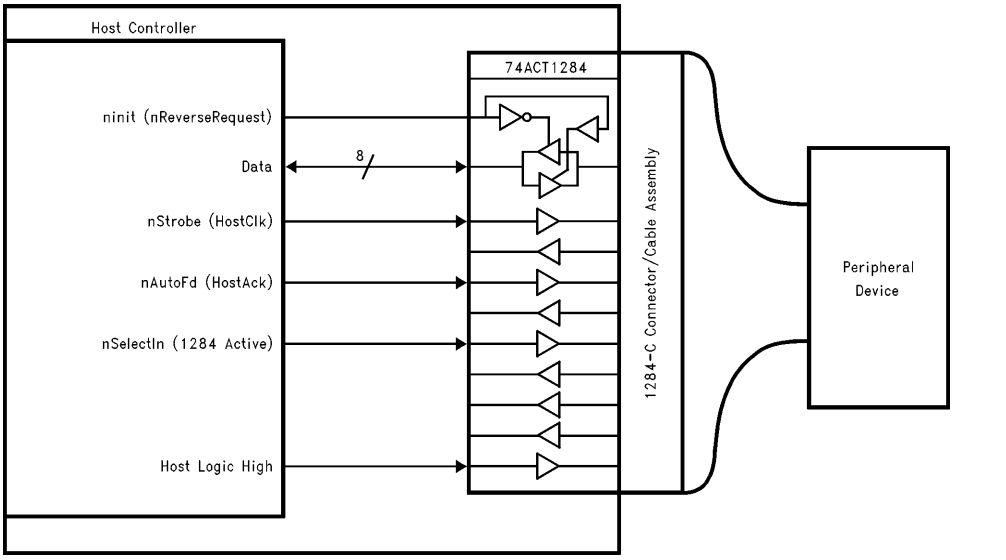

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FIGURE 2. Host-Side 74ACT1284 Application

PERIPHERAL-SIDE APPLICATION OF THE 74ACT1284

Similar to *Figure 2*, *Figure 3* shows a diagram of peripheral-side application of the 74ACT1284. Both *Figure 2* and *Figure 3* application examples depict the peripheral and host controller direct I/O port interface portion of the system only.

Register names and hooks will vary depending on controller design, therefore, it is likely that not all register connections will be shown in the figures. We would like to re-emphasize that buffering of **all** signals at the port is the best way of assuring system functionality and reliability.

The peripheral can take many forms and still support IEEE 1284. Other devices that use the new IEEE 1284 standard are scanners, tape backup, CD ROM and network/LAN adapters.

For clarity, *Figure 4* has been included to show the signal connections which comprise the entire system. It is beyond the scope of this paper to assume how all signals might be used to and from the controller registers. The examples show basic IEEE 1284 control signal names. There may be other signals used which are not shown in the examples.

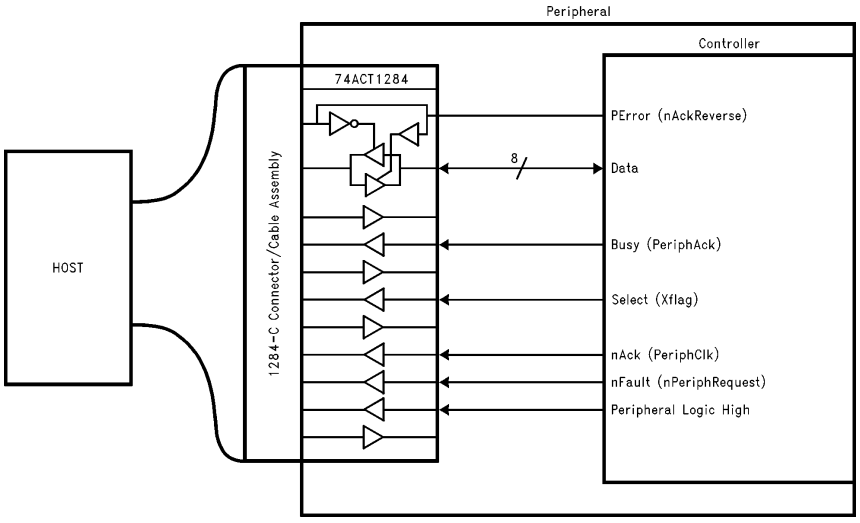

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FIGURE 3. Peripheral-Side 74ACT1284 Application

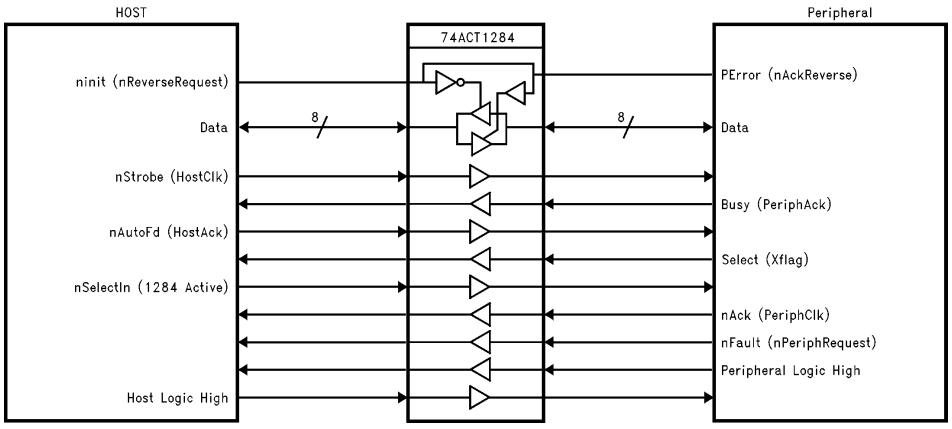

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FIGURE 4. Host/Peripheral System Signals

SUMMARY

With the advent of IEEE 1284, system designers are looking at a new horizon with which to implement the information exchange between computer and peripheral. The proliferation of high performance computing systems coupled with IEEE 1284 compliant intelligent peripheral devices will serve to outmode the old methods of transporting data via the parallel port and its external support medium.

For new IEEE 1284 compliant designs to reach their market in a shorter time, solutions which enhance the design cycle through simplification are usually a good alternative. The NSC 74ACT1284 was developed to provide a packaged solution to the design of the bus interface in IEEE 1284 compliant systems. It is a device intended to alleviate the problems associated with IEEE 1284 specification conformance and can be thought of as a drop-in stage for ensurance of IEEE 1284 compliance.

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