CMOS 300 Baud Modem

National Semiconductor
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INTRODUCTION

The advent of low cost microprocessor based systems has created a strong demand for low cost, reliable means of data communication via the dial-up telephone network. The most widespread means for this task is the Bell 103 type modem, which has become the de facto standard of low speed modems. This type of modem uses frequency shift keying (FSK) to modulate binary data asynchronously at speeds up to 300 baud.

The success of this type of modem, despite its modest transmission speed, is largely due to its ability to provide full duplex data transmission at low error rates even with unconditioned telephone lines. It also has a significant cost advantage over the other types of modems available today. Advances in CMOS and circuit design technology have made possible the 74VHC942—a high performance, low power, Bell 103 compatible single chip modem. This chip combines both digital and linear circuitry to bring the benefits of system level integration to modem and system designers.

(The 74VHC942/943 devices are direct pin, function and spec replacements for the MM74HC942/943 devices.)

THE PROCESS—microCMOS

The chip was designed with National's double poly CMOS (microCMOS) process used extensively for its line of PCM CODECs and filters. This is a self-aligned, silicon gate CMOS process with two layers of polysilicon, one of which is primarily used for gates of the MOS transistors. Thus there are three layers of interconnect available (two polysilicon and one metal layer) making possible a very dense layout.

The two polysilicon layers also offer a near perfect capacitor structure which is used to advantage in the linear portions of the chip. The self-aligned silicon gate P and N-channel MOSFETs combine high gain with minimal parasitic gate-to-drain overlap capacitance, facilitating the design of operational amplifiers with high gain-bandwidth product and excellent dynamic range.

CHIP ARCHITECTURE

The chip architecture was arrived at after critically evaluating several trial system partitionings of the Bell 103 type data set. The overriding goal was to integrate as much of the function as possible without sacrificing versatility and cost effectiveness in new applications. The resulting chip architecture reflects this philosophy. Since the majority of users of this device would probably be digital designers unfamiliar with filter design and analog signal processing, inclusion of these functions was thus mandatory. The precision filters needed for a high performance modem also make discrete implementations expensive. On the other hand, the majority of new systems will typically include a microprocessor which is quite capable of handling the channel establishment protocol. Besides, different systems may require different protocols. Circuitry for this task was therefore omitted.

A block diagram illustrating the chip architecture is shown in *Figure 1*. The on-chip line driver and line hybrid greatly simplify interfacing to the phone line by saving two external op amps. The output of the line hybrid, which is used to reduce

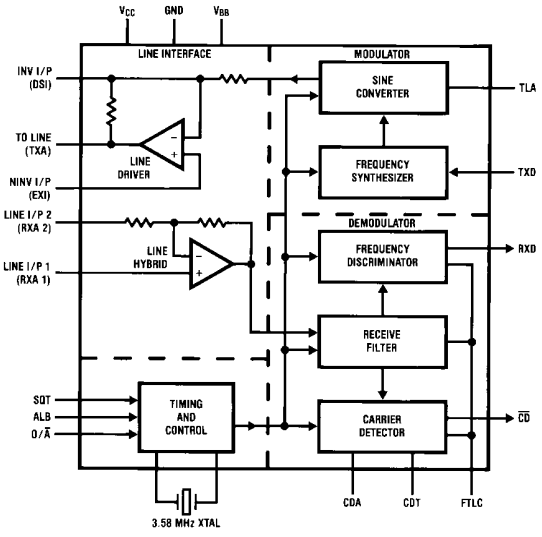

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FIGURE 1. Chip Architecture of the 74VHC942

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the effect of the local transmit signal on the received signal, goes to a programmable receive bandpass filter. This filter improves the signal-to-noise ratio at the input of the frequency discriminator, which performs the actual FSK demodulation. The output of the receive filter is also monitored by a carrier detector which compares the amplitude of the received signal to an externally adjustable threshold level.

The modulator consists of a frequency synthesizer which generates a clock at a frequency determined by the TXD (transmit data) and O/$\overline{A}$ (originate/answer) inputs. This is subsequently shaped by the sine converter into the final modulated transmit carrier signal.

All internal clocks and control signals are derived from an on-chip oscillator operating from a common 3.58 MHz TV crystal. On-chip control logic allows the modem to be set to answer or originate mode operation, or to an analog loopback mode via the O/$\overline{A}$ and ALB inputs respectively. The line driver can be squelched via the SQT input, which typically occurs during the channel establishment sequence.

Another feature of this design not obvious from the block diagram of *Figure 1* is that the chip can be powered down by asserting the ALB and SQT inputs simultaneously, a condition that does not occur during normal operation. This cuts power consumption to typically under 50 μA, making it very suitable for battery operation.

DEMODULATOR

Receive Filter

This is a nine pole, switched capacitor[1,2] bandpass filter. It is programmable by internal logic to one of two passbands, corresponding to originate or answer mode operation. The measured frequency response of the filter is shown in *Figure 2.* It shows that better than 60 dB of adjacent channel rejection has been achieved. Note also the deep notches at the frequencies of the locally transmitted tone pair.

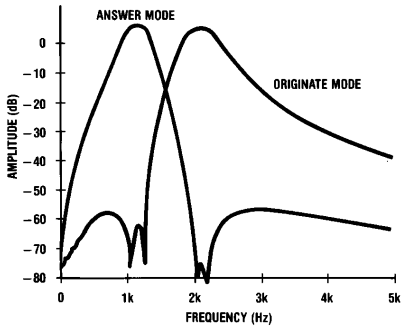

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FIGURE 2. Measured Frequency Response of the Receive Filter

A key design goal was to minimize the delay distortion of the filter. This has also been met as evidenced by the delay response curves shown in *Figures 3a* and *3b*. These curves have been normalized to the delays at 1170 Hz and 2125 Hz respectively. They show that the delay distortion in the 1020 Hz to 1320 Hz band is approximately 70 μs, while that in the 1975 Hz to 2275 Hz band is approximately 110 μs. These bands contain all the significant sidebands of a 300 baud FSK signal. The low delay distortion of the receive filter translates directly into low jitter in the demodulated data.

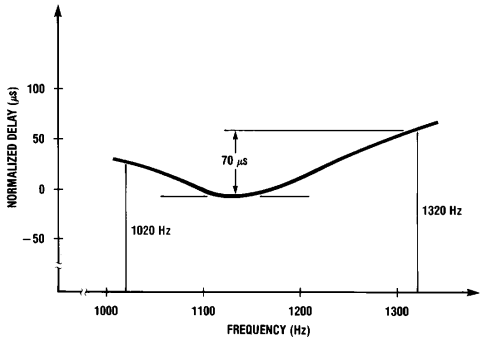

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FIGURE 3a. Normalized Delay Response of the Receive Filter in Answer Mode

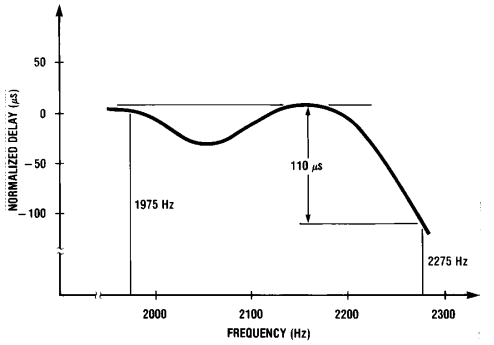

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FIGURE 3b. Normalized Delay Response of the Receive Filter in Originate Mode

An on-chip, second order, real time anti-aliasing filter precedes the receive filter. This masks the sampled data nature of the switched capacitor design from the user, contributing to the ease of use of the chip.

Frequency Discriminator

Referring to *Figure 4*, the filtered receive carrier is first hard limited to remove any residual amplitude modulation. It is then split into two parallel, functionally indentical paths, each consisting of a second order bandpass filter (BPF), a full wave detector and a post detection lowpass filter (LPF).

The bandpass filter in the upper path is tuned to the 'mark' frequency, and that in the lower path to the 'space' frequency. The detectors are full wave rectifier circuits which, together with the post detection filters, measure the energy in the mark and space frequencies. These are compared by the trailing comparator to decide whether a mark or space has been received.

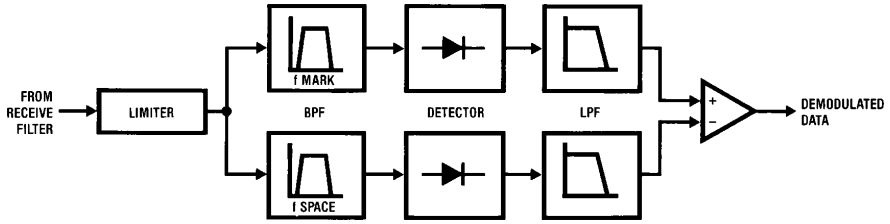

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FIGURE 4. Block Diagram of the Frequency Discriminator

Carrier Detector

The carrier detector compares the output of the receive filter against an externally adjustable threshold voltage. Referring back to *Figure 1*, if the CDA (carrier detect adjust) pin is left floating, the threshold is nominally set to ON at −44 dBm, and OFF at −47 dBm. This can be modified by forcing an external voltage at the CDA input. If the received carrier exceeds the set threshold, the $\overline{CD}$ (carrier detect) output will go low after a preset time delay. This delay is set externally by a timing capacitor connected to the CDT (carrier detect timing) pin.

MODULATOR

As shown in *Figure 5*, the modulator consists of a frequency synthesizer and a sine wave converter. The transmit data (TXD) and mode (O/$\overline{A}$) inputs set the divisor of a dual modulus programmable divider. This produces a clock at sixteen times the frequency of the transmitted tone. This then clocks a four bit counter, whose states represent the voltage levels corresponding to the sixteen time slots in one cycle of a staircase approximated sine wave. The sine ROM decodes the state of the counter and drives a digital-to-analog converter to synthesize the frequency shift keyed sine wave. This modulator design also preserves phase coherence in the transmit carrier across frequency excursions.

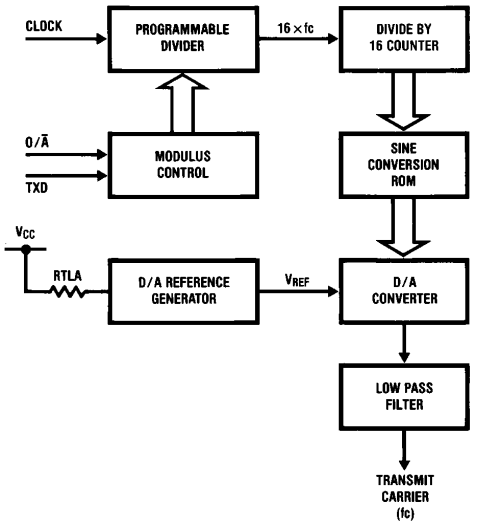

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FIGURE 5. Modulator Block Diagram

The reference voltage for the digital-to-analog converter is derived from a reference generator controlled by an external resistor (RTLA). This allows the transmit signal level to be programmable in accordance with the Universal Service Order Code. This code specifies the programming resistances corresponding to various transmit levels. If no external resistor is connected, the transmit level defaults to −12 dBm.

The synthesized sine wave is filtered by a second order, real time low pass filter to remove spurious harmonics before being fed to the line driver amplifier.

LINE INTERFACE

Line Driver

This is a class A power amplifier designed to drive a 600Ω line through an external 600Ω terminating resistor. With the proper transmit level programming resistor installed, it will drive the line at 0 dBm when operated from ±5V supplies. The quiescent current of the output stage of the driver varies with the programmed transmit level to maximize the efficiency of the amplifier. A class A design was chosen mainly because it can tolerate a wider range of reactive loads.

As shown in *Figure 6*, both inverting and non-inverting inputs of the driver amplifier are accessible externally, making it easy to accommodate an external signal source, such as a tone dialer. An external capacitor can also be connected between the inverting input and the amplifier output to give it a lowpass response.

Line Hybrid

The line hybrid is essentially a difference amplifier which, when connected as shown in *Figure 6*, causes the transmit carrier to appear as common-mode signal and be cancelled from the output. If the termination resistor (R_T) and phone line impedance are perfectly matched, the output of the line hybrid would be just the received carrier. In practice, perfect matching is impossible and 10 dB to 20 dB of transmit carrier rejection is more realistic. The residual is more than adequately rejected by the receive filter of the demodulator.

TIMING AND CONTROL

This includes an oscillator amplifier, divider chain and internal control logic. The oscillator, in conjunction with an external 3.58 MHz TV crystal and the divider chain, provides all the internal clocks for the switched capacitor circuits and the frequency synthesizer. The control logic orchestrates the various operating modes of the chip (e.g., originate, answer or analog loop-back modes).

APPLICATIONS

Figure 7 shows the 74VHC942 in an acoustically coupled modem application. It demonstrates the simplicity of the resulting design and a dramatic reduction in parts count. *Figure 8* shows two typical direct connect modem applications. The simplicity of these circuits is again evident.

The simple power supply requirement (±5V), low power (60 mW when transmitting at −9 dBm, 0.5 mW standby) and low external component count makes the 74VHC942 an efficient implementation of the 300 baud modem function.

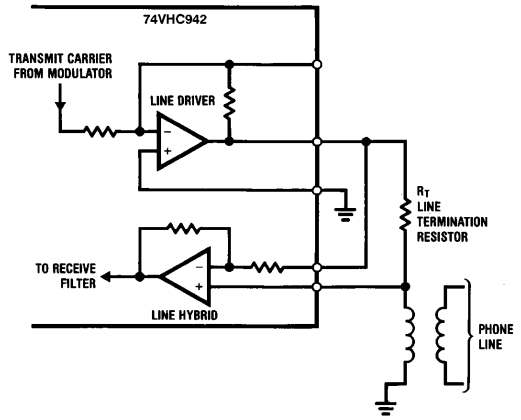

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FIGURE 6. Typical Interface Between the 74VHC942 and the Phone Line

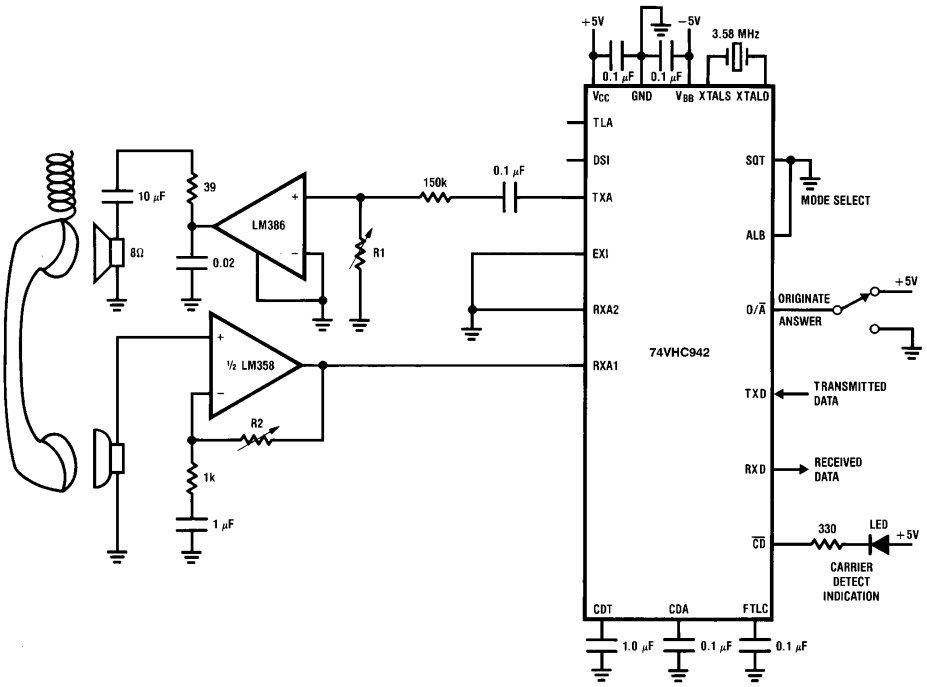

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FIGURE 7. Typical Implementation of an Acoustically Coupled Modem Using the 74VHC942

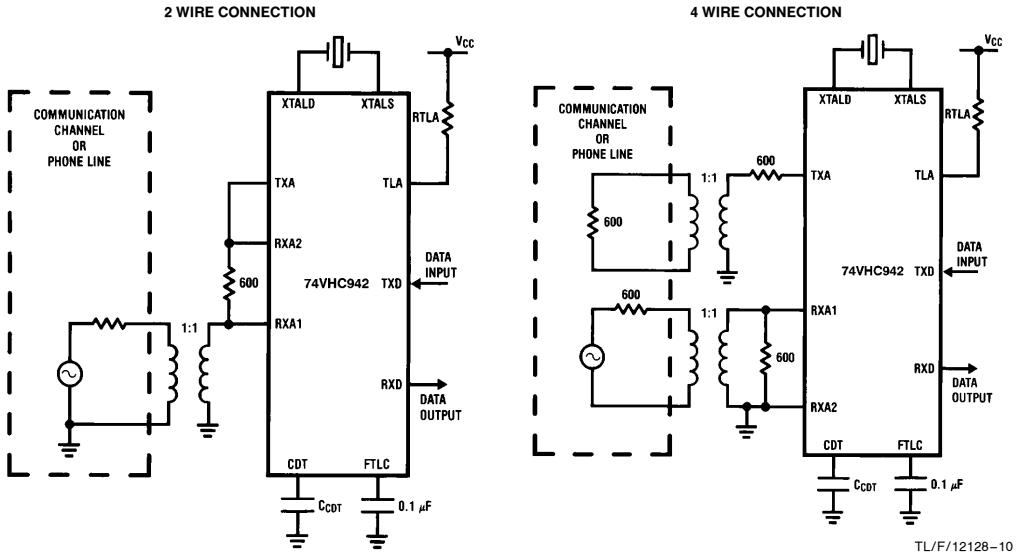

FIGURE 8. Typical Implementations of Direct Connect Modems Using the 74VHC942

SUMMARY

In conclusion, the 74VHC942 integrates the entire data path of a Bell 103 type data set into a 20-pin package with the following features:

- On-chip 9 pole receive filter
- Carrier detector with adjustable threshold
- Analog demodulator with low bit jitter and bias
- Phase coherent modulator with low spurious harmonics
- 600Ω line driver with adjustable transmit level
- On-chip line hybrid
- Full duplex originate or answer mode operation
- Low power operation, power-down mode
- Simple supply requirements (±5V)

REFERENCES

1. J. Caves et al., ''Sampled Analog Filtering using Switched Capacitors as Resistor Equivalents'', *IEEE Journal of Solid State Circuits,* Vol. SC-12, No. 6, Dec. 1977

2. W. Black et al., ''A High Performance Low Power CMOS Channel Filter'', *IEEE Journal of Solid State Circuits,* Vol. SC-15, No. 6, Dec. 1980.

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