# Monolithic Modem Chip Eases $\mu$ P's Phone Access

National Semiconductor Application Note 1015 October 1995



When mated with a handful of CMOS peripheral ICs, a single-chip CMOS modem device allows you to configure simple, inexpensive microprocessor-telephone interface systems with autodial and autoanswer capabilities

Integrated-circuit modems represent the final link in the chain of devices that connect the digital world of the microprocessor bus to the analog world of the telephone line. The 74VHC943 is such an IC; it's a single-chip and -supply Bell-103 modem whose on-chip analog filtering, carrier-detect circuitry and complete hybrid function spare you the complexities of analog design. (The 74VHC942/943 devices are direct pin, function, and spec replacements for the MM74HC942/943 devices.)

Linked with such CMOS peripheral ICs as the NSC858 UART, the TP5088 DTMF dialer and some 74HC logic, the IC allows the design of relatively inexpensive systems that can profit from the intelligence and flexibility of microprocessor control. What's more, its silicon-gate CMOS process suits the IC to applications in portable, battery-powered, remote and harsh-environment systems. With little difficulty, you can easily integrate the IC into an auto-originate, auto answer modem in a  $\mu$ P-based system.

Figure 1 shows the basic functional blocks needed to connect a microprocessor bus to a telephone line. The bus decoders are necessary to assign a unique set of addresses to the UART (universal asynchronous receiver/transmitter) and dialer circuit. The dialer circuit must be bus compatible; i.e., it must be capable of accepting binary inputs from the data bus. The dialer can create pulses, as with rotary-dial phones, or it can send DTMF (dual-tone multifrequency) signals to the central office to establish a connection with another phone.

When the modem operates with the dialer to call another

mode. When the microcomputer receives a call through the modem interface, the ring-indicator circuit serves to interrupt the microprocessor to answer the call automatically. In this case, the modem goes to the answer mode. The block denoted "hook-switch control" is a logic-controlled relay that connects the system to or disconnects it from the phone line.

Protective circuitry is needed to isolate the microcomputer user from hazards (e.g., lightning) transmitted by the phone line and also to protect the public phone system from anything potentially damaging that may emanate from the user's computer equipment. This circuit also provides a 2-sec billing delay when an incoming call is answered. During this period, data may not be sent or received. These protectivecircuitry functions are required (and must be approved) by the FCC (a later section discusses them in detail). The depicted hybrid block performs 2-to-4 wire conversion, necessary because both send and receive frequency bands use the same pair of wires and it's necessary to separate the received signal from the transmitted one.

The next functional block is the modem itself. Modems have only recently become available in integrated-circuit form; two standards currently prevail in the U.S. The 103 standard is for 300-baud, full-duplex communication; the 202 standard allows 1200-baud transmission while receiving at 5 baud, and vice versa. Another standard, the 212, specifies full-duplex, 1200-baud operation.



*I*onolithic Modem Chip Eases  $\mu$ P's Phone Access

AN-101



In addition to the ICs that satisfy U.S. standards, there are integrated-circuit solutions that conform to European (CCITT) standards. These devices use bit rates that are similar to those for the Bell standards, but they also use a slightly altered set of frequency bands; moreover, they send an extra tone to disable the European phone system's echo suppressors.

Figure 1 also shows a block for an external receive filter that may or may not be needed, depending on which manufacturer's modem chip is used. The modem basically receives a frequency-shift-keyed (FSK) mark (logical One) or a space (logical Zero), and sends serial Ones and Zeros to the UART. At the same time, the modem also receives serial data and synthesizes a phase-continuous sine wave to send to another modem at the other end of the phone line.

Finally, the UART takes parallel data from the microprocessor and feeds a serial data stream to the modem. It also configures the modem's serial output to form a parallel word on the bus. The UART must add start, stop and parity bits to the data word from the bus before transmission of the character and then strip off these same bits at the reception of a character. UARTs have long been available in IC form; they offer various degrees of programmability as well as such features as on-chip baud-rate generation and advanced modem-interface capabilities.

Moving from a block diagram to a specific one, consider the all-CMOS, intelligent-modem board shown in *Figure 2*. This system interfaces with the NSC800 bus; however, you could use any mutiplexed-bus microprocessor. The two -HC688s are bus comparators that are hard wired to generate chipselect signals to the dialer and UART upon accessing the proper memory location. The first -HC688 decodes the eight MSBs from the bus to activate the TP5088 tone generator. When a call is originated, the digits of the phone number are retrieved one at a time from system RAM.

With the modem chip's transmitter squelched, the TP5088 uses the DSI (drive-summing input) pin to the -VHC943's line driver for tone transmission. In order to avoid clipping, you must be sure that the TP5088's output signal level does not exceed the transmit level selected by the TLA resistor. Writing the data on bus lines AD<sub>0</sub> through AD<sub>3</sub> to the tone-generator address causes the TP5088's tone-enable input to switch high through the NOR gate. A low-going WR from the bus latches the four bits into the DTMF generator.

When the -HC688's output enables tone generation, it simultaneously fires one of the -HC123 dual one-shots onto the NSC800 bus's Wait line for 80 msec. Thus, one of 16 possible tone combinations feeds through to the central office for 80 ms. Before the generation of the next tone, a software wait loop serves to turn the generator off for 80 ms, i.e., until transmission of the next DTMF tone pair. This action allows for an 80-ms-On, 80-ms-Off make-break ratio, one that works with almost any central-office receiving equipment. You can change this make-break ratio to suit any requirement by altering the software timing and the one-shot's external-component values.

The same bus comparator pulls in the relay to take the phone off-hook. A read to the address of the first -HC688 does not affect the TP5088; instead, it clocks flip flop 1 of the -HC74 dual D flip flop. This action controls the on-/off-hook relay for answering or hanging up the phone connect

tion. Clocking the -HC74 flips the relay into its opposite state; resetting the NSC800 on power-up causes Reset-Out on the bus to become active. This signal, fed into the Clear input of the -HC74's flip flop 1, keeps the connection on-hook when power is first applied to the system. For micro-processors lacking this Reset-Out signal, a power-on reset circuit could provide this function.

Directly connected to the phone line, the ring-indicator circuit tells the microprocessor that the line is ringing locally. When this happens, the optocoupler's transistor toggles on and off, resulting in a long positive pulse from the normally low Schmitt-trigger NAND output. This signal routes to the RC network and Schmitt-trigger NAND gate, which form a simple one-shot. The resistor and capacitor values are such as to convert the ring signal from a series of low-going spikes into a constantly low logic level.

The first pulse sets off the one-shot, which in turn drives the UART's input. The UART can then interrupt the processor as detailed in a later section. The  $600\Omega$  1:1 transformer isolates the line from hazards. The transformer and ring-indicator circuit connect directly to the phone line; therefore, their designs must follow the isolation guidelines in FCC Rules, part 68.

The NSC858 UART (Figure 3), a member of the NSC800™ family, features an on-chip baud-rate generator, a powerdown mode and extensive interrupt capabilities. It also has two modem-control outputs (DTR and RTS) and three modem-control inputs, (DCD, DSR] and CTS). The absence of an RS-232C connection in this application removes the need for most of these protocols. As a result, except for DCD, these controls serve as general-purpose I/O controls for the modem's SQT and  $O/\overline{A}$  pins and as interrupt inputs. The NSC858 has internal registers that monitor the status of these inputs; if enabled, the registers cause the UART to interrupt the processor if a data set change occurs (i.e., if a logic level changes on one of the modem-control inputs). This is how the ring-indicator circuit in Figure 2 is able to generate an interrupt. The UART's DCD input is connected to the -VHC943's carrier-detect (CD) output to generate an interrupt upon the loss of carrier to the modem. To see which status change is responsible for the interrupt, software can check the UART's modem-status register.

In this application, the  $\overline{\text{RTS}}$  output pin serves to control the O/A pin on the -VHC943. The  $\overline{\text{DTR}}$  output enters the billingdelay circuit shown in *Figure 4*; its function is to activate or deactivate the squelching function for the -VHC943's modulator. Software squelches the modem only by asserting a logical Zero on  $\overline{\text{DTR}}$  whenever its intent is to open the 3state output of the modem's sine-wave synthesizer (*Figure 1*) and to allow the tone generator to use the line driver for externally generated tones.

When  $\overline{\text{PD}}$  goes Low, the -VHC943 and -HC858 power down. The TP5088 is in its low-power mode whenever it is not producing tones.  $\overline{\text{PD}}$  on the NSC800 bus is actually an input to power down the NSC800; therefore, it's assumed that another power-saving control device powers down the whole system. One example of such a device is a real-time clock (for example, the MM58167A) with an alarm-compare interrupt output that can interrupt the processor once during a selected time period.



The modem, UART and DTMF dialer chip can use a 3.579545 MHz TV color-burst crystal. *Figure 2* shows the UART's crystal oscillator driving the other two devices. Schmitt triggers serve to square up the signals to the other devices. The added input capacitance from the Schmitt triggers slightly alters the oscillator frequency, but not appreciably (less than 0.1%). Note that it's important to balance any added capacitance on both sides of the crystal.

#### FCC-REGISTERED PROTECTION

Be warned that before you can legally connect any modem to the phone lines, you must obtain FCC approval of the protective circuitry (once known as the data-access arrangement). *Figure 2*'s subsystem is registered as a "dataterminal device"; it must be able to withstand the high voltages specified in part 68 of the FCC's Rules and Regulations. Hybrid modules to perform the protective functions are available from various manufacturers; some come with FCC approval.

Some of the available modules perform the ring-indicator, billing-delay, filtering, and hybrid functions (as well as other functions). Note, however, that these devices are too expensive for high-volume modem systems. In many cases, moreover, the devices include unneeded or redundant functions. The configuration in *Figure 2* uses a custom protective circuit that includes only the necessary functions, but be aware that the circuit has not undergone the FCC approval process, so it carries no guarantees. For any protective-circuit design, you'd be well advised to obtain the assistance of a qualified consultant in procuring FCC approval. The billing-delay circuitry is shown in *Figure 4*. It uses an -HC00 quad NAND package, half of an -HC123 dual oneshot and half of an -HC74 dual D flip flop. This circuit keeps the -VHC943 squelched for 2 sec after the connection goes off-hook in the answer mode. There is no transmission delay in the originate mode. The 2-sec interval allows the phone company to send supervisory billing tones before the transmission of any data.

The UART's  $\overline{\text{DTR}}$  output pin is low when the modem is to be squelched; this logic level keeps the flip flop's Q output cleared. This low logic level also masks the one-shot's output, so the signal from the NAND gates to the -VHC943's SQT pin remains high, thereby keeping the modem squelched. When the UART brings  $\overline{\text{DTR}}$  high, the flip flop's Q output stays low while the one-shot is fired. The -HC123's normally high  $\overline{\text{Q}}$  output is now pulsed low for 2 sec; this action keeps the modem squelched.

After the delay, the one-shot's output provides a rising edge to the flip flop's clock to transfer the high-logic-level input from DTR to the Q output. The NAND gates now transfer a low level to the modem's SQT pin; as a result, the modem sends a 2025 Hz answer-mode mark. Note that if the system receives a power-down signal from PD, the modem is not allowed to transmit.

If the microprocessor and firmware were included on the same board for submission to the FCC, separate billing-delay circuitry would not be necessary. A 2-sec software wait loop could instead provide the delay; it would act as the billing-delay circuitry.



# DON'T FORGET SOFTWARE

The hardware configuration discussed in the preceding section is, of course, useless without proper software routines to control it. This software comprises three phases: initialization, call establishment and information transfer. Upon system power-up, the initialization procedure must reset the UART and prevent the modem from coming up in an arbitrary mode and thereby transmitting a tone.

The call-establishment phase can commence once the user makes his decision to call another modem or enables the system to accept an incoming call. The main program is for full-duplex character transfer once the phone connection is established and the two modems are talking. If the connection is lost for one reason or another, the call-establishment phase is reentered.

The initialization routine of *Figure 5* serves to set up all the UART's registers immediately after power-up. It starts with a hardware reset from the microprocessor (Reset Out for the NSC800), thereby clearing most of the UART's internal registers and disabling the modem-control pins and their associated interrupts. This register-clearing action also temporarily disables transmission and reception through the UART; it's reenabled only after all the registers are correctly set up and the two modems are receiving each other's carriers.

In the initialization of the transmit-mode register, the  $\overline{\text{CTS}}$  (Clear To Send) pin is normally enabled—however, it's not used in this design, so it's left disabled. In both the transmitand receive-mode registers, the same parity, data-size and internal-clock bits are written in the initialization word. One difference is that  $\overline{\text{CTS}}$  is disabled in the TX mode register's bit 6, but in the RX mode register, bit 6 serves to enable DCD (data-carrier detect).

The other difference is that the TX mode register accesses the transmit-abort end condition (TAEC), which decides whether the last character to be sent out of the UART (when transmission is disabled) is from the TX holding register or the TX shift register. The holding register is the first UART buffer to receive the data before it is sent to the shift register and clocked out to the modem (as shown in *Figure 3*). TAEC selection depends on the perceived urgency of data reception, which is given higher priority than transmission.

The global mode register selects the clock factor ( $\times$ 16) for the on-chip baud-rate generator. This selection determines at what multiple of the baud rate data clocks into the transmit shift register and clocks out of the receive shift register. The global mode register also selects the number of transmit stop bits.

The next step is to initialize the receive-transmit status mask register; this is used in conjunction with the receive-transmit status register, which is read to determine what caused the UART to interrupt the microprocessor. The status signals used to generate interrupts in this design include

- · Receiver data ready
- Receiver overrun error (meaning data has overwritten an unread received character)
- Receiver framing error (no valid stop bit detected)
- Receiver parity error
- Data set change
- · Data set change

The reason for writing to the transmit-receive status mask is to select those status signals that will be allowed to generate interrupts. A data set change refers to a logic-level change on one of the modem's status input pins. The



registers just after power-up. A reset from the  $\mu$ P starts the sequence; it also disables transmission and reception through the UART until the modems receive each other's carriers. Additionally, it sets the clock factor and the baud-rate generator for the desired data rate. Finally, the initialization sequence selects autoanswer or auto-originate mode. UART's modem status mask register masks these signals to determine which ones will be allowed to create a dataset-change interrupt.

The final area of initialization sets the baud rate for sending data out of the UART's transmit shift register and for clocking data out of the receive shift register. Writing a value of 745<sub>10</sub> into the baud-rate divisor latch gives 300-baud operation with a 3.579545 MHz crystal, using the previously selected  $\times$ 16 clock factor.

#### AUTO-ORIGINATE ROUTINE

The auto originate routine in *Figure 6* begins by disabling interrupts to prevent an incoming call or anything else from taking over the processor and damaging the critical dialing timing. A read to the address occupied by the tone decoder causes the system to go off-hook. It's necessary to wait a suitable amount of time, depending on the phone system's response time, for a dial tone. Dial-tone reception is not

acknowledged in this application, so it's best that the wait loop be as long as possible.

Next, the first binary phone-number digit is retrieved from memory and is written onto the AD<sub>0</sub> through AD<sub>3</sub> line from the microprocessor bus. This action automatically puts the  $\mu$ P in wait state for 80 ms (in hardware) while the tone is sent. After this wait, a software wait loop gives 80 ms of silence between tones. The next phone-number digit is then retrieved from memory; the process continues until the number is completely dialed.

At this point, selection of the originate mode occurs by writing a Zero to bit 6 (RTS) in the command register. This action sets the  $\overline{\text{RTS}}$  pin (which directly feeds  $O/\overline{A}$  in the -VHC943) High in the UART. Next, a wait loop occurs concurrently with the polling of bit 5 of the modem status register. If, after 30 sec of waiting, no carrier is received (bit 5 = 0), the connection has not been established. A carrier is typically detected in about 10 sec; 30 sec is the maximum.



If no carrier is received, you can hang up the connection and call the number again, enter the autoanswer mode, or abandon the call. If the connection is established, and an answer-mode carrier is received, then writing a One to bit 7 (DTR) of the command register removes the squelch previously imposed upon the originate modem's carrier. This action causes the UART's DTR pin to switch Low; as a result, SQT = 0 in the modem. Now the UART's command register enables the receiver and transmitter, and full-duplex communication can begin through the main program. The autoanswer routine of *Figure 7* must begin with an interrupt that indicates that the phone line has a ring signal on the answer modem's side of the telephone line. Before this can occur, it's necessary to enable interrupts. The hookswitch control circuit is still on-hook as it was after powerup. Writing a One to bit 7 of the UART's command register ensures squelching of the modem's transmitter. Writing a One to DSR in the modem mask register and Zeros to all other bits in this register prevents any other type of dataset-change interrupt from occurring.



The system can continue to do other tasks in anticipation of a calling interrupt, providing the preceding conditions do not change. When an interrupt does occur, checking bit 7 of the receive-transmit status register reveals whether a data set change has occurred. If one hasn't occurred, then some other peripheral has interrupted the microprocessor. Upon verification of a data set change, it's necessary to check bit 6 of the modem status register to see whether the  $\overline{\text{DSR}}$  pin has gone high.

Because all other bits in the modem status mask were masked out, it's unlikely that any other modem status pin has caused the interrupt. Once bit 6 is verified to be high, system interrupts are disabled and the processor's stack popped to prevent an interrupt return. Meanwhile, the phone line still sees a ringing signal, so a wait loop can be inserted for a programmed number of rings before the call is answered. The connection then goes off-hook as a result of reading the tone dialer's address space.

Writing a One to bit 6 (RTS) of the command register selects the -VHC943's answer mode. This action brings the modem's O/ $\overline{A}$  pin Low. A 2 sec wait now occurs in hardware, as previously discussed. The originate modem is now waiting in silence. Writing a One to bit 7 (DTR) of the command register now removes the squelch imposed upon the answer modem's transmitter. This operation forces the -VHC943's squelch (SQT) pin Low and causes transmission of a 2025 Hz answer-mode mark.

The answer modem is now anticipating the originate modem's 1270 Hz carrier. During a 5 sec max wait, bit 5 (DCD) of the UART's modem-status register is polled for a logical One. If DCD does not go high in this time, the connection goes on-hook and the answer modem's carrier is suppressed by the squelch circuit. The originate modem can now attempt a recall. If the modem receives a carrier within the 5 sec limit, bits 0 and 1 in the command register both go High, enabling both transmission and reception. Full-duplex communication can now begin, and access to the main program for this operation now occurs.

## THE MAIN RX/TX PROGRAM

data word receives top priority.

After establishing the phone connection between the two modems, the main program of Figure 8 controls the reception and transmission of data. The routine begins with the enabling of system interrupts. Transmission uses a wellknown polling technique that checks the receive-transmit status register whenever a character is ready for transmission. If the TXBE (transmit buffer empty) bit is Zero, polling of the bit continues until it reads logical One. A character is then written into the transmit holding register and the process continues. The character is also transferred to and clocked out of the transmit shift register and sent to the -VHC943: this final process is transparent to the software. Data reception receives a higher priority than does transmission, in most cases, because a character will be overwritten in the UART if it is not read promptly enough. Thus, reception is interrupt-driven. Other UART-oriented functions

are interrupt-driven in the main program, but reception of a



A read of the receive-transmit status register serves to poll six of its important bits. Bit 0 (Receiver Data Ready) is polled first; if it's a logical One, a read of the RX holding register takes place. This action is followed by an interrupt return that transfers control back to the transmission mode. If bit 0 yields no information, bits 3, 4 and 5 are read in order. If one of these bits reads logical One, this means a receiver-overrun, framing or parity error has occurred; the incoming data is defective and must be retransmitted.

A suitable means of requesting a retransmission of the last block of characters is to transmit a break, which is a continuous string of logical Zeros. Variable break lengths are programmable on the NSC858. If the three bits yield no error information, then a check of bit 3 (BRK) reveals whether the remote modem has received an error and is requesting a block resend. The two modems must agree upon both break length and block size in order to honor retransmission requests.

Finally, if none of these bits yields any information on the cause of the interrupt, the only remaining possibility is loss of carrier. This loss is verifiable by looking for a logical Zero on bit 5 of the modem status mask. If carrier loss occurs, communication must be reestablished. Both modems are put back in their originate or answer modes, as applicable.

Note in *Figure 8* that a full RX buffer or an RX error does not require a stack pop, because the transmission of data can continue undisturbed. If, instead, a break is received (implying loss of carrier), then the stack must be popped because data transmission is in error or has been broken off—so there's no sense in returning to the transmit mode.

### HOW MUCH POWER?

Hardware and software requirements satisfied, it's important to consider the worldly question of power consumption. It's easy to calculate the consumption of *Figure 2's* system. The -HC688s, the -HC123 and the -HC74 switch at a very slow rate, so you can use their quiescent-I<sub>CC</sub> specs. At 25°C, the worst-case I<sub>CC</sub> for these devices is 8  $\mu$ A. The other logic chips (i.e., the quad NOR and Schmitt NAND) are also 74HC devices; they consume only 2  $\mu$ A per package at 25°C.



FIGURE 9. This simple power-down circuit puts the crystal oscillator to sleep, reducing the modem's quiescent current by 245 μA.

The consumption of the -HC devices is insignificant in comparison with that of the larger circuits in *Figure 2*. The NSC858 uses 5 mA when operating at 300 baud, and it uses, at most, approximately 200  $\mu$ A in power-down mode. The -VHC943 consumes 9 mA max when transmitting at -9 dBm; I<sub>CC</sub> drops to 250  $\mu$ A in power-down mode. The resistor divider for the -VHC943's analog-ground connection consumes approximately 1 mA. This current is not required by the -VHC942; moreover, using an op-amp-generated reference instead of a divider can eliminate it for the -VHC943.

Because the TP5088 never operates at the same time as the modem, and because the modem consumes more power, only the DTMF generator's idle-mode (no tones sent) current of 100  $\mu$ A is needed. The hook-switch relay typically consumes about 5 mA, but this figure is strongly dependent on the type of relay used. The ring-indicator circuit is line powered; therefore, you need not include its consumption in these calculations.

The total worst-case current at 25°C is 20 mA when the modem is transmitting, 1.5 mA when the system is in the power-down state. This power-down current is roughly equivalent to the current consumed by a single low-power Schottky-logic gate. *Figure 9* shows a method of powering down the crystal oscillator, reducing the power-down current for the -VHC943 and the system in *Figure 2* by 245  $\mu$ A. Note that the microprocessor's power calculations, and those of the system memory or other peripherals, are not included in these computations.

## APPLICATIONS AREAS

Where can you apply the modem system described in this article? The most obvious application area is perhaps the area of personal computers. But this design is suitable for many other microprocessor-controlled systems. For example, *Figure 10* shows a  $\mu$ P-based electronic-funds-transfer (EFT) terminal (using public telephone lines) at a gasoline station. The system comprises a magnetic-card reader linked to a display, and several gasoline pumps, each with its own display.

The pumps are connected to the system controller, which is a  $\mu$ P-based system with memory, data-encryption firmware, pump-control electronics and a modem board. Because transactions are executed upon the request of the debit-card holder (and not on the request of the bank), the mo-



FIGURE 10. An electronic-funds-transfer system allows for gasoline purchases in this example. The gas pumps connect to a system controller that protects data by using an encryption technique. The system uses public phone lines instead of expensive leased lines. The preferred data rate for such proposed systems is 300 baud. dem circuit of *Figure 2* would be configured as an originateonly system. The answer-routine software and the ring-indicator circuit are not needed.

For central-office receiving equipment that operates on pulses rather than on DTMF tones, the tone-dialing circuitry (TP5088, -HC688 and -HC123) is also unneeded. The microprocessor could toggle the logic-controlled relay to send the dialing pulses while software wait loops control the pulse duration.

For a large number of EFT terminals linked to one system, a subset of the terminals could interface with a network controller that would communicate with the central computer at a much higher data rate than that of any one terminal. The network controller would multiplex the data from the terminals in its local cluster. This configuration would reduce the number of leased lines used from one per terminal to one per controller, substantially reducing system cost.

Most of the risk of opening the public phone system to electronic-funds transfer could be eliminated by using data encryption, with a key that's easily changed electronically (and it should be changed as often as possible). Data encryption handled in hardware would offer the speediest operation. Such networks are common today, except that usually only leased lines are used for EFT. Standards for EFT over the public phone system are currently in development.

In using public phone lines for EFT, the data-transfer rate would necessarily be 300 baud for reliable operation over all the lines in the system. The 212A standard could also apply (it would be as reliable as the 103 standard because it has a 300-baud FSK backup mode), but a single-chip 212A IC could easily attain ten times the cost of the 300-baud -VHC943 because of the IC's much greater die size. A smaller number of applications would derive much benefit from the more expensive 212A IC; applications in which very short blocks of data are transferred would glean the least benefit of all.

For example, if the total number of characters (bytes of data) to be transferred is 60, then the transmission time is 2 sec at 300 baud. Using the 212A standard (1200 baud; full duplex), this time would be reduced to 0.5 sec, for a 1.5-sec savings. This time savings is minimal in terms of billing time. And when you consider the total calling time, this 1.5-sec decreased delay does not make the EFT terminal or credit-verification system appreciably more convenient.

Long-distance dialing with a conventional pulse or rotary system can take as long as 10 sec, while DTMF dialing takes 1 sec. The interoffice switching time from dialing completion to remote ring can be as long as 12 sec. Finally, for every data transmission over the phone system, the FCC requires a 2-sec billing delay before data can be sent. So, the total transmission time can be as long as 18sec with DTMF dialing; 26 sec with pulses. It's now evident why the savings of 1.5 out of 18 or 26 sec does not justify the much greater cost of a 212A system in applications using short blocks of data. For a properly engineered EFT system, a 60character block of data per transaction in both directions is not unreasonably restrictive.

Finally, there are many other applications that could use the public phone lines to transmit data and that could benefit from the advantages of 1-chip modems. These areas include credit-verification terminals, security systems, acoustic modems, cellular telephones, vending machines, electronic-mail terminals and remote utility-metering devices.

# ANATOMY OF A 1-CHIP MODEM

The Bell 103 standard specifies the frequency bands for FSK marks and spaces. If the modem originates the call, it transmits a space as a 1070 Hz; sine wave; a mark is at 1270 Hz. It receives a mark as 2225 Hz and a space as 2025 Hz. Consequently, the answer modem receives marks at 1270 Hz and spaces at 1070 Hz; it transmits them at 2225 and 2025 Hz, respectively. Originate and answer modes are selectable on the -VHC943's O/Ā pin (*Figure A*).

The transmission level is set by a resistor to the TLA (transmit-level adjust) pin. The resistor values and attendant transmit levels follow the Universal Service Order Code, as shown in the -VHC943's data sheet. Raising the SQT pin produces a squelch, causing the modem's sine-wave synthesizer to assume open 3-state outputs. A squelch action is needed when the modem's line driver is being used to send externally generated dial tones, voice transmission or other signals.

The modem IC also has an analog loopback (ALB) pin that, when taken high, allows input data on pin TXD to come out on the RXD pin after a short delay. Analog loopback is useful as a diagnostic tool. When both SQT and ALB are taken high, the -VHC943 goes into its power-down mode—I<sub>CC</sub> drops to 250  $\mu$ A and the line-driver's 3-state output assumes the open state.

The -VHC943 has an on-chip carrier-detect circuit that signals the reception of an adequate carrier (signal from the modem at the other end of the line). When no carrier is present, the modem's  $\overline{\text{CD}}$  output assumes a logical One. When a carrier at or above -44 dBm is received,  $\overline{\text{CD}}$  goes low after a time delay that's controllable by the CDT input.

The carrier-detect trip point then drops 3 dB, providing hysteresis to stabilize the  $\overline{\text{CD}}$  output. Varying the capacitor on the CDT pin changes the carrier-detect turn-on time delay. This capacitor similarly affects carrier-detect turn-off time. The carrier-detect off-to-on times are set to be longer than the on-to-off times. This means the carrier must be present and stable to be acknowledged; and that if the carrier changes from a stable level to a marginal one, it will be quickly rejected.

The -VHC943 offers several advantages over other approaches to modem design. One beneficial feature is the fact that the receive filter, carrier-detect circuit and hybrid function are included on the chip (*Figure A*). This inclusion lowers parts count, saves board space and makes the part easy to design in and use.

The IC is also very economical with power, using only 8 mA when transmitting at -9 dBm. It also includes a powerdown mode that reduces  $I_{CC}$  to 250  $\mu$ A. The device operates from one 5V supply; this span gives the modem a typical output transmit range of -9 to -12 dBm. A variation, the -VHC942, has an output transmit range of 0 to -12dBm typ when operating from  $\pm$ 5V supplies.

The -VHC943 performs well in the presence of noise. In tests using the industry-standard C-message-weighted noise injected over a resistive phone-line simulator and with the modem's transmitter sending pseudorandom data, the IC received a 511-bit pseudorandom pattern with a bit-error rate of 10<sup>-5</sup>, or one error in 10<sup>5</sup> bits sent. These tests were conducted with 4.5-dB signal-to-noise ratio. Further bit-error ror-rate tests are under way; the results will be published soon.



# LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation National Semiconductor Europe   111 West Bardin Road Arlington, TX 76017 Tel: 1(800) 272-9959 Fax: 1(800) 737-7018 National Semiconductor Europe   Fax: (+49) 0-180-530 85 86 Emglish Tel: (+49) 0-180-532 85 85 English Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-532 43 16 80	National Semiconductor Hong Kong Ltd. 13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2736-9960 Fax: (852) 2736-9960	National Semiconductor Japan Ltd. Tel: 81-043-299-2309 Fax: 81-043-299-2408
----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.