74VHC942 and 74VHC943 Design Guide

National Semiconductor
Application Note 1016
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The 74VHC942/943 devices are direct pin, function and spec replacements for the MM74HC942/943 devices.

1) TIMING AND CONTROL

a) Input and Output Thresholds

The 74VHC942/943 may be used in a CMOS or TTL environment. In a CMOS environment, no interfacing is required. If the 74VHC942/943 is interfaced to NMOS or bipolar logic circuits, standard interface techniques may be used. These techniques are discussed in detail in National Semiconductor Application Note AN-314.

b) Logic States and Control Pin Function

Transmitted Data

TXD (pin 11) in conjunction with O/A selects the frequency of the transmitted tone and thus controls the transmitted data.

TXD = V_{CC} selects a ''mark'' and thus the high tone of the tone pair. This is discussed further in the following section.

Originate and Answer Mode

This is controlled by O/A (pin 13). O/A = V_{CC} selects originate mode. O/A = GND selects answer mode. These modes refer to the tone allocation used by the modem. When two modems are communicating with each other one will be in originate mode and one will be in answer mode. This assures that each modem is receiving the tone pair that the other modem is transmitting. The modem on the phone that originated the phone call is called the originate modem. The other modem is the answer modem.

The other pin controlling the transmitted tone is TXD (pin 11).

Bell 103 Tone Allocation				
Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz

Squelch Transmitter

Transmitter squelch is achieved by putting SQT = V_{CC} (SQT is pin 14). The line driver remains active in this state (assuming ALB = GND).

This state is commonly used during the protocol of establishing a call. The originate user initiates a phone call with its transmitter squelched, and waits for a tone to be received before beginning transmission. During the wait time, the modem is active to allow tone detection, but no tone may be transmitted.

The state SQT = V_{CC} may also be used if the line driver is required but a signal other than modem tones (e.g., DTMF tones or voice) is to be transmitted. This is discussed further in Transmission of Externally Generated Tones (section 3d).

Analog Loop Back

ALB = V_{CC}, SQT = GND selects the state ''analog loop back''. (The state ALB = SQT = V_{CC} is discussed in the following section.)

In analog loop back mode, the modulator output (at the line driver) is connected to the demodulator input (at the hybrid), and the demodulator is tuned to the transmitted frequency tone set. Thus the data on the TXD pin will, after some

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delay, appear at the RXD pin. This provides a simple ''self test'' of the modem.

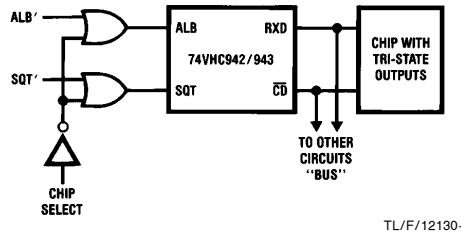
The signal applied to the demodulator during analog loop back is sufficient to cause the carrier detect output CD to go low indicating receipt of carrier.

In analog loop back mode, the modulator and transmitter are active, so the transmitted tone is not squelched.

Power-Down Mode

The state SQT = ALB = V_{CC} puts the 74VHC942/943 in power-down mode. In this state, the entire circuit except the oscillator is disabled. (The oscillator is left running in case it is required for a system clock). In power-down mode the supply current falls from 8 mA (typ) to 180 μA (typ), and all outputs, both analog and digital, TRI-STATE (become Hi-Z).

Using TRI-STATE Capability



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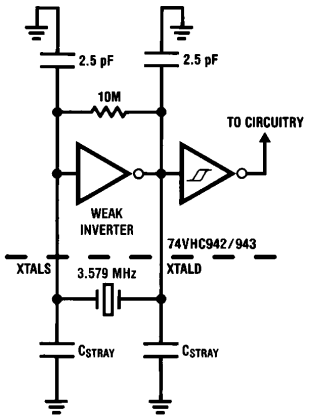
The ability of the outputs to TRI-STATE allows the modem to be connected to other circuitry in a bus-like configuration with the state SQT or ALB = GND being the modem chip select.

c) The Oscillator

The oscillator is a Pierce crystal oscillator. The crystal used in such an oscillator is a parallel resonant crystal.

The Oscillator



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The capacitors used on each end of the crystal are a combination of on-chip and stray capacitances. This generally means the crystal is operating with less than the specified parallel capacitance. This causes the oscillator to run faster than the frequency of the crystal. This is not a problem as the frequency shift is small (approximately 0.1%).

The oscillator is designed to run with equal capacitive loading on each side of the crystal. This should be taken into consideration when designing PC layouts. This need not be exact.

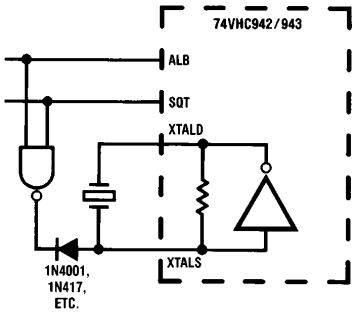
If a 3.58 MHz oscillator is available, the XTALD pin may be driven. The internal inverter driving this pin is very weak and can be overpowered by any CMOS gate output.

The Oscillator and Power-Down Mode

When the chip powers down, all circuits except the oscillator are switched off. The oscillator is left running so it may be used as a clock to drive other circuits within the system.

It is possible to shut the oscillator down by clamping the XTALS pin to V_{CC} or GND. This will cause the total chip current to fall to less than 5 μA. This may be useful in battery powered systems where minimizing supply current is important.

Powering Down the Oscillator



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2) MODULATOR SECTION

a) Operation

The modulator receives data from the transmit data (TXD) pin and synthesizes a frequency shift keyed, phase coherent sine wave to be transmitted by the line driver through the transmit analog (TXA) pin. Four different sine wave frequencies are generated, depending on whether the modem is set to the originate or answer mode and whether the data input to TXD is a logical high or low. See Timing and Control (section 1) for more information.

The TXD and O/A pins set the divisor of a dual modulus programmable divider. This produces a clock frequency which is sixteen times the frequency of the carrier to be transmitted. The clock signal is then fed to a four bit counter whose outputs go to the sine ROM. The ROM acts like a four-to-sixteen decoder that selects the appropriate tap on the D/A converter to synthesize a staircase-approximated sine wave. A switched capacitor filter and a low pass filter smooth the sine wave, removing high frequency components and insuring that noise levels are below FCC regulations.

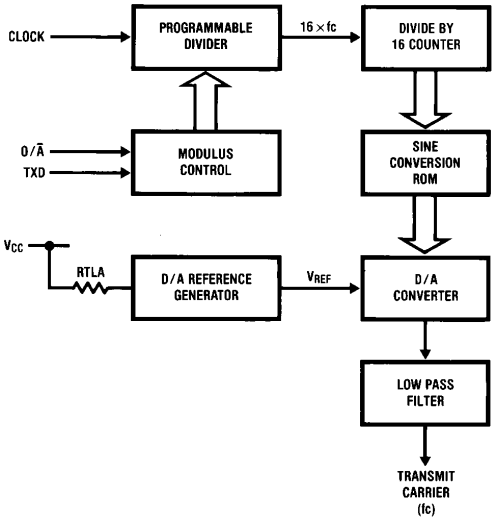
b) Transmit Level Adjustment

The maximum transmit level of the 74VHC943 is −9 dBm. Since most phone lines attenuate the signal by 3 dB, the maximum level that will be received at the exchange is −12 dBm. This level is also the maximum allowed by most phone companies. The 74VHC942 has a maximum transmit level of 0 dBm, making possible adjustments for line losses up to −12 dB. The resistor values required to adjust the transmit level for both the 74VHC942 and the 74VHC943 follow the Universal Service Order Code and can be found in the data sheets.

This resistor added between the TLA pin and V_{CC} serves to control the voltage reference at the top of the D/A ladder, adjusting output levels accordingly.

Note that for transmission above −9 dBm the required resistor must be chosen with the co-operation of the relevant phone company. This resistor is usually wired into the phone jack at the installation as the resistor value is specific to the particular phone line. This is called the Universal Registered Jack Arrangement. This arrangement is possible only with the 74VHC942 because of the dynamic range constraints of the 74VHC943.

The Modulator



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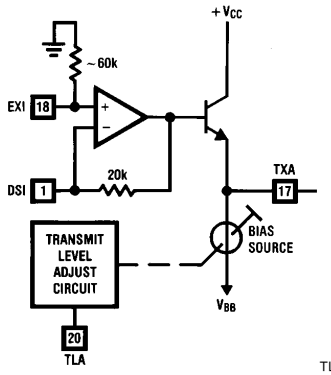
3) THE LINE DRIVER

a) Operation

The line driver is a class A power amplifier for transmitting the carrier signals from the modulator. It can also be used to transmit externally generated tones such as DTMF signals, as discussed in section 3d. When used for transmitting modem-produced tones, the external input (EXI) pin should be grounded to pin 19 for both the 74VHC942 and the 74VHC943. The line driver output is the transmit analog (TXA) pin.

The Line Driver Equivalent Schematic



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b) Second Harmonic Distortion

If the modem is operating in the originate mode, the line driver output has frequencies of 1070 Hz for a space and 1270 Hz for mark. The second harmonic for a space frequency is at 2140 Hz, and this falls in the originate modem's receive frequency band from 2025 Hz to 2225 Hz. While the modulator produces very little second harmonic energy, the amplifier has been designed not to degrade the analog output any further. The result is that the second harmonic is below −56 dBm. Thus it is well below the minimum carrier amplitude recognized by the demodulator.

c) Dynamic Range

The decision to use the 74VHC942 or the 74VHC943 is a tradeoff between output dynamic range and power supply constraints. The power supply is discussed in another section. The 74VHC942 will transmit at 0 dBm while the maximum transmit level of the 74VHC943 is −9 dBm. This level applies to externally generated tones as well as the standard modem tone set.

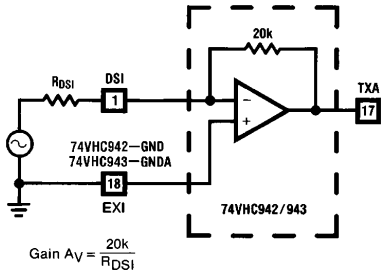
It is important to realize that the signal levels referred to above, and in the data sheet's specifications, are the levels referred to a 600Ω load resistor (representing the phone line) when driven from the external 600Ω source resistor. Also, the transmit levels discussed previously are maximum values. Typical values are 1 dB to 2 dB below these.

d) Transmission of Externally Generated Tones

Since a phone line connection is usually made on the TXA pin, it may be useful to use the line driver to transmit DTMF, voice or other externally generated tones. Both the inverting and non-inverting inputs to the line driver are available for this purpose. A DTMF tone generator with a TRI-STATE output may instead be directly connected to the same node as the TXA pin rather than the line driver. The choice of which method to use depends on whether the 74VHC942 or 74VHC943 is being used and the signal level of the transmission. Most phone companies allow DTMF tone generation at 0 dBm. This level is the maximum that the 74VHC942 can produce and is beyond the range of the 74VHC943.

If the line driver is to be used for external tone generation, the modem must be powered up and the transmission must be squelched by the SQT pin being held high. This will disable the output of the modulator section. The choice between the EXI pin and DSI pin is up to the user. The EXI pin gives a fixed gain of about 2. The DSI input allows for adjustable gain as a series resistor is necessary.

Using the DSI Input



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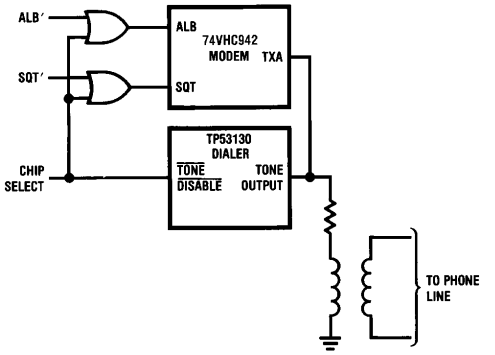
A better solution may be to use the power-down mode of the 74VHC942/943 with a DTMF tone generator that has a TRI-STATE output. Such a device is a TP53130 and is

shown in the diagram following. When the tone generator is not in use and the modem is not squelched, the DTMF generator's output is in TRI-STATE. Rather than using the line driver, the tone generator's output is instead connected to the same node as the TXA pin. The tone generator is active when the modem is in power-down. Power-down TRI-STATEs the TXA output.

Interfacing to DTMF Generator Using TRI-STATE Feature



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4) THE HYBRID

The 74VHC942/943 has an on-chip hybrid. (A hybrid in this context refers to a circuit which performs two-to-four wire conversion.)

Under ideal conditions the phone line and isolation network have an equivalent input impedance of 600Ω. Under these conditions the gain from the transmitter to the op amp output is zero, while the gain from the phone line to the op amp output is unity. Thus the hybrid, by subtracting the transmitted signal from the total signal on the phone line, has removed the transmitted component.

Unfortunately, these ideal conditions rarely exist and filtering is used to remove the remaining transmitted signal component. This is discussed further in the next section.

Note that the signals into the hybrid must be referred to GND in the 74VHC942 and GNDA in the case of the 74VHC943. Thus blocking capacitors are required in the latter case. This is discussed further in DC Levels and Analog Interface (section 9a).

5) THE RECEIVE FILTER

The signal from the hybrid is a mixture of transmitted and received signals. The receive filter removes the transmitted signals so only received signal goes to the discriminator.

The receive filter may be characterized by driving RXA1 or RXA2 with a signal generator. The filter response may then be observed at the FTLC pin with the capacitor removed. In this state the output impedance of the FTLC pin is 16 kΩ nominal.

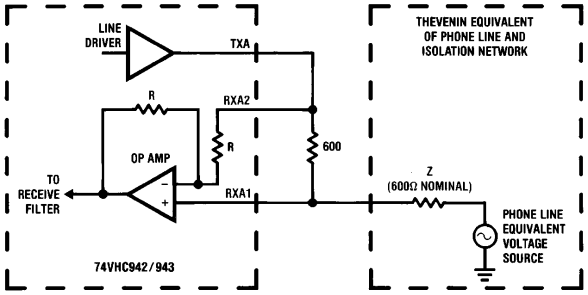
6) THE FTLC PIN

The FTLC pin is at the point of the circuit where the receive filter output goes to the hard limiter input and the carrier detect circuit input.

The signal at the output of the receive filter may be as low as 7 mVrms. It is thus important that the wiring to the FTLC pin and the associated circuit be clean. Ideally the track from the capacitor to pin 19 (GND on the 74VHC942, GNDA on the 74VHC943) should be shared by no other devices.

If these precautions are not observed, circuit performance may be unnecessarily degraded.

The Hybrid



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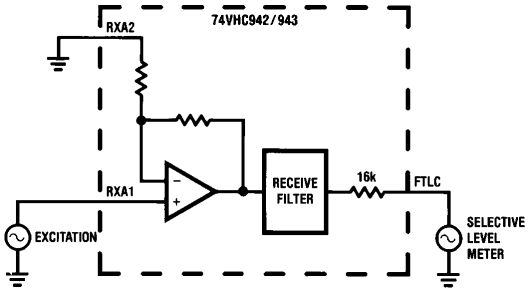
Characterizing the Receive Filter



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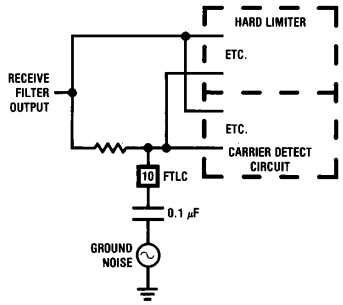
The FTLC Pin and Associated Circuitry



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7) THE CARRIER DETECT CIRCUIT

a) Operation

The carrier detect circuit senses if there is carrier present on the line. If carrier is not present, the data output is clamped high.

The RC circuit filters the DC from the output of the receive filter. The comparator inputs are thus the filter output, and the DC level of the receive filter minus the controlled offset. The controlled offset sets the amount that the AC signal must exceed the DC level (and thus the AC amplitude) before the comparator switches. When this happens, the comparator output sets a resettable one-shot which converts the periodic comparator output to a continuous signal. This signal then controls the time delay set by the CDT pin. After the preset time delay the CD bar output goes low. This shifts the comparator offset providing hysteresis to the overall circuit.

b) Threshold Control

The carrier detect threshold may be adjusted by adjusting the voltage on the CDA pin.

The carrier detect trip points are nominally set at −38 dBm and −41 dBm. The CDA pin sits at a nominal 1.2V. The carrier detect trip points are directly proportional to the voltage on this pin, so doubling the voltage causes a 6 dB increase in the carrier detect trip points. Similarly, halving the voltage causes a 6 dB decrease in carrier detect trip points.

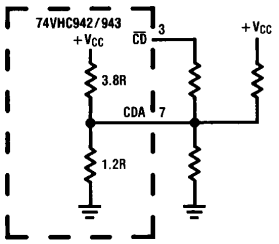
Note that as the carrier detect trip point is reduced, the system noise will approach the carrier level, and the accuracy and predictability of the carrier detect trip points will decrease.

The output impedance of the CDA pin is high. It is constant (±10%) from die to die but has a very high temperature coefficient. It is thus advisable, if the CDA pin is driven, to drive from a low source impedance.

Because the output impedance of the CDA pin is high, capacitive coupling from the adjacent XTALD pin can present a problem. For this reason a 0.1 μF capacitor is usually connected from the CDA pin to ground. If the CDA pin is driven from a low impedance source, this capacitor may be omitted.

If a resistor is connected from the CD bar pin to the CDA pin, the CDA voltage will vary depending on whether carrier is detected. This will effectively increase the carrier detect hysteresis.

Increased Carrier Detect Hysteresis



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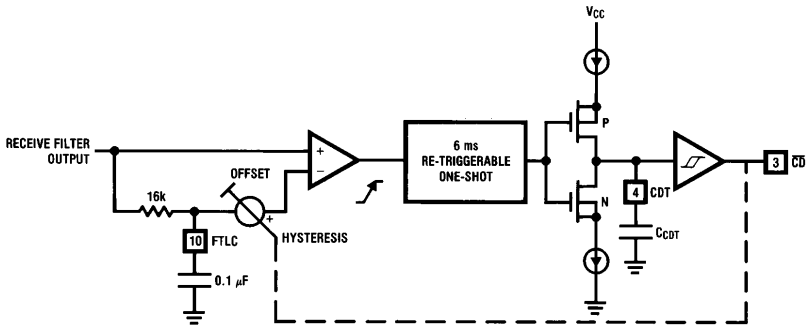
Similarly an inverter and a resistor from the CD bar pin to the CDA pin will reduce the hysteresis. This is not recommended as the 3 dB nominal figure chosen is close to the minimum value useable for stable operation.

c) Timing Control

The capacitor on the CDT pin adjusts the amount of time that carrier must be present before the carrier is recognized as valid.

Carrier Detect Block Diagram



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This circuit is designed for a long off-to-on time compared to the on-to-off time. This means carrier must be present and stable to be acknowledged, and that if carrier is marginal it will be rejected quickly.

The equations for the capacitor value are

$T_{on\text{-}to\text{-}off} = C \times 0.54$ seconds

and

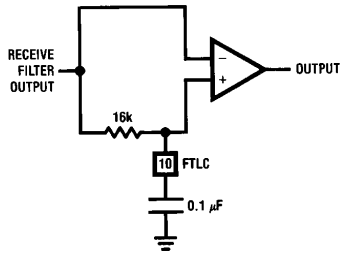
$T_{off\text{-}to\text{-}on} = C \times 6.4$ seconds.

The ratio of on-to-off and off-to-on times may be adjusted over a narrow range by the addition of pull-up or pull-down resistors on the CDT pin.

The repeatability of the times is high from die to die at fixed temperature, but is strongly temperature dependent. The times will shift by approximately ±30% over process and temperature.

8) THE DISCRIMINATOR

a) The Hard Limiter



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The signal to the inverting input of the comparator has the same DC component as the signal to the non-inverting input. The differential input to the comparator is thus the AC component of the filter output. The comparator has very low input offset and so the limiter will operate with very low input signal levels.

The demodulator employed requires an input signal having equal amplitude for a mark and a space. It also requires a high level signal. The hard limiter converts all signals to a square wave. All amplitude information is lost but frequency information is retained.

By removing the capacitor from the FTLC pin, the hard limiter ceases to operate, but the filter output may be observed. This is useful for circuit evaluation and testing.

b) Discriminator Operation

The discriminator separates the incoming energy into mark and space energy. This occurs in the band pass filters which are tuned to the mark and space frequencies. The outputs of the mark and space band pass filters are rectified to extract the output amplitudes. The rectifier outputs are filtered to remove ripple. The low pass filter outputs are compared to determine if the mark or space path is receiving greater energy, and thus if the incoming data is a mark or a space.

The output of the discriminator is only valid if carrier is being received. If carrier is not being received (as determined in the carrier detect circuit) the RXD output is clamped high. This stops the discriminator from attempting to demodulate a signal which is too low for reliable operation.

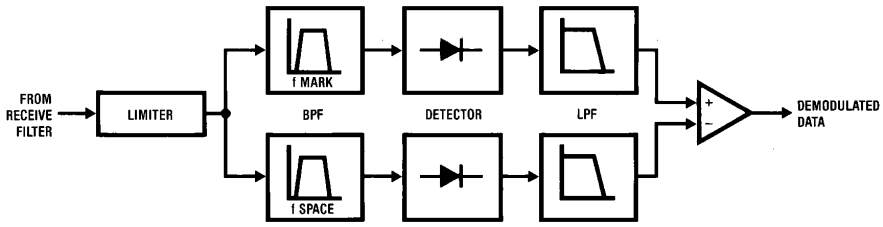
9) POWER SUPPLIES

a) DC Levels and Analog Interface

The 74VHC942 refers all analog inputs and outputs to GND (pin 19). The analog interface thus requires no DC blocking capacitors.

The 74VHC943 refers all analog inputs and outputs to GNDA (pin 19) which requires a nominal 2.5V supply. The current requirements of GNDA are low, so the GNDA supply may be derived with a simple resistive divider. The GNDA supply can then be referenced to GND using capacitors. This GNDA supply will have poor load regulation so the high current interface must be connected to GND and a DC blocking capacitor used.

As the FTLC capacitor is connected to the input of the hard limiter, any noise on the FTLC ground return will couple directly into this circuit. The signal on FTLC may be only millivolts, so it is important that the FTLC capacitor ground be at the same potential as the chip's ground reference. Thus when using the 74VHC943 the FTLC capacitor ground return should go directly to GNDA (pin 19). For both the 74VHC942 and 74VHC943 this ground return should be shared by no other circuits. Failure to observe this precaution could result in unnecessary reduction of dynamic range and carrier detect accuracy, and an increase in error rate.



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b) Power Supply Noise

It is important that the power supplies to the 74VHC942/943 be stable supplies, having low noise, particularly in the frequency band from 50 kHz to 10 MHz.

The 74VHC942/943 use switched capacitor techniques extensively. A feature of switched capacitor circuits is their ability to translate noise from high frequency bands to low frequency bands. At the same time it is difficult to design op amps with high power supply rejection at high frequencies. (The 74VHC942/943 has 19 op amps internally.) As a result the high frequency PSSR of the 74VHC942/943 is not high, so high frequency noise on the power supply can degrade circuit operation.

This should not cause a problem if the circuits are powered from a three terminal regulator, and no other circuitry shares the regulator. Power supply noise could be a problem if:

a) One or both of the power supplies are switching regulator circuits. Switching regulators can produce a lot of supply noise.

b) The modem shares its supply with a large digital circuit. Digital circuits, particularly high speed CMOS (the HC family) can produce large spikes on the supplies. These spikes have wide spectral content.

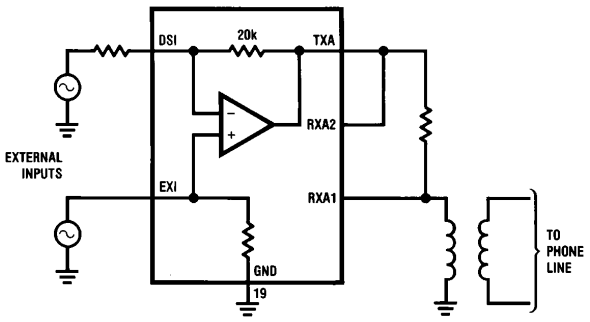
Ideally the modem could have its own supply. This may not be cost effective, so in some applications power supply filters may be necessary. These may just be RC filters but LC filters may be necessary depending on the extent of the supply noise. Miniature inductors in half watt resistor packages are cheap, lend themselves to automatic insertion, and are ideal for these filters.

It is difficult to set specifications for a ''clean'' supply because spectral density considerations are important. The following guidelines should be taken as ''rule of thumb'':

a) From 50 kHz to 20 MHz the ripple should not exceed −60 dBV.

b) From DC to 50 kHz the ripple should not exceed −50 dBV.

74VHC942 Analog Interface



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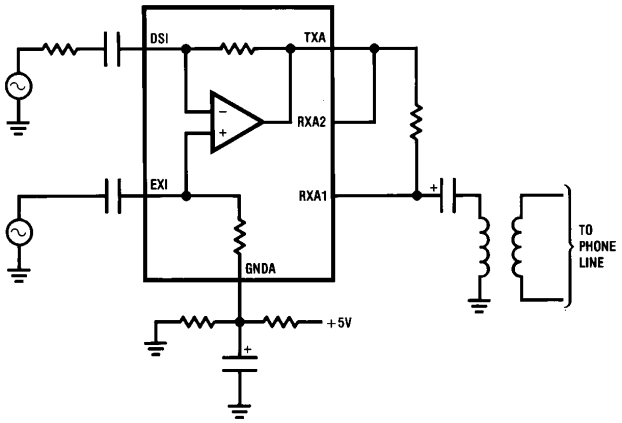
74VHC943 Analog Interface



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