Structural System Test via IEEE Std. 1149.1 with Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F

National Semiconductor
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INTRODUCTION

IEEE Std. 1149.1 (JTAG) defines a standard Test Access Port (TAP), protocol and set of commands for built in test at both the chip and board level. A board designed with boundary scan components typically consists of one scan chain which daisy-chain (TDO to TDI) all components on the board. While a single scan chain solution might be adequate for testing a board in production or a single-board system, it is not adequate when a multi-board system requires interconnects between boards be tested after system integration. A number of methods are available for accessing system level boundary scan nets. Traditional methods included using a multi-channel tester to physically access each board, using a single tester connection with each board's TDI and TDO traces daisy chained together or by multiplexing the TMS pins running to each board. An alternative approach is to implement an addressable test access controller such as the SCANPSC110. The SCANPSC110 eliminates the shortcomings of the traditional methods while also providing the capability to partition a single board level scan chain into smaller chains.

While it is possible to separate cables to each board during production test, it becomes unwieldy quickly as the number of boards increase. Furthermore a multiple port solution is not practical for use with embedded test.

Even though daisy chaining multiple boards together is simple, several drawbacks exist. For example, ATPG software for a multiple-board system views the system as if it were one board. As the system scales upward, the number of NETS become large as will the number and length of serial test vectors required. When a board is missing or empty on a backplane, or a fault occurs in the boundary scan infrastructure of any one of the boards, the entire system becomes untestable.

A multiplexed TMS scheme works well for partitioning a system and giving board test access through a single test port. But, it does not scale up well on a backplane, and there is no provision for backplane interconnect testing. Backplane interconnect testing required the ability to park a board in the Pause-DR/IR TAP states (See Section 2, *Figure 4* in the Scan Databook for explanation of TAP states) while accessing another board. It also requires a means for performing system wide updates of scan commands and data.

The PSC110F solution provides a simple means for tying independent scan chains from multi-board systems together and selectively accessing them. A six-bit addressing scheme allows for up to 59 bridges on a single backplane. Test vectors generated for testing the individual boards can be used for testing the boards after system integration as well as for embedded test in the field. The partitioning achieved by using the PSC110F will automatically isolate faults down to the board level with no diagnostics. The multiple local scan ports (LSP) allow for additional partitioning of scan chains within a board. Backplane interconnect testing is enabled through the PARKPAUSE command and broadcast addressing feature. ATPG software is easily implemented and is available through multiple venders.

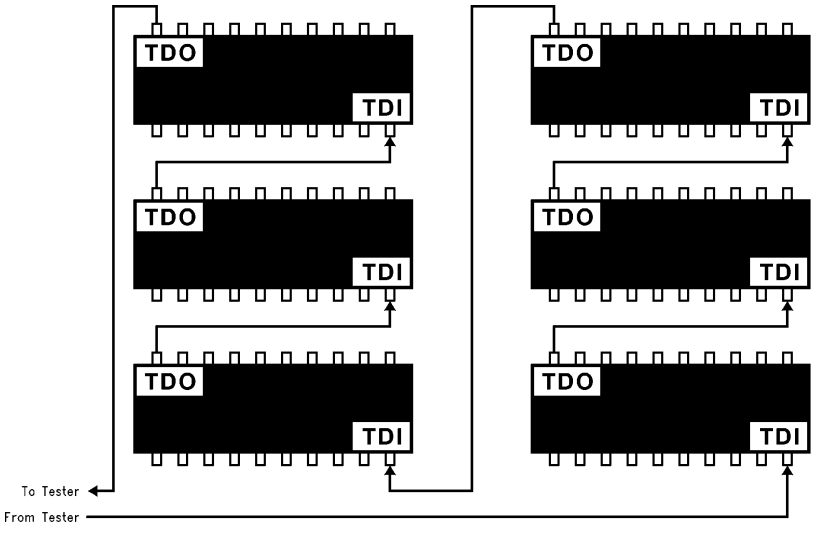

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FIGURE 1. Single Board Boundary Scan Implementation

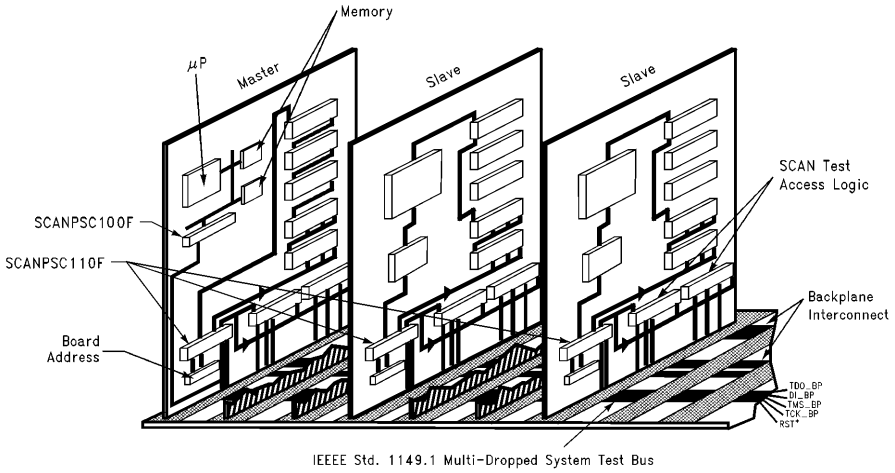

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FIGURE 2. SCANPSC110F Multidrop Configuration

SCANPSC110F APPLICATION EXAMPLE

For more information on this application example, refer to AN-1037 ''Embedded IEEE 1149.1 Test Application Example.''

Consider a system with a multidrop backplane. In general there are ''N'' slots. Some slots are populated with cards, others empty. There may be many different card types that may be used with this backplane, and there may be multiple cards of the same type used within this backplane for a given configuration.

The backplane architecture in this example is quite simple. Each of the N slots receive the same set of multidrop backplane signals. There are no active components on the backplane. However, there may be passive pull-up resistors to hold backplane signals high when tri-stated. The system test bus, (TDO__BP, TDI__BP, TMS__BP, TCK__BP, TRST__BP* (Asynchronous active low input)), is also connected to each slot in a multidrop configuration. Each card has a PSC110F connected to the system test bus, and a boundary scan interface (IEEE 1149.1 compliant drivers, latches, and transceivers such as SCAN18540T, SCAN18373T, SCAN182245T) connected to the system backplane.

SYSTEM WIDE INFRASTRUCTURE TEST

Infrastructure testing is always the first test that must be performed. At the system level, the infrastructure test consists of verification and determination of backplane configuration and then testing connectivity, identity and functionality of the components that make up the output scan chains which interface with the PSC110F LSP's.

VERIFICATION AND DETERMINATION OF BACKPLANE CONFIGURATION

This test sweeps the entire address range of the PSC110F and reads the captured value from the instruction register of a selected PSC110F. The PSC110F instruction register will capture the value ''XXXXXX01'', where ''XXXXXX'' represents the assigned address on the slot inputs. If the value scanned back matches the outgoing address, a PSC110F has been selected. A scanned back value of ''11111111''would indicate that there is no PSC110F at the outgoing address, such as in the case of empty slot. These results can be used in one of two ways:

1. If the exact system configuration is known at test time, which is often the case in production, the results of the address range sweep can be compared to the known configuration. If a PSC110F is not found at an address where there should have been one, or if a PSC110F is found at an address where there should not have been one, the tester will report a failure.
2. If the system configuration is unknown at test time, the results from the address range sweep can be compared to a database containing all possible boards to determine what board types are present in the current configuration of the system. Later when interconnect testing of the cards and backplane is performed, this predetermined configuration is used to select the proper tests for the specific configuration.

LOCAL SCAN PORT INSTRUCTION TEST

After the system configuration is verified or determined, the test circuitry on each card must be tested. This is done by addressing each PSC110F unparking each of its LSP's, and scanning back the value captured by the Instruction Registers of each component in the local chains. A captured value of ''01'' in the least significant bits represents a functioning boundary scan component. In some cases the remaining bits of the Instruction Register capture are used to encode a pseudo ID code (e.g., components like National's SCAN18XXXT, SCAN18XXXA), and can be used to test for correct component placement. Optionally, the device identification register can be checked for each boundary scan component on the cards to check for correct component placement. The 18-bit SCAN ABT Test Access Logic SCAN18XXXA family includes the optional ID register, but some of the earlier boundary scan components were not equipped with the ID register.

BOARD LEVEL INTERCONNECT TESTING VIA SCANPSC110F

The individual boards or cards have already been tested during production. Re-testing after system integration is optional, but makes for a good QA check. In the case of embedded test that will be used for power on self test or periodic field testing, running go/no-go board level tests will enable built-in diagnostics down to the board level.

PSC110F Selection and Configuration

A. Select PSC110F by scanning an address into the PSC110F Instruction Register.

B. Configure the Mode Register for the appropriate local serial port network configuration for board test. If the board has only one scan chain connected to LSP1, the default configuration will be appropriate. If there are multiple chains connected to multiple LSPs on a board with interconnects running between the components of different chains, it is appropriate to unpark multiple LSPs to form what looks like one larger chain.

   The LSP network configuration is performed by:

   1. Scanning the MODESEL command into the selected PSC110F's Instruction Register.
   2. Scanning the appropriate value into the Mode register of the selected PSC110F.

C. Unpark the LSP by scanning the UNPARK command into the instruction register of the selected PSC110F.

Once the PSC110F is selected and its LSPs unparked, the connection is made between the tester and the target scan chains. The remainder of the board test consists of the same commands and test data that would be used for testing a board without the PSC110F with one exception:

The data for the PSC110F Instruction Register, Bypass data register, and PAD bits, must be added to the serial vectors.

The remaining steps for board test are:

D. Scan the SAMPLE/PRELOAD command into the target devices and the BYPASS command to the PSC110F.

E. Scan the first test vector into the boundary registers of the target devices.

F. Scan the EXTEST command into the target devices and the BYPASS command to the PSC110F.

G. Scan the next vector into the target devices; the captured results from the previous vector are shifted out as this vector is shifted in. This step is repeated until all test vectors for this board have been exercised.

H. Scan the GOTOWAIT command into the PSC110F instruction registers to return all PSC110F to the Wait-For-Address state where the next card can be addressed.

BACKPLANE INTERCONNECT TESTING

Testing the backplane is similar to testing NETS within a board with one exception. The nodes of the backplane NETS terminate at components that are connected to a different LSP on a PSC110F. (See *Figure 4*) For example in order to test the I/O lines of a multidrop backplane, say, with 3 cards, each card is connected to the test bus by its own PSC110F. The PSC110F provides the address information. One of the PSC110F's 3 LSPs (local scan ports) is connected to a backplane driver, such as National's SCAN ABT Test Access Logic, SCAN182245A. These drivers, in turn, are connected to the backplane itself, and thereby provide scan test operations for backplane interconnect testing.

Boundary scan ATPG software generates patterns with the assumption that the output cells of all of the components connected to a NET will be updated simultaneously. This assumption allows for one node to drive a NET during pattern i and another node to drive the same NET during pattern i + 1. If the update did not happen simultaneously at the two nodes, there could be significant periods of bus contention between the multiple outputs on a NET. Therefore, the Update-IR of the EXTEST command and all Update-DRs between patterns vectors (while EXTEST is the active command) must be performed simultaneously for all boards using the broadcast address on order to select all PSC110Fs on the backplane. In general, shifting operations must be done by addressing one PSC110F at a time.

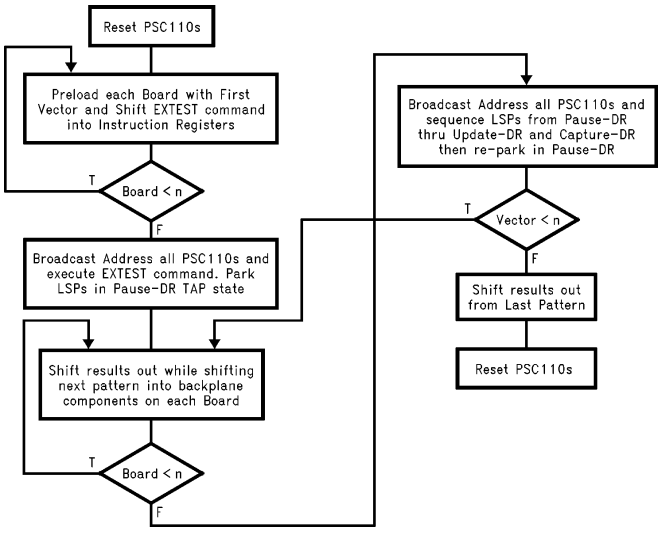

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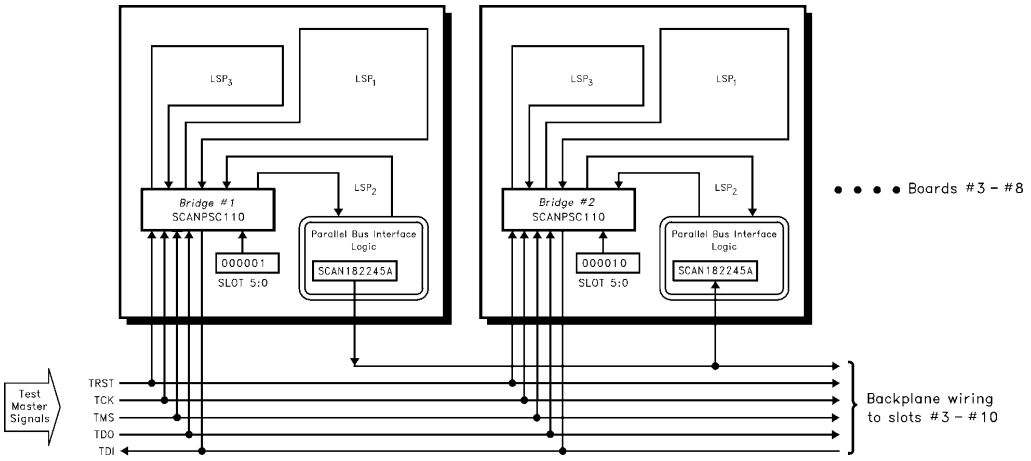
FIGURE 3. Backplane Interconnect Test Flow



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The PSC110F has 3 local scan ports. One port is connected to the backplane drivers. The other two partition the resident board.

FIGURE 4. Testing the Backplane Interconnects

A detailed description of the flow of the backplane interconnect test follows.

I. Reset all PSC110F: This can be performed by forcing TRST low or clocking TCK__BP five times while holding TMS__BP high.

II. Configure/Preload: Preload boundary scan registers of components connected to backplane signals on each card (i = 1 to n) with first test pattern, and shift EXTEST command into the Instruction Registers of all components that interface with the backplane signals.

A. Select PSC110F by scanning an address into the PSC110F Instruction Register.

B. Configure the Mode Register to unpark the LSP that interfaces to the backplane logic. This is not necessary if LSP1 is used (default configuration).

C. Unpark the LSP by scanning the UNPARK command into the Instruction Register of the selected PSC110F.

D. Scan the SAMPLE/PRELOAD command into the target devices and the PARKPAUSE command to the PSC110F.

E. Scan the first test vector into the boundary registers of the target devices. The TAP state sequence should go from Shift-DR to Exit1-DR through the Pause-DR state, after shifting the test vector, to avoid parking the LSP in the Pause-DR state (see PARKPAUSE command in the SCANPSC110F data sheet).

F. Shift the EXTEST command into the target devices and the GOTOWAIT command to the PSC110F. The TAP state sequence should go from Shift-IR to Exit1-IR to Update-IR, after shifting the commands, so that the active LSP will be parked in the Pause-IR state.

G. Repeat for each board involved with the backplane test.

III. Execute EXTEST Command: The EXTEST command is updated to all backplane components simultaneously to avoid significant periods of bus contention that would result from executing the EXTEST command one board at a time.

A. Select all PSC110F by scanning the broadcast address into the PSC110F Instruction Registers.

B. Scan the UNPARK command into the Instruction Register of the selected PSC110F. The LSP will not actually be unparked until the backplane TAP is sequenced back into the Pause-IR state, while the UNPARK command is active.

C. Scan the PARKPAUSE command into the PSC110F instruction register. The TAP state sequence should go from Shift-IR to Exit1-IR through the Pause-IR state, after shifting in the PARKPAUSE command. The LSP will unpark upon entering the Pause-IR state. The EXTEST command had previously been shifted into the Instruction Registers of the target devices and will become the active insruction once the LSP is unparked and sequenced through the Update-IR state.

D. Capture the logic values on the inputs of the target devices and park the LSP in the Pause-DR state by sequencing the backplane TAP's through Capture-DR to Exit1-DR to Update-DR.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

IV. Shift Test Data: Test results from the previous pattern are shifted out while the next pattern is shifted into the boundary registers of the components on each board in the system. Ater the data is shifted, the LSP is parked in the Pause-DR TAP state so that the boundary register contains the new data, but has not yet updated the value in its output cell.

A. Select a PSC110F by scanning an address into the PSC110F Instruction Register.

B. Scan the PARKPAUSE command into the Instruction Register of the selected PSC110F. (The PARKPAUSE command is used to unpark the LSP as well as to park the LSP).

C. Sequence the backplane TAPs into the Pause-DR state in order to unpark the LSP.

D. From the Pause-DR state, transition to Exit2-DR to Shift-IR, where the next test vector is shifted into the target devices, then to Exit1-DR to Update-DR. The LSP will be reparked in the PAUSE-DR state when transitioning from Exit1-DR to Update-DR, because the PARKPAUSE command is still active.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

F. Repeat for each board involved in the backplane test.

V. Drive/Capture: All PSC110F are selected and their LSPs that interface to the backplane components are unparked and sequenced through the Update-DR and Capture-DR states.

A. Select all PSC110F by scanning the broadcast address into the PSC110F Instruction Registers.

B. Scan the PARKPAUSE command into the Instruction Register of the selected PSC110F.

C. Sequence the backplane TAPs to the Pause-DR state in order to unpark the LSP.

D. Sequence from the Pause-DR state through Update-DR through Capture-DR to Exit1-DR to Update-DR. This will execute the next vector and repark the LSP in the Pause-DR state.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

VI. Shift Out Test Results from Last Vector: The test results from the last vector are shifted out while shifting in a safe dummy vector, one that tri-states the bus.

A. Select a PSC110F by scanning an address into the PSC110F Instruction Register.

B. Scan the PARKPAUSE command into the Instruction Register of the selected PSC110F. (The PARKPAUSE command is used to unpark the LSP as well as to park the LSP).

C. Sequence the backplane TAPs to the Pause-DR state in order to unpark the LSP.

D. From the Pause-DR state, transition to Exit2-DR to Shift-IR, where the results of the last test vector are shifted out, to Exit1-DR to Update-DR. The LSP will be reparked in the Pause-DR state when transitioning from Exit1-DR to Update-DR, because the PARKPAUSE command is still active.

E. Scan the GOTOWAIT command into the PSC110F Instruction Registers.

VII. Reset Test Logic: This can be performed by clocking TCK__BP eight (8) times while holding TMS__BP high. It takes three (3) clocks to reset the PSC110F from the Run-Test/Idle state and five (5) more to reset the target components from the Pause-DR state. In general, it takes five (5) TCK's for each level of test hierarchy.

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