National Semiconductor

Device Description and Characteristics

Family Comparison Chart

Depending on system architecture and purpose, devices are selected to optimize system performance. National offers CMOS and BiCMOS SCAN families, and the comparison chart is provided to assist you with your selection criteria. Speed, power, noise drive, etc. may weight differently in importance depending on whether the end system requires computing speed, low standby power, low EMI to meet FCC regulations or must meet any one of many bus standards.

BiCMOS and CMOS Family Comparison

Criteria		Significance	BiCMOS	CMOS
Guaranteed Speed—t_{PLH} ns (A → B)		Faster system performance	6.5	8.5
Static Power I_{CCL} (Outputs Low)		Lower quiescent supply current, less power consumption, and less cooling required	65 mA	0.8 mA
Guaranteed Dynamic Power I_{CCD} (mA/MHz)		Lower system power consumption under heavier loading conditions	0.2 (Note 3)	not specified
Ground Bounce V_{OLP} (5V, 25°C)		Less data disruption, especially when switching multiple outputs at one time	not specified	1.5
Dynamic Threshold (5V, 25°C)	V_{ILD}	Less data disruption, especially when connected to a bus	0.8	0.8
	V_{IHD}		2.0	2.0
Packaging		Compatible with 16-bit wide pinout	SSOP	SSOP
Capacitance	C_{IN} (pF)	Lower capacitance means less bus loading, notwithstanding frequency	5.9	4.0
	$C_{I/O}$ (pF)		13.7	20
Output Drive (mA)	I_{OL}		15	64
	I_{OH}		−32	−32
ESD (Note 4)		Easier handling	>2000V	>2000V

NG = Not Guaranteed; NA = Not Available; NS = Not Specified

Assumptions: Device is SCAN18245T CMOS and SCAN182245A BiCMOS

Note 1: V_{OLP} is measured on '244 function.

Note 2: Specified with 8 outputs switching and no load.

Note 3: I_{CCD} measured 1 bit toggling, 0V to 5V, 50% duty cycle, outputs loaded with 50 pF, no resistor.

Note 4: Typical values for HBM ESD.

SCAN ABT Test Access Logic

When these functions are added to the card edge going into the backplane, users gain these benefits:

— Live insertion

— Removal of boards without having to power down the system

This saves time and eliminates those unwelcome sparks!

Here are other SCAN ABT features:

— 25Ω series resistors on the outputs reduce ringing (noise) and eliminate the need for an external ''damping'' resistor. In the past, this was used to reduce noise on CMOS or FCT products.

— SCAN ABT will power up in TRI-STATE®. Beyond allowing live insertion and board removal, it enables system power partitioning by electronically switching them offline to save on power. This is particularly beneficial in remote locations that experience power shortages.

— SCAN ABT has reduced power during power-up and power-down TRI-STATE. This reduces the loading on the bus to which it is attached, taking less time to charge up all of the capacitance on the circuit using SCAN ABT, and allowing the bus to run faster.

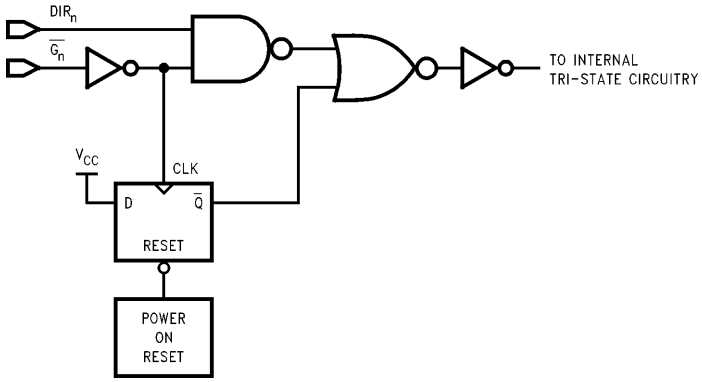
For more information on power-up and power-down characteristics refer to Application Note AN-881, *''Design Considerations for Fault Tolerant Backplanes,''* found in Section 7.

SCAN ABT Live Insertion and Power Cycling Characteristics

SCAN ABT is intended to serve in live insertion backplane applications. It provides 2nd Level Isolation[1] which indicates that while external circuitry to control the output enable pin is unnecessary, there may be a need to implement differential length backplane connector pins for V_{CC} and GND. As well, pre-bias circuitry for backplane pins may be necessary to avoid capacitive loading effects during live insertion.

SCAN ABT provides control of output enable pins during power cycling via the circuit in *Figure 1*. It essentially controls the $\overline{G_n}$ pin until V_{CC} reaches a known level.

During *power-up*, when V_{CC} ramps through the 0.0V to 0.7V range, all internal device circuitry is inactive, leaving output and I/O pins of the device in high impedance. From approximately 0.8V to 1.8V V_{CC}, the Power-On-Reset circuitry, (POR), in *Figure 1* becomes active and maintains device high impedance mode. The POR does this by providing a low from its output that resets the flip-flop The output, $\overline{Q}$, of the flip-flop then goes high and disables the NOR gate from an incidental low input on the $\overline{G_n}$ pin. After 1.8V V_{CC}, the POR circuitry becomes inactive and ceases to control the flip-flop. To bring the device out of high impedance, the $\overline{G_n}$ input must receive an inactive-to-active transition, a high-to-low transition on $\overline{G_n}$ in this case to change the state of the flip-flop. With a low on the $\overline{Q}$ output of the flip-flop, the NOR gate is free to allow propagation of a $\overline{G_n}$ signal.



TL/F/12133–2

FIGURE 1

[1]Section 7, *Design Considerations for Fault Tolerant Backplanes,* Application Note AN-881.

SCAN ABT Live Insertion and Power Cycling Characteristics (Continued)

During *power-down*, the Power-On-Reset circuitry will become active and reset the flip-flop at approximately 1.8V V_{CC}. Again, the $\overline{Q}$ output of the flip-flop returns to a high and disables the NOR gate from inputs from the $\overline{G_n}$ pin. The device will then remain in high impedance for the remaining ramp down from 1.8V to 0.0V V_{CC}.

Some suggestions to help the designer with live insertion issues:

- The $\overline{G_n}$ pin can float during power-up until the Power-On-Reset circuitry becomes inactive.
- The $\overline{G_n}$ pin can float on power-down only after the Power-On-Reset has become active.

The description of the functionality of the Power-On-Reset circuitry can best be described in the diagram of *Figure 2.*

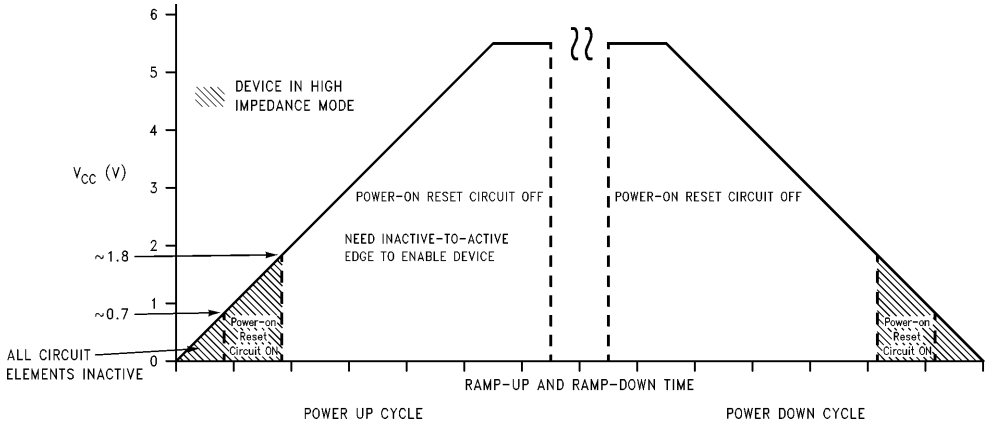


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FIGURE 2. SCAN ABT Includes Additional Power-On Reset Circuitry Not Otherwise Included in ABT Devices

ABT Circuit and Design Architecture

SCAN ABT performs as ABT devices, except as where noted.

The circuitry for an ABT non-inverting Buffer with TRI-STATE control logic is shown in *Figure 3*. Robust bipolar components form the dual rail ESD protection networks for both input and output structures. The Q6 and D6 ESD circuits provide protection to the V_{CC} rail and have a high enough breakdown voltage rating to remain high impedance ($I_{ZZ} < 100\ \mu A$) during powered-down applications. The Schottky transistors Q5, Q7 and Q8 provide protection to the Ground rail and double functionally as highly conductive undershoot clamps.

The TRI-STATE output structure is formed with Bipolar components to produce high drive ($I_{OL} = 64$ mA; $I_{OH} = -32$ mA) and high speed TTL compatible logic swings. The pull-up stage utilizes cascaded emitter followers Q3 and Q4 to provide high source current drive for the charging of capacitive loads. The no-load TTL compatible V_{OH} level is one forward-biased V_{BE} (Q3) drop and one forward-biased V_{FD} Schottky diode (D4) drop below the V_{CC} rail yielding typical 3.8V V_{OH} at 5V V_{CC}, 25°C and 10 μA source current. The ON source impedance of this pull-up stage is typically less than 10Ω for source currents between −5 mA to −40 mA at 25°C. This initial low impedance turn-on characteristic allows the pull-up stage to easily provide a V_{OH} level of 2V minimum at I_{OH} source current of −32 mA over the operating V_{CC} and temperature ranges. At 25°C and source currents above −50 mA, the pull-up stage becomes limited by voltage drop across the RI_{OS} resistor and the effective source impedance becomes 25Ω typically. Schottky diodes D3, D4 and D5 also provide blocking to insure that the pull-up stage remains high impedance during power down applications.

When the output is enabled by a logic low on the $\overline{OE}$ input and a logic high is on the Data input, the base of Q3 is driven to the V_{CC} rail by the CMOS inverter in the data path. The open drain CMOS NAND gate is logic high-open (non-conducting) and allows the base of Q4 to be driven ON by Q3. The CMOS NOR gate goes low turning Q1 OFF and turning ON the CMOS AC/DC Miller Killer circuitry which grounds the base of Q2, quickly turning it OFF. This circuitry provides an active shunt for any charge coupled by the Miller Effect of the Q2 collector-base capacitance during the low to high output transition. Use of this active circuitry improves output rise time and serves to reduce simultaneous conduction of pull-up and pull-down stages during LH transitions. The AC/DC Miller Killer circuit is also active when the output goes to TRI-STATE to prevent Q2 base injection by the LH transitions of other outputs on a bus, therefore dynamic bus loading will be capacitive only.

Power Down Miller Killer circuitry at the base of Q2 is inactive when V_{CC} is applied. When V_{CC} is powered down, the Power Down Miller Killer circuitry provides an active shunt to transient energy coupled to the Q2 base by its collector base capacitance. This prevents momentary turn-on of Q2 during LH transitions in partial power down bus applications and maintains the powered off output as only a Hi-Z light capacitive load ($I_{ZZ} < 100\ \mu A$) to the bus.

Note that Q1 drives only the Q2 pull-down stage and does not function as the Phase Splitter driver typical of TTL logic. The pull-up stage is controlled by CMOS logic independent of Q1. This feature allows the input threshold voltages for the CMOS logic driving the pull-up stage to be set independent of the logic driving the pull-down stage.

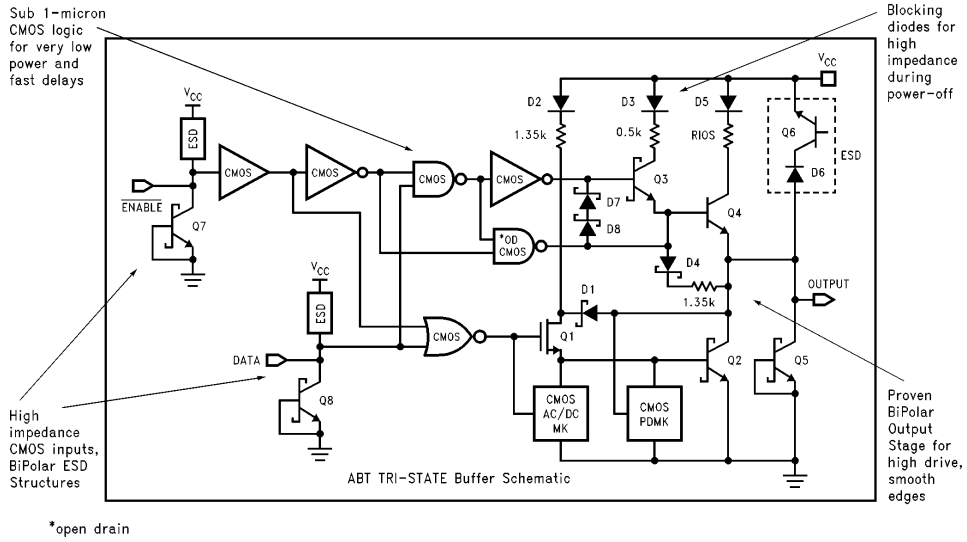

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FIGURE 3. Basic ABT TRI-STATE Buffer Schematic

ABT Circuit and Design Architecture (Continued)

The transfer function for the non-inverting ABT Buffer shown in *Figure 4* indicates that the data input switching threshold for the pull-down stage is approximately 200 mV lower than the pull-up stage. As the Data input is swept from logic LOW to logic HIGH, the output switches from active LOW to high impedance at an input threshold of about 1.3V at 25°C and a V_{CC} of 5.0V. When the input reaches about 1.5V, the output switches from high impedance to HIGH. This design feature serves to reduce simultaneous conduction of the stages during switching. Also, the 200 mV offset in Data input switching thresholds acts like hysteresis and causes the buffer to be very tolerant of slow data input edge rates, i.e., edge rates slower than 10 ns/V can easily be tolerated without output oscillation. The switching threshold is proportional to V_{CC} as indicated in *Figure 5* and is quite stable as a function of temperature as indicated by *Figure 6*.

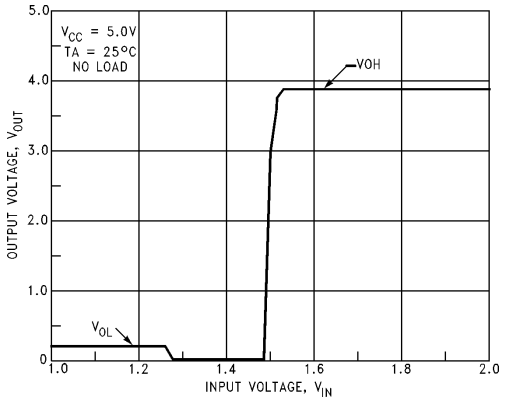

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FIGURE 4. Buffer Transfer Function @ Room Temperature V_{CC} = 5V, T_A = 25°C, No Load

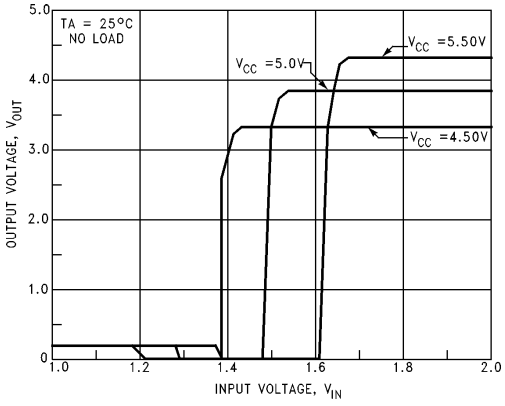

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FIGURE 5. Transfer Function vs V_{CC} T_A = 25°C, No Load

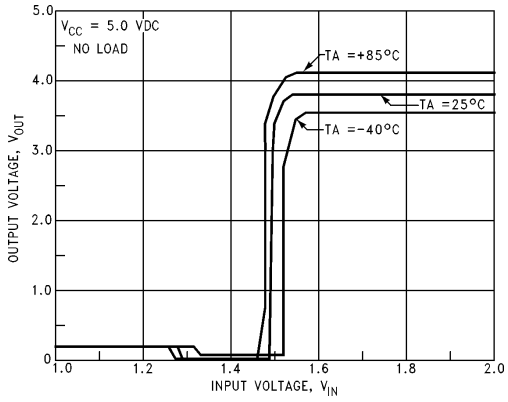

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FIGURE 6. Transfer Function vs Temperature V_{CC} = 5V DC, No Load

With the output enabled by a LOW on the $\overline{OE}$ input, a LOW on the Data input forces active LOWS on both the CMOS inverter and the open drain CMOS NAND gate outputs, which then simultaneously turn OFF Q3 and Q4. The CMOS NOR gate output goes HIGH, turning the AC/DC Miller Killer circuitry OFF and Q1 ON to drive Q2 ON. Q2 is designed to easily sink 64 mA I_{OL}, at $V_{OL} < 0.55V$. During HL output transitions, Schottky diode D1 assists the pull-down stage in providing a low impedance discharge path for the output load capacitance. As the stage turns on, part of the charge on the output load passes through D1 and Q1 to momentarily increase the base drive to Q2 and increase Q2's current sink capability. See output characteristics in *Figure 7*, I_{OL} vs V_{OL}.

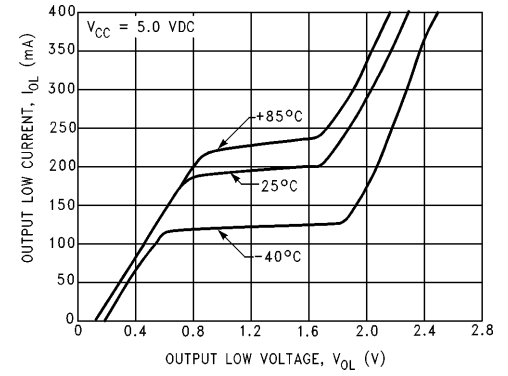

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FIGURE 7. Output Low Characteristics V_{CC} = 5V DC

ABT Circuit and Design Architecture (Continued)

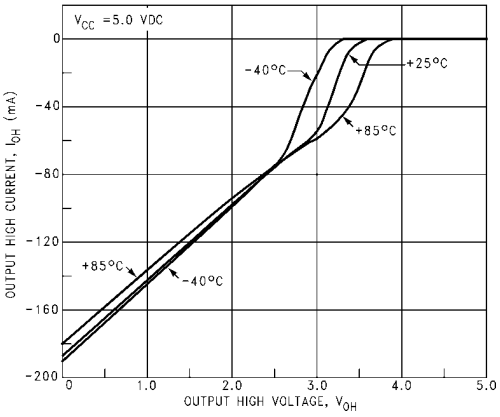

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FIGURE 8. Output High Characteristics V_{CC} = 5V DC

When the output is disabled by a HIGH on the $\overline{OE}$ input, the enable CMOS logic quickly overrides the Data path logic and cuts off drive to whichever stage is ON. In the case of an LZ transition, the CMOS NOR gate is driven LOW turning OFF Q1 and turning ON the AC/DC Miller Killer circuitry to insure Q2 is quickly turned off. In the case of a HZ transition, the CMOS inverter goes hard LOW to turn off Q3 and quickly discharge the base of Q4 through Schottky diodes D7 and D8. The effect of disable time (t_{PLZ}, t_{PHZ}) being typically faster than enable time (t_{PZL}, t_{PZH}) inherently helps avoid bus contention.

Since the CMOS Enable logic remains active to V_{CC}'s well below 2V, high impedance control can be maintained to V_{CC} voltages below the turn-on V_{CC} thresholds of the Bipolar output stage. This insures the capability for glitch free power ON/OFF high impedance outputs with the provision that the $\overline{OE}$ input is maintained logic HIGH at or greater than the data sheet specified 2.0V minimum V_{IH} during the V_{CC} power ramp. However, since the CMOS logic switching threshold varies proportional to V_{CC}, a practical worst case $\overline{OE}$ logic high of 2.0V or 50% of V_{CC}, will maintain the power ON/OFF TRI-STATE condition during the V_{CC} transition.

ABT is designed to be tolerant of controlled live insertion at the PCB level. Controlled means that the insertion or removal methodology is accomplished in such a way that power to the PCB is applied in a preferred sequence and that control signals are provided to the PCB also in the preferred sequence such that output control is asserted to prevent contention of outputs attached to a bus during the power up or down sequence.

Tolerant means that ABT is designed and guaranteed to behave in a predictable manner during controlled PCB live insertion in systems requiring fault-tolerant or noninterruptable applications. Additionally, ABT has features which facilitate design of systems which must utilize power partitioning for redundant circuitry or for powering saving of inactive circuits.

All ABT input, output, and I/O pins are protected with robust Bipolar components with respect to both V_{CC} and Ground rails. This circuitry is designed to withstand 2000V (Human Body Model) and also to provide clamping action for voltage undershoot while preserving low capacitive loading of the pin. The clamping action by the undershoot clamp begins aggressively at voltages more negative than -0.5V relative to Ground, but this clamp remains non-conductive at voltages up to 7V. Relative to the V_{CC} rail, the ESD circuitry begins clamping only at voltages greater than 5.5V above V_{CC}. These ESD circuits remain high impedance and non-conductive for applied input or output voltages between -0.4V to 5.5V with V_{CC} = 0V to 5.5V.

ABT CMOS input stages are Hi-Z with or without V_{CC} applied. The I_{IL}, I_{IH}, and I_{BVI} datasheet specification guarantees high DC impedance for inputs with V_{CC} applied. The V_{ID} specification guarantees Hi-Z inputs with V_{CC} = 0V.

High impedance output and I/O pins are capable of maintaining Hi-Z status with V_{CC} = 0 and during the application or removal of V_{CC}. The ABT data sheet parameters I_{OZH} and I_{OZL} guarantee < 50 μA output leakage for applied V_{OUT} voltages of 2.7V or 0.5V at any V_{CC} between 5.5V and 0V with the output disabled and with the appropriate logic input voltage maintained on the $\overline{OE}$ input pin. An additional I_{ZZ} bus drainage specification guarantees < 100 μA output leakage at V_{OUT} = 5.5V with V_{CC} = 0V. Therefore, ABT outputs are guaranteed to remain glitch-free during the power cycle and at power down V_{CC} = 0V. Refer to Application Section for a more detailed discussion of live insertion and powerup/down TRI-STATE capabilities of ABT.

Threshold and Noise Margin

Figure 9 describes the input signal voltage levels for use with ABT products. The AC testing input levels follow industry convention which require 0.0V for a logic LOW and 3.0V level for a logic HIGH. DC input levels are typically 0.0V to V_{IL}, and high input levels are typically V_{IH} to V_{CC}. DC testing uses a combination of threshold and hard levels to assure datasheet guarantees. Input threshold levels are usually guaranteed through V_{OL} and V_{OH} tests.

High level noise immunity is the difference between V_{OH} and V_{IH} and low level noise immunity is the difference between V_{IL} and V_{OL}. Noise-free V_{IH} or V_{IL} levels should not induce a switch on the appropriate output of an ABT device. When testing in an automated environment, extreme caution should be taken to ensure that input levels plus noise do not go into the transition region.

Dynamic System Power Dissipation

One of several advantages to using BiCMOS logic is its low power when compared to bipolar technologies. As well, it has reduced dynamic output power because of the reduced output swing in comparison to CMOS devices. In the static or quiescent high state, SCAN ABT will consume power like a pure CMOS device, and in the quiescent low state all power goes to driving the bipolar output pull-down transistor.

Total power consumption under AC conditions comes from three sources; quiescent power, internal dynamic power, and output dynamic power.

In other words: $P_{TOTAL} = P_{DQ} + P_{DINT} + P_{DOUT}$

Where:

- P_{TOTAL} = Total Power Dissipation
- P_{DQ} = Quiescent Power Dissipation
- P_{DINT} = Internal Dynamic Power Dissipation
- P_{DOUT} = Output Power Dissipation

First the Quiescent power can be derived from the following equation.

$$P_{DQ} = \left[\frac{I_{CCL}}{N} * N_{QOL} * V_{CC}\right] + \left[D_{ICC} * N_{QIH} * V_{CC}\right] + \left[\frac{I_{CCH}}{N} * N_{QOH} * V_{CC}\right]$$

Where:

- P_{DQ} = Quiescent Power Dissipation
- I_{CCH} = Quiescent Power Supply Current with All Outputs High
- I_{CCL} = Quiescent Power Supply Current with All Outputs Low
- N_{QOL} = Number of Quiescent Outputs Low
- N_{QOH} = Number of Quiescent Outputs High
- N_{QIH} = Number of Quiescent Inputs High
- N = Number of Active Outputs
- DI_{CC} = Power Supply Current for Input with V_{IN} other than V_{CC}

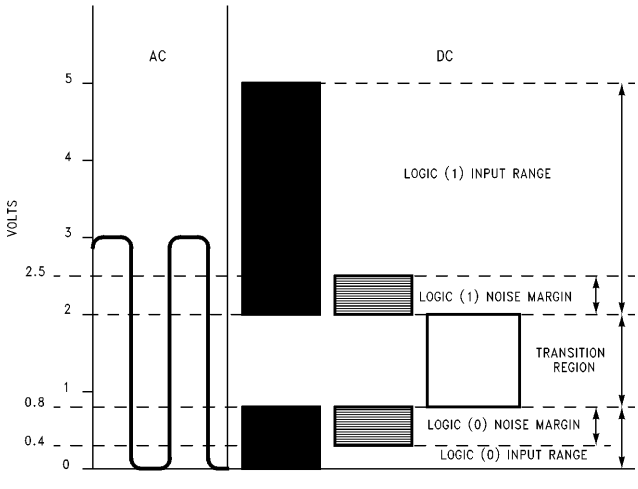

FIGURE 9

Dynamic System Power Dissipation (Continued)

Secondly, a SCAN ABT device will dissipate power internally by charging and discharging internal capacitiance. The following equation takes into account the duty cycle of inputs and outputs and current due to the internal switching of capacitances.

$$P_{DINT} = [(DI_{CC}*DH*NS)*V_{DD}] + \left[\left(\frac{I_{CCL}}{N}*NS*DL\right)*V_{CC}\right] + [(I_{CCD}*f*NS)*V_{CC}]$$

Where:

P_{DINT} = Internal Dynamic Power Dissipation

V_{CC} = Power Supply Voltage

DI_{CC} = Power Supply Current for Input with V_{IN} other than V_{CC} (For example, a typical TTL input voltage is considered to be 3.4V)

Note: The farther away an input (V_{IN}) is from threshold (1.5V), the less power supply current the IC will consume.

N = Number of Active Outputs

DH = Duty Cycle for Switching Inputs High

DL = Duty Cycle for Switching Outputs Low

I_{CCL} = Data book specification for power supply current with all outputs low

I_{CCD} = Power consumption coefficient (mA/MHz) for 1-bit toggling

f = Frequency of Outputs

NS = Number of Outputs Switching

Finally, at high frequencies a significant amount of current is consumed by a device to drive its output load. SCAN ABT has an advantage here because of its reduced output swing compared to CMOS devices. For a simple case, if we assume only capacitive components to the load, we can use the following equation.

$$P_{OUT} = [C_L * VS * f] * V_{CC}$$

Where:

P_{DOUT} = Output Power Dissipation

C_L = Load Capacitance

VS = Output Voltage Swing

f = Output Operating Frequency

V_{CC} = Power Supply Voltage

Take for an example a SCAN182244A with all 18 outputs switching at 16 MHz. How much power would be consumed by the IC in this case?

Assumptions:

1. $V_{CC} = 5V$
2. The data and control inputs are being driven with 0V and 3.4V voltages for logic levels.
3. Data input frequency = 16 MHz @ 50% duty cycle.
4. $C_L = 50$ pF
5. There are no DC loads on the outputs, i.e., outputs are either unterminated or terminated with an AC shunt termination.
6. Since the output high voltage is produced by a Darlington transistor pair, the output voltage swing will be assumed to be $V_{CC} - 1.6V$ or $5.0 - 1.6V = 3.4V$. Therefore VS = 3.4V with $V_{CC} = 5.0V$.

For quiescent current, all data inputs and outputs are switching leaving only the 2 $\overline{OE}$ inputs static low.

$$P_{DQ} = \left[\frac{I_{CCL}}{N}*N_{QOL}*V_{CC}\right] + [DI_{CC}*N_{QIH}*V_{CC}] + \left[\frac{I_{CCH}}{N}*N_{QOH}*V_{CC}\right]$$

$$= 0 + 0 + 0 = 0$$

Internal Dynamic Current

$$P_{DINT} = [(DI_{CC}*NS*DH)*V_{DD}] + [(\frac{I_{CCL}}{N}*NS*DL)*V_{CC}] + [\ (I_{CCD}*f*NS)*V_{CC}]$$

$$P_{DINT} = [(2.5e-3*18*0.5)*5.0] + [(\frac{30e-3}{18}*8*0.5)*5.0] + [(0.1*16*18)*5.0]$$

$$= 5.60 + 1.66 + 144$$

$$= 151.3 \text{ mW}$$

Finally the Output Current

$$P_{OUT} = [C_L * VS * f] * V_{CC}$$

$$P_{OUT} = [50.e-12*3.4V*16e6] * 5.0$$

$$= [2.72e-3]*5$$

$$= 13.5 \text{ mW}$$

$$P_{TOTAL} = P_{DQ} + P_{DINT} + P_{DOUT}$$

$$= 0 + 151.3 \text{ mW} + 13.5 \text{ mW}$$

$$P_{TOTAL} = 164.8 \text{ mW}$$

ABT Process Characteristics

PROCESS CHARACTERISTICS

National's 1.0 BCT combines bipolar and CMOS transistors in a single process to achieve high speed, high drive characteristics while maintaining low tri-state power and the ability to control noise.

National's 1.0 BCT provides a suitable platform for migration to higher performance levels with minor technology enhancements planned for the near future. In its present form, the technology supports Interface, Digital, Bus and Telecom products from National Semiconductor.

PROCESS FEATURES

- 18 masking layers using stepper lithography
- 100% ion implantation utilized for dopant placement
- Localized retrograde wells tailored for high performance
- Optimized recessed and field isolation sequence for CMOS/bipolar
- NMOS LDD (Lightly Doped Drain), PMOS Halo architecture
- 150Å gate oxide
- Self aligned bipolar contact set utilizing minimum geometries
- Localized retrograde sub-emitter collector
- Advanced planarization on all topographies
- PtSi Schottky diodes, all contacts use platinum for resistance reduction
- Barrier metal of TiW
- Dual layer metal of Al-Cu 0.3% for long term reliability
- Metal pitch of 3.5 microns

PROCESS FLOW

1.0 Buried Layer
2.0 P-Well
3.0 N-Well
4.0 Isolation
5.0 Sink
6.0 Active
7.0 Active Strip
8.0 Poly
9.0 Base
10.0 Bipolar Contact
11.0 Emitter
12.0 P+ Source/Drain
13.0 N+ Source/Drain
14.0 Contact
15.0 Metal 1
16.0 Via
17.0 Metal 2
18.0 Passivation

PROCESS PARAMETERS

- Bipolar Performance: 10 GHz Ft with gains greater than 100
- CMOS Performance: 0.5 μm min Leff
- Platinum Schottky diodes for TTL
- Typical ESD Performance: >2000V, Human Body Method
- Robust latch-up and punch-through protection with retrograde wells
- Advanced interconnect supports superior temperature cycle performance

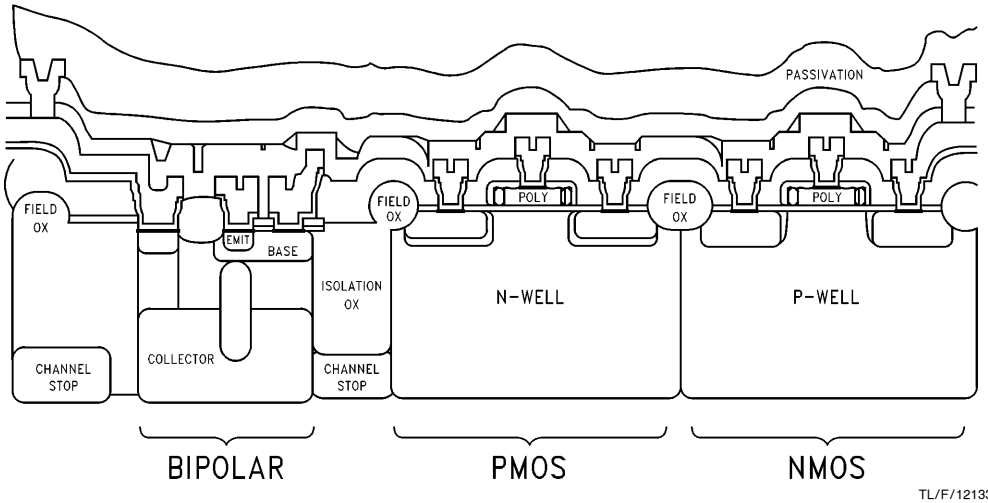

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FIGURE 10. 1.0 μm BCT Process Cross Section

SCAN CMOS Test Access Logic

SCAN CMOS features low power consumption. Products are used in board test by surrounding clusters of non-boundary scan devices to create a fully 1149.1 compliant board. SCAN CMOS provides adequate drive and buffering for microprocessors, too. For more information on Advanced CMOS devices, refer to the FACT Databook.

SCAN CMOS logic is manufactured on a 1.3 μm process and offers a good combination of high speed, low power dissipation, high noise immunity, wide fanout capability and high reliability.

Characteristics

Meets or Exceeds JEDEC Standards for 74ACXX

Family

High Performance Outputs
- — Common Output Structure
- — Output Sink/Source Current of −24/48 mA
- — Transmission Line Driving 50Ω (Commercial)/75Ω (Military) Guaranteed

Temperature Range

— Commercial	−40°C to +85°C
— Military	−55°C to +125°C

Improved ESD Protection Network

High Current Latch-Up Immunity

Patented Noise Suppression Circuitry

Noise Immunity

The DC noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The input threshold of a device and the output voltage, $|V_{IL} - V_{OL}|/|V_{IH} - V_{OH}|$ at 4.5V V_{DD}, for SCAN CMOS is 1.25V/1.25V.

Noise Characteristics

The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of SCAN CMOS.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture or Equivalent
Tektronics Model 7854 Oscilloscope or Equivalent

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the word generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. Swap out the channels that have more than 150 ps of skew until all channels being used are within 150 ps. It is important to deskew the word generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set V_{DD} to 5.0V.
5. Set the word generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and affect the results of the measurement.
6. Set the word generator input levels at 0V LOW and 3V HIGH. Verify levels with a digital volt meter.

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV}:

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.

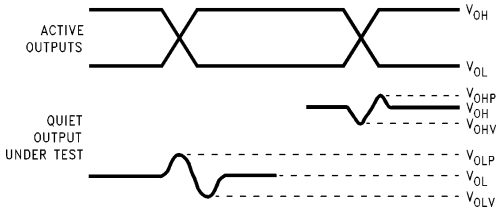

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FIGURE 11. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

- Measure V_{OLP} and V_{OLV} on the quiet output LOW during the HL transition. Measure V_{OHP} and V_{OHV} on the quiet output HIGH during the LH transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD}:

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL}, until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD}.
- Next decrease the input HIGH voltage level on the word generator, V_{IH} until the output begins to oscillate. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD}.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

Noise Characteristics (Continued)

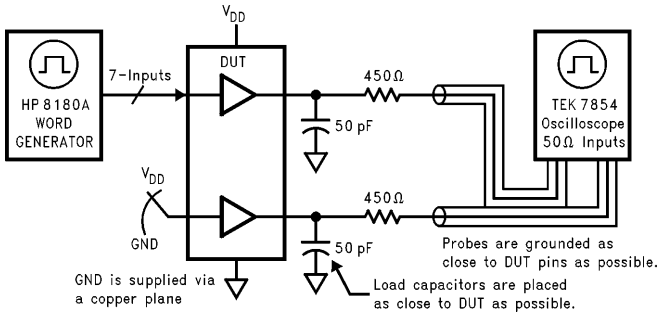

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FIGURE 12. Simultaneous Switching Test Circuit

Output Characteristics

All SCAN CMOS outputs are buffered to ensure consistent output voltage and current specifications. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All SCAN CMOS devices are guaranteed to source 48 mA and sink −24 mA. Commercial devices are capable of driving 50Ω transmission lines.

Circuit Characteristics

POWER DISSIPATION

One advantage to using CMOS logic is its extremely low power consumption. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Total power dissipation of SCAN CMOS device under AC conditions is a function of three basic sources, quiescent power, internal dynamic power, and output dynamic power dissipation.

Firstly, a SCAN CMOS device will dissipate power in the quiescent or static condition. This can be calculated by using the formula: (Note: In many datasheets I_{DD}, ΔI_{DD}, I_{DDT}, and V_{DD} are referred to as I_{CC}, ΔI_{CC}, I_{CCT}, and V_{CC}, respectively. There are no differences.)

Eq. 1 $PD_Q = I_{DD} \bullet V_{DD}$

PD_Q = Quiescent Power Dissipation
I_{DD} = Quiescent Power Supply Current Drain
V_{DD} = Power Supply Voltage

Secondly, a SCAN CMOS device will dissipate power dynamically by charging and discharging internal capacitance. This can be calculated by using the following formula:

Eq. 2.

$$PD_{INT} = [(I_{DDT} \bullet D_H \bullet N_T) \bullet V_{DD}] + [(C_{PD} \bullet V_S \bullet f) \bullet V_{DD}]$$

PD_{INT} = Internal Dynamic Power Dissipation
I_{DDT} = Power Supply Current for a TTL HIGH Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs HIGH
N_T = Number of TTL Inputs at D_H
V_{DD} = Power Supply Voltage
C_{PD} = Device Power Dissipation Capacitance
V_S = Output Voltage Swing
f = Internal Frequency of Operation

C_{PD} values are specified for each device and are measured per JEDEC standards as described in this section. On device data sheets, C_{PD} is a typical value and is given either for the package or for the individual stages with the device. V_S and V_{DD} are the same value and can be replaced by V_{DD}^2 in the formula.

Thirdly, a SCAN CMOS device will dissipate power dynamically by charging and discharging any load capacitance. This can be calculated by using the following formula:

Eq. 3 $PD_{OUT} = (C_L \bullet V_S \bullet f) \bullet V_{DD}$

PD_{OUT} = Output Power Dissipation
C_L = Load Capacitance
V_S = Output Voltage Swing
f = Output Operating Frequency
V_{DD} = Power Supply Voltage

Circuit Characteristics (Continued)

In many cases the output frequency is the same as the internal operation frequency. Also V_S is similar to V_{DD} and can be replaced by V_{DD}^2.

The total device power dissipation is the sum of the quiescent power and all of the dynamic power dissipation. This is best described as:

Eq. 4 $PD_{TOTAL} = PD_Q + PD_{DYNAMIC}$ or
$PD_{TOTAL} = PD_Q + PD_{INT} + PD_{OUT}$

The following is an exercise in calculating total dynamic I_{DD} for SCAN CMOS. The device used as an example is the SCAN18245T. Static I_{DD}, I_{DDT} and C_{PD} numbers can be found in the datasheet. I_{DD} numbers used will be worst-case commercial guarantees. Room temperature power will be less. These are approximate worst-case calculations.

The following assumptions have been made:

1. I_{DD} will be calculated per input/output (as per JEDEC C_{PD} calculations). The total for the SCAN18245T will be the calculated $I_{DD} \times 18$.
2. Worst case conditions and JEDEC would require that the data is being toggled at the clock frequency in order to change the outputs at the maximum rate (½ CP).
3. The data and clock input signals are derived from TTL level drivers (0V to 3.0V swing) at 50% duty cycle.
4. The clock frequency is 16 MHz.
5. I_{DD} will be calculated for $C_L = 50$ pF.
6. $V_{DD} = 5V$.
7. Total POWER dissipation can be obtained by multiplying total I_{DD} by V_{DD} (5.0V).
8. Quiescent I_{DD} will be neglected in the total I_{DD} calculation because it is 1000 times less than dynamic I_{DD}.
9. There is no DC load on the outputs, i.e. outputs are either unterminated or terminated with series or AC shunt termination.

The I_{DD} calculations are as follows:

I_{DD} Total = Input I_{DD} + Internal Switching I_{DD} + Output Switching (AC load) I_{DD}

Input I_{DD} = $(I_{DDT}) \times$ (number of TTL inputs) $\times$ (Duty Cycle)
= $(2 \times 10^{-3}) \times (1) \times (0.50)$
= 1.0 mA per input being toggled at TTL levels

Internal I_{DD} = $(V_{SWING}) \times (C_{PD}) \times$ (CP freq)
= $(5.0) \times (41 \times 10^{-12}) \times (16 \times 10^{+6})$
= 3.28 per mA per input being toggled by CP

Output I_{DD} = $(V_{SWING} \times (C_L) \times$ (Q freq)
C_L = 50 pF
= $(5.0) \times (50 \times 10^{-12}) \times (8 \times 10^{+6})$
= 2 mA per output toggled at ½ CP

Adding Input, Internal and Output I_{DD} together and multiplying by 18 I/O per SCAN18245T, the approximate worst-case I_{DD} calculations are as follows:

C_L = 50 pF I_{DD} total = 100.48 mA or 502.4 mW* at a CP of 16 MHz

(*Power is obtained by multiplying I_{DD} by V_{DD})