National Semiconductor

Loading Specifications, Waveforms, Quality and Reliability

Definition of Terms

DC Characteristics

Currents: Positive current is defined as conventional current flow into a device. Negative current is defined as current flow out of a device. All current limits are specified as absolute values.

Voltages: All voltages are referenced to the ground pin. All voltage limits are specified as absolute values.

I_{BVI} Input HIGH Current (Breakdown Test). The current flowing into an input when a specified Absolute MAX HIGH voltage is applied to that input.

I_{BVIT} I/O Pin HIGH Current (Breakdown Test). The current flowing into a disabled (output is high impedance) I/O pin when a specified Absolute MAX HIGH voltage is applied to that I/O pin.

I_{CEX} Output HIGH Leakage Current. The current flowing into a HIGH output due to the application of a specified HIGH voltage to that output.

I_{CCH} The current flowing into the V_{CC} supply terminal when the outputs are in the HIGH state.

I_{CCL} The current flowing into the V_{CC} supply terminal when the outputs are in the LOW state.

I_{CCT} Additional I_{CC} due to TTL HIGH levels forced on CMOS inputs.

I_{CCZ} The current flowing into the V_{CC} supply terminal when the outputs are disabled (high impedance).

I_{IL} Input LOW Current. The current flowing out of an input when a specified LOW voltage is applied to that input.

I_{IH} Input HIGH Current. The current flowing into an input when a specified HIGH voltage is applied to that input.

I_{OH} Output HIGH Current. The current flowing out of an output which is in the HIGH state.

I_{OL} Output LOW Current. The current flowing into an output which is in the LOW state.

I_{OS} Output Short Circuit Current. The current flowing out of an output in the HIGH state when that output is shorted to ground (or other specified potential).

I_{OZL} Output OFF current (LOW). The current flowing out of a disabled TRI-STATE® output when a specified LOW voltage is applied to that output.

I_{OZH} Output OFF current (HIGH). The current flowing into a disabled TRI-STATE output when a specified HIGH voltage is applied to that output.

I_{ZZ} Bus Drainage. The current flowing into an output or I/O pin when a specified HIGH level is applied to the output or I/O pin of a power-down device.

V_{CC} Supply Voltage. The range of power supply voltages over which the device is guaranteed to operate.

V_{CD} Input Clamp Diode Voltage. The voltage on an input (−) when a specified current is pulled from that input.

V_{ID} Input Breakdown Voltage. The voltage on an input of a powered-down device when a specified current is forced into that input.

V_{IH} Input HIGH Voltage. The minimum input voltage that is recognized as a DC HIGH-level.

V_{IHD} Dynamic Input HIGH Voltage. The minimum input voltage that is recognized as a HIGH-level during a Multiple Output Switching (MOS) operation.

V_{IL} Input LOW Voltage. The maximum input voltage that is recognized as a DC LOW-level.

V_{ILD} Dynamic Input LOW Voltage. The maximum input voltage that is recognized as a LOW-level during Multiple Output Switching (MOS) operation.

V_{OH} Output HIGH Voltage. The voltage at an output conditioned HIGH with a specified output load and V_{CC} supply voltage.

V_{OHV} Minimum (valley) voltage induced on a static HIGH high output during switching of other outputs.

V_{OL} Output LOW Voltage. The voltage at an output conditioned LOW with a specified output load and V_{CC} supply voltage.

V_{OLP} Maximum (peak) voltage induced on a static LOW output during switching of other outputs.

V_{OLV} Minimum (valley) voltage induced on a static LOW output during switching of other outputs.

AC Characteristics

f_t Maximum Transistor Operating Frequency—The frequency at which the gain of the transistor has dropped by three decibels.

f_{max} Toggle Frequency/Operating Frequency—The maximum rate at which clock pulses may be applied to a sequential circuit. Above this frequency the device may cease to function.

t_{PLH} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined LOW level to the defined HIGH level.

t_{PHL} Propagation Delay Time—The time between the specified reference points, normally 1.5V on the input and output voltage waveforms, with the output changing from the defined HIGH level to the defined LOW level.

t_w Pulse Width—The time between 1.5V amplitude points of the leading and trailing edges of a pulse.

t_h Hold Time—The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.

t_s Setup Time—The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{PHZ} Output Disable Time (of a TRI-STATE Output) from HIGH Level—The time between the 1.5V level on the input and a voltage 0.3V below the steady state output HIGH level with the TRI-STATE output changing from the defined HIGH level to a high impedance (OFF) state.

t_{PLZ} Output Disable Time (of a TRI-STATE Output) from LOW Level—The time between the 1.5V level on the input and a voltage 0.3V above the steady state output LOW level with the TRI-STATE output changing from the defined LOW level to a high impedance (OFF) state.

t_{PZH} Output Enable Time (of a TRI-STATE Output) to a HIGH Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a HIGH level.

t_{PZL} Output Enable Time (of a TRI-STATE Output) to a LOW Level—The time between the 1.5V levels of the input and output voltage waveforms with the TRI-STATE output changing from a high impedance (OFF) state to a LOW levels.

t_{rec} Recovery Time—The time between the 1.5V level on the trailing edge of an asynchronous input control pulse and the same level on a synchronous input (clock) pulse such that the device will respond to the synchronous input.

AC Loading and Waveforms

For Normal Operation *Figures 1* and *2* show waveforms for all propagation delay and pulse width measurements while *Figures 3* and *4* show waveforms for TRI-STATE enable and disable times. The waveforms shown in *Figure 5* describe setup, hold and recovery times. These diagrams define all input and output measure points used in testing devices in the Normal Operation Mode.

For SCAN Test Operation, *Figure 8* shows propagation delay waveforms; *Figures 9* and *10*, TRI-STATE enable and disable times waveforms; *Figure 11* Set up, hold, and recovery time waveforms and *Figure 12,* Pulse Width waveform.

Figure 6 shows the AC loading circuit used in characterizing and specifying propagation delays of all devices, unless otherwise specified in the data sheet of a specific device. The value of the capacitive load (C_L) is variable and is defined in the AC Electrical Characteristics.

The 500Ω resistor to ground in *Figure 6* is intended to slightly load the output and limit the quiescent HIGH-state voltage to about +3.5V. Also shown in *Figure 6* is a second 500Ω resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring a device with open-collector outputs and for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a TRI-STATE output. With the switch closed, the pair of 500Ω resistors and the +7.0V supply establishes a quiescent HIGH level of +3.5V, which correlates with the HIGH level discussed in the preceding paragraph.

Figures 7a and *7b* describe the input pulse requirements necessary when testing circuits.

Waveforms

Normal Operation

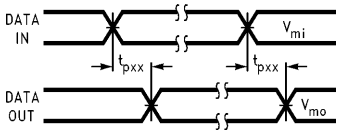

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FIGURE 1. Waveform for Inverting and Non-Inverting Functions

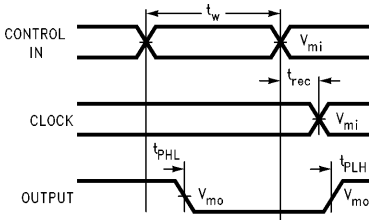

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FIGURE 2. Propagation Delay, Pulse Width and t_{rec} Waveforms

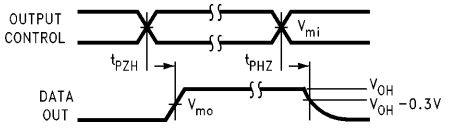

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FIGURE 3. TRI-STATE Output High Enable and Disable Times

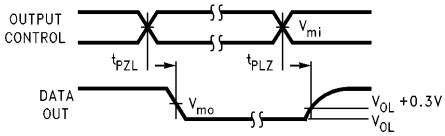

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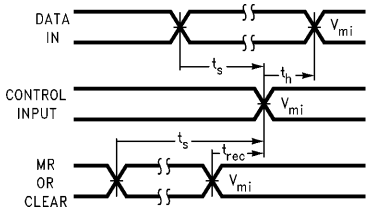
FIGURE 4. TRI-STATE Output Low Enable and Disable Times



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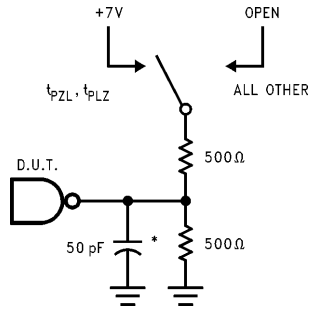
V_{mi} = 1.5V
V_{mo} = 1.5V

FIGURE 5. Setup Time, Hold Time and Recovery Time



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*Includes jig and probe capacitance

FIGURE 6. Standard AC Test Load

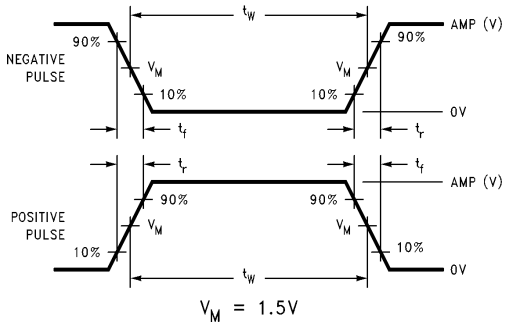

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FIGURE 7a. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 7b. Test Input Signal Requirements

Waveforms (Continued)

Scan Test Operation

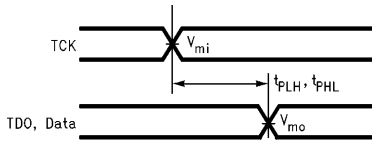

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FIGURE 8. Propagation Delay

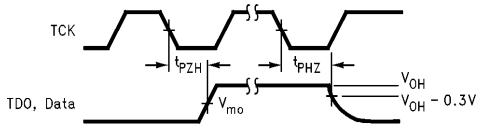

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FIGURE 9. TRI-STATE Output High Enable and Disable Times

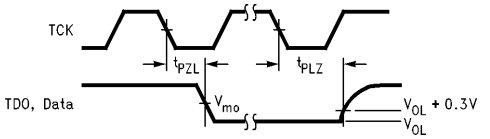

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FIGURE 10. TRI-STATE Output Low Enable and Disable Times

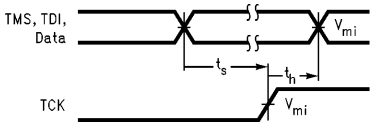

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FIGURE 11. Setup Time, Hold Time and Recovery Time

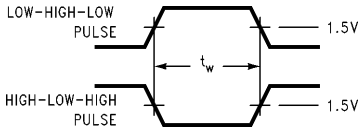

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FIGURE 12. Pulse Width

V_{mi} = 1.5V
V_{mo} = 1.5V

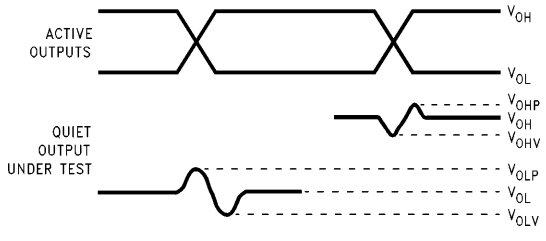

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FIGURE 13. Quiet Output Noise Voltage Waveforms

Note A: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note B: Input pulses have the following characteristics: f = 1 MHz, t_r = 3 ns, t_f = 3 ns, skew < 150 ps.

Skew Definitions and Examples

Minimizing output skew is a key design criteria in today's high-speed clocking schemes, and National has incorporated skew specifications into the SCAN CMOS family of devices.

This section provides general definitions and examples of skew.

CLOCK SKEW

Skew is the variation of propagation delay differences between output clock signal(s). See *Figure 15*.

Example:

If signal appears at out #1 in 3 ns and in 4 ns at output #5, the skew is 1 ns.

Without skew specifications, a designer must approximate timing uncertainties. Skew specifications have been created to help clock designers define output propagation delay differences within a given device, duty cycle and device-to-device delay differences.

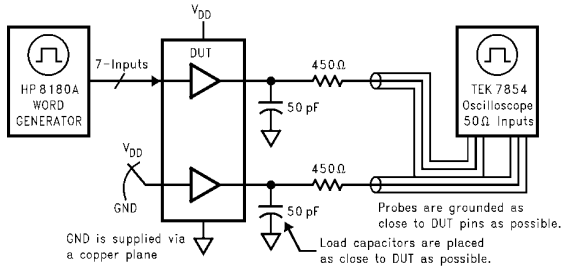

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FIGURE 14. Simultaneous Switching Test Circuit

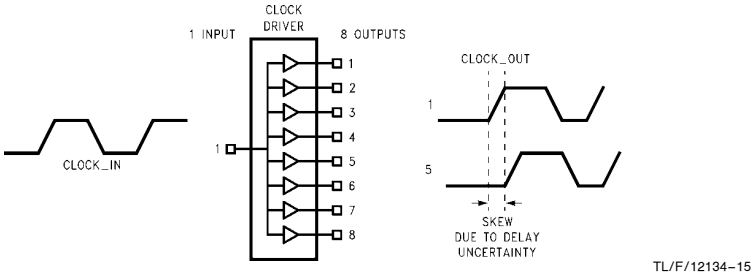

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FIGURE 15. Clock Output Skew

SOURCES OF CLOCK SKEW

Total system clock skew includes intrinsic and extrinsic skew. Intrinsic skew is defined as the differences in delays between the outputs of device(s). Extrinsic skew is defined as the differences in trace delays and loading conditions.

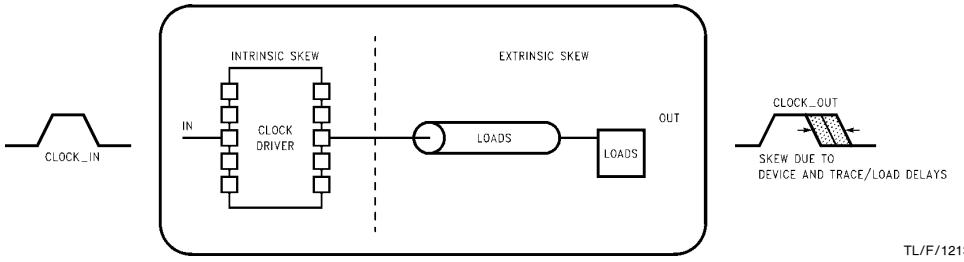

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FIGURE 16. Sources of Clock Skew

Example: 50 MHz Clock signal distribution on a PC Board.

50 MHz signals produces 20 ns clock cycles

Total system skew budget = 10% of clock cycle = 2 ns* → 2 ns

If extrinsic skew = 1 ns → − 1 ns

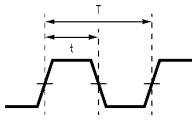
Device skew (intrinsic skew) must be less than 1 ns! ← 1 ns

*Clock Design *Rule of thumb.*

Skew Definitions and Examples (Continued)

CLOCK DUTY CYCLE

- Clock Duty Cycle is a measure of the amount of time a signal is *High* or *Low* in a given clock cycle.



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Duty Cycle = t/T * 100%

FIGURE 17. Duty Cycle Calculation

Clock Signal

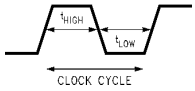

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FIGURE 18. Clock Cycle

Example:

t_{HIGH} and t_{LOW} are each 50% of the clock cycle therefore the clock signal has a Duty Cycle of 50/50%.

- Clock skew effects the Duty Cycle of a signal.

Clock + Skew

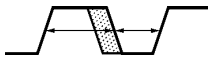

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FIGURE 19. Clock Skew

Example: 50 MHz clock distribution on a PC board.

Skew must be guaranteed less than 1 ns at 50 MHz to achieve 55/45% Duty Cycle requirements of core silicon!

TABLE I

System Frequency	Skew	t_{HIGH}	t_{LOW}	Duty Cycle		
50 MHz	0 ns	10 ns	10 ns	50/50%	←	Ideal Duty Cycle (50/50%) occurs for zero skew.
50 MHz	2 ns	12 ns	8 ns	60/40%		
50 MHz	1 ns	11 ns	9 ns	55/45%		
33 MHz	2 ns	17 ns	15 ns	55/45%	←	Note that at lower frequencies, the skew budget is not as tight and skew does not effect the Duty Cycle as severely as seen at higher frequencies.

Definition of Parameters

t_{OSLH}, t_{OSHL} (Common Edge Skew)

t_{OSHL} and t_{OSLH} are parameters which describe the delay from one driver to another on the same chip. This specification is the worst-case number of the delta between the fastest to the slowest path on the same chip. An example of where this parameter is critical is the case of the cache controller and the CPU, where both units use the same transition of the clock. In order for the CPU and the controller to be synchronized, $t_{OSLH/HL}$ needs to be minimized.

Definition

t_{OSHL}, t_{OSLH} (Output Skew for High-to-Low Transitions):

$t_{OSHL} = |t_{PHL_{MAX}} - t_{PHL_{MIN}}|$

Output Skew for Low-to-High Transitions:

$t_{OSLH} = |t_{PLH_{MAX}} - t_{PLH_{MIN}}|$

Propagation delays are measured across the outputs of any given device.

Example

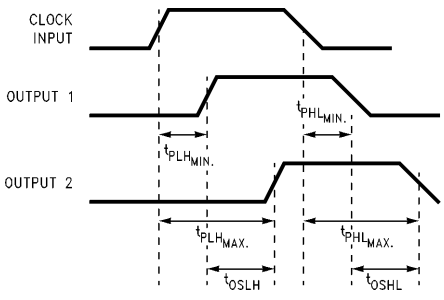

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FIGURE 20. t_{OSLH}, t_{OSHL}

Characterization and Test Specifications

Philosophy

During the product introduction process for National logic IC's, a new IC design will undergo a rigorous characterization to baseline its performance. This data is required to correlate with simulation models, determine product specifications, compare performance to other product, provide a feedback mechanism to the fabrication process, and for customer information. National's Logic IC characterizations are designed to get as much information as possible about the product and potential customer application performance.

National's logic IC characterization methodology uses past knowledge of design performance, simulation, and process parametrics to determine what electrical parameters to characterize. Characterization samples are selected so that they have key process parametrics (e.g., Drive, Beta, V_{tn}, V_{tp} L_{eff}, etc.) which have been shown to significantly affect device electrical parameters. Data is acquired and processed using statistical analysis software. Manufacturing test limits are then set using the knowledge of variations due to fabrication, package, tester, V_{CC}, temperature, and condition. This allows product to be shipped on demand without problems or delays.

The following are brief summaries of characterization tests performed.

AC Electrical Characteristics

Single Output Switching propagation delays
Testing includes measured propagation delays at 50 pF and 250 pF output load capacitances.

t_{PLH} t_{PHL}	Active Propagation Delays
t_{PZH} t_{PZL}	Enable Propagation Delays
t_{PLZ} t_{PHZ}	Disable Propagation Delays

Also included are input timing parameters

t_S	Setup Time
t_H	Hold Time

Multiple (Simultaneous) Output Switching Propagation Delays

These tests are used to ensure compliance to the extended databook specifications and include active propagation delays, disable and enable times at 50 pF and 250 pF output loads.

Multiple Output Switching Skew

Performance data from the Multiple Output Switching propagation delay testing is analyzed to obtain information regarding output skew of an IC.

FMAX (synchronous logic)

FMAX determines the minimum frequency at which the device is guaranteed to operate for a clocked IC. This test is package and test environment sensitive.

Pulse Width (synchronous logic)

Pulse Width testing is used to define the minimum pulse duration that a flip-flop or latch input will accept and still function properly. This test is package and test environment sensitive.

F-Toggle (asynchronous logic)

F-Toggle is the minimum frequency at which the IC is guaranteed to function under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

AC Dynamic (Noise) Characteristics

V_{OLP}, V_{OLV}—Ground Bounce (Quiet Output Switching)

Measured parameters with 50 pF loading relate the amount that a static conditioned output will change in voltage under multiple outputs switching condition with outputs operating in phase. They are heavily influenced by the magnitude that V_{CC} and Ground move internal to the IC.

V_{ILD}, V_{IHD}—Dynamic Threshold

Dynamic threshold measures the shift of an IC's input threshold due to noise generated while under multiple outputs switching condition with outputs operating in phase. This test is package and test environment sensitive.

Input Edge Rate

This test is performed to determine what minimum edge rate can be applied to an input and have the corresponding output transition with no abnormalities such as glitches or oscillations.

DC Electrical Characteristics

Automated Test Equipment (ATE) DC Tests

DC test data gathered show the performance of an IC to statically applied voltages and currents.

Functional Shmoo

The function shmoo shows the function operational window of an IC at a wide range of V_{CC}'s and temperatures.

Power Up & Power Down Output Shmoo

Similar to the function shmoo, the power up and power down output shmoo shows the DC operation of an output during power up and power down conditions.

Transfer Characteristic (V_{IN}/V_{OUT})

Input Traces (V_{IN}/I_{IN})
Output Traces (V_{OL}/I_{OL}, V_{OH}/I_{OH})

Power

Power-Up I_{CC} Traces

Shows how the supply current reacts to various input conditions during power up.

I_{CC} vs V_{IN} Traces

Traces of I_{CC} vs V_{IN} show how the supply current changes with input voltage.

Power (Continued)

I_{CCD} (Dynamic I_{CC})

Determines the amount of current an IC will consume at frequency.

Capacitance

Input/Output Capacitance (C_{IN}/C_{OUT})

Reliability Tests

Latch-up

Testing determines if an IC is susceptible to latch-up from over-current or over-voltage stresses per MIL-STD-883 JEDEC method 17.

HBM Electrostatic Discharge, Human Body Model

Per MIL-STD-883C method 3015.6.

Quality and Reliability

Introduction

Product qualification is a disciplined, team activity which focuses on demonstrating, through the acquisition and analysis of engineering data, that a device design, fab process, or package design meets or exceeds minimum standards of performance. In most cases, this involves running samples of product through a series of tests which expose the samples to operating stresses far in excess of those which would be encountered in even the most severe ''real life'' operating environment. These tests are called either accelerated stress tests or accelerated life tests. A properly designed qualification test sequence exposes, within a matter of days or weeks, those design, materials, or workmanship defects which would lead to device failure in the customer's application after months or even years of operation.

In order to be considered a ''world class'' supplier of semiconductor devices, NSC designs and manufactures products which are capable of meeting the reliability expectations of its most demanding customers. While customer requirements and expectations vary on the subject of reliability requirements for devices, virtually all large users have general procurement specifications which establish failure rate goals or objectives for the suppliers of the components used in their products.

Failure rate goals for infant mortality and long-term-failure-rate-in-service have been established for all NSC product lines. These goals are published internally at the beginning of each fiscal half-year (usually June and December). The actual performance of the product against these goals is measured monthly using life test data gathered from various sources including the Fast Reaction and Long Term Audit Program. Performance is reviewed every six (6) months by Reliability and Product Group management and adjusted as necessary to reflect customer expectations, competitive data, and/or historical performance trends.

Given that product reliability is an overriding corporate objective, and that any deficiency in design, materials, procedures, or workmanship, has a potential for adversely affecting the reliability of the product, Manufacturing and Engineering organizations within NSC, its subsidiaries, and its sub-contractors, involved in introducing a new device, process, or package, share a joint responsibility for demonstrating that the product does conform to NSC standards and to the standards and expectations of NSC's customers.

As a matter of policy, it is NSC's goal to design and manufacture product that is 100% defect-free and capable of surviving the qualification tests with zero failures. This policy is not interpreted as a directive to abandon a qualification program when failures occur or to delay new product releases until perfection has been achieved. Rather, the policy is intended to focus engineering resources on the identification and elimination of the design, process, or workmanship deficiencies that are the root causes of the failures and then to engineer a solution to correct those deficiencies.

Results from the initial qualification for the SCAN ABT Advanced Logic families are published in Self Qualification handbooks. Additional stress testing is performed regularly as a reliability monitor as part of the Fast Reaction Program and Long Term Audit Program. The Self Qualification handbook contains the data typically requested by customers as part of joint qualification programs in addition to detailed explanations of all tests performed. The Logic self qualification handbook may be obtained by contacting the Customer Response Center at 1-800-272-9959.

TABLE II. Qualification Requirements for Logic Integrated Circuits

Test	Test Method	Test/Stress Conditions	Sample Size Each Lot
Operating Life	SOP-5-049-RA Method 107	1000 Hours @T_A = 125°C	77
High Temperature Storage	SOP-5-049-RA Method 103	1000 Hours @150°C	45
Temperature Cycle	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature Cycle with Preconditioning	SOP-5-049-RA Method 105	1000 Cycles −65°C to +150°C	77
Temperature-Humidity-Bias	SOP-5-049-RA Method 104	1000 Hours 85°C @ 85%RH	77
Temperature-Humidity-Bias with Preconditioning	Method 112 Method 104	Precondition plus 100 hours 85°C to 85%RH	77
Autoclave	Method 101	500 hours 121°C @ 15 psig	45
Thermal Shock	Method 106	100 Cycles −65°C to +150°C	22
Salt Atmosphere	Method 209	25 Hours 35°C	22
Resistance to Solvents	Method 207	4 Solvents	3 Each Solvent
Lead Integrity	Method 205	Condition as Appropriate to Package	22 Leads
Solderability	Method 203	8 Hour Steam 5 secs @260°C	22
Solder Heat	Method 204	12 secs 260°C	22

Quality Information and Communication (QUIC) System

BACKGROUND

National's Quality Assurance Systems Development group (QASD) maintains a variety of data tracking systems such as: Electronic Reliability Data Management (ERDM), Failure Analysis (F/A), Burn-in Board Inventory, and a number of others.

QUIC users will find a user friendly, menu-driven, real-time system that gives them a simultaneous-user environment with timely data inputs from sites around the world. QUIC is programmed to recognize each individual user of the system at the point of logging on to the mainframe, and provides an appropriate list of menu options consistent with the user's level of access requirements.

National grants access to QUIC by customers that provides a sufficient level of security over the entire system, thus precluding the possibility of accidental access (or even damage) to various files.

HOW A CUSTOMER LINKS TO QUIC

1. Check to make sure you have the hardware components listed below. (An attached printer is desirable but not imperative.)

   IBM/PC compatible computer with at least 128k memory.

   Hayes compatible 1200 baud modem (or 2400, 4800 or 9600).

   Touch tone phone.
2. Request access to QUIC by contacting your National sales representative or Customer Service Center at 1-800-272-9959, who will coordinate all activities necessary to provide access for your company and arrange training (usually handled over the telephone).
3. Identify the person who will be your company's main contact and user of the QUIC system. This person will assume responsibility for the USERID assigned to your company and will receive training on how to access and use the QUIC system.
4. National will provide a USERID, password and account number with appropriate menus and a communications software package called EXECULINK, which allows the customer's PC to talk with NSC's host computer and also turns the PC into a virtual host terminal, with full-screen editing capability and full use of program function (PF) keys. EXECULINK also provides for file transferring between host and PC and spooling of print files to a PC-attached printer.

ONGOING IMPROVEMENTS

As we receive feedback from the users of QUIC, we (QASD) will continue to enhance the ''User Friendliness'' of the system and add new features which, we hope, will help promote a true sense of teamwork between us and our customers.

Wafer Level Reliability (WLR)

BACKGROUND

The conventional methods of reliability screening, that of short-term burn-in to eliminate infant mortalities and long-term life tests at high temperature, will soon become impractical for many devices. The reasons for this are tighter infant mortality ppm requirements, higher costs, and shortened lifetimes.

As device complexity increases, the testing sample size required to ensure infant mortality ppm levels in the 0–10 ppm range will quickly deplete reliability test capacity. While burn-in eliminates inferior devices, it can also substantially shorten the lifetimes of ''good'' devices to an unacceptable level, creating an expensive and somewhat risky procedure. New technology advances which minimize geometry, have moved our device lifetime distributions closer to our customer's expected system life. As device geometries shrink, resulting in higher current densities, electric fields, and chip temperatures, tighter fab process control and instant feedback become critical.

THE GOAL OF WAFER-LEVEL-RELIABILITY TESTING-PROCESS RELIABILITY

Wafer-level-reliability testing represents a proactive, correlation and control approach to ensuring device reliability. WLR is not meant to replace classical reliability testing. Instead it is used to supplement existing methods.

WLR testing is used to:

1. Identify shifts in On-Line Process Controls (fab monitors) which affect product reliability.
2. Reduce process qualification cycle time.
3. Improve process qualification success rate.
4. Assess reliability trends of production processes.
5. Quantify the reliability impact of process modifications.

WLR provides faster feedback for fab process control. The collection of WLR test data during and at the end of wafer fab processing provide a reliability baseline for each of our fab processes. Shifts in WLR test results, whether intentional (a process change or qualification) or unintentional (a process control problem), signal an increase or decrease in product reliability risk. WLR monitoring of production processes using Statistical Quality Control (SQC) techniques provides engineering with the information required to find and fix process control problems faster, and to determine the effectiveness of on-line process controls from a reliability standpoint. In this way, WLR testing is used to link on-line process controls to the traditional accelerated life testing methods.

NATIONAL'S WLR PROGRAM

National developed a corporate-wide WLR program which continues to implement powerful, new test techniques. WLR testing has been used effectively to help understand how process variability affects product reliability. It is also used to help build-in reliability at the design stage for new process technologies.

WLR tests and test structures have been designed to increase the likelihood and predict a rate of a reliability failure mechanism occurrence. In addition, National has developed a partnership with a leading parametric test system supplier. Working together, a WLR test system was designed and developed to meet the unique requirements of Wafer-Level-Reliability testing. These systems are capable of testing to the voltage, current, and temperature extremes required for inducing the desired failure mechanisms in a short period of time. Some examples of the reliability failure mechanisms that are monitored using WLR techniques include:

Interlayer Dielectric Integrity

Unique high voltage testing (to 1500V) is used to test for dielectric particles, metal hillocks or contamination, and poor dielectric stop coverage. Designed experiments

Wafer Level Reliability (WLR) (Continued)

have been successful in correlating the high voltage WLR test results to fab process monitors (such as deposition temperature and etch selectivity), and to accelerated life test results (Op-life, Temp Cycle, and Thermal Shock).

Metal Step Coverage

High current testing of large area metal serpentine structures is performed to detect restrictions in the conducting stripe. Designed experiments have been successful in correlating the high current WLR test results to fab process monitors such as metal thickness, critical dimensions, and via size.

Mobile Ions

A 200°C hot chuck is used with custom-built high temperature probe cards to accurately measure transistor threshold voltage shifts for a variety of oxide layers. Other methods for detecting mobile ion contamination include the use of self-heated polysilicon gate test structures and Triangular Voltage Sweep (TVS) test techniques.

Metal Stress Voids

High current resistance measurements are taken before and after wafers are processed through a series of heating and cooling cycles. This heat treatment is designed to mimic the high temperature processing incurred during device assembly (such as a seal-dip furnace), and it has been shown to accelerate metal void formation when the stress of the overlying film is high enough. Significant increases in the final resistance indicate the formation of metal stress voids.

Gate Oxide Integrity:

JEDEC J_{RAMP}, V_{RAMP} and Q_{BD} test techniques are used to monitor gate oxide quality. The WLR tester is also used to perform very sensitive leakage current measurements, using a specially designed picoammeter module, which allows us to detect subtle differences in gate oxide quality.

Passivation Integrity

A novel wafer-level-autoclave test technique has been developed which allows us to quantify the level of protection the passivation film provides when the wafer is subjected to a high temperature, high humidity environment.

Hot Electron Degradation

Two wafer level tests are performed to indicate device susceptibility to hot electron damage. First, the maximum substrate current is measured to indicate the level of impact ionization occurring at the drain edge. Second, gate current measurements are taken to gauge the magnitude of electron injection during device operation. Long-term DC stressing of transistors at peak substrate current conditions is also monitored.

Electromigration

A Standard Wafer Electromigration Accelerated Test (SWEAT) technique is used to measure the sensitivity of a metal line to electromigration failures. SWEAT is used as a relative test of the reliability of a line.

Contact Electromigration

Risk of failures due to contact spiking and solid phase epitaxial growth (SPEG) are monitored by forcing current through specially designed test structures, and monitoring increases in resistance and substrate leakage.

Electrostatic Discharge Sensitivity (ESD)

BiCMOS LOGIC

National BiCMOS Logic has designed special dual-rail ESD protection circuitry to increase its level of ESD performance over non-protected inputs and outputs. This protection is standard on all BiCMOS Logic designs and was first used in National's family.

By design, this circuitry limits product vulnerability to both positive and negative Human Body Model (HBM) ESD and Electrical Overstress (EOS) voltages by protecting inputs and outputs connected to V_{CC} as well as ground. Protection to ground is provided through the transistor Q2 and diode D2, standard Schottky clamp. The path to V_{CC} is protected through the BVCEO breakdown mechanism of Q1. Diode D1 ensures isolation of the input or output from V_{CC} leakages.

The device design and layout ensures dependable turn-on characteristics as well as robustness.

ESD protection was achieved with no appreciable affect on speed or increase in capacitance.

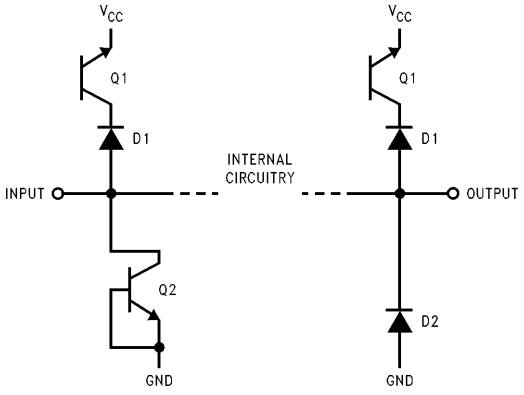

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Figure 21. ESD Protection Circuit

Electrostatic Discharge Sensitivity (ESD) (Continued)

ABT and SCAN ABT logic ESD sensitivity is guaranteed greater than 2000V, using the MIL-STD-883C, test method 3015 for Human Body Model (HBM) ESD.

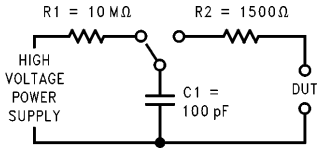

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Figure 22. HBM Test Circuit

Normal handling precautions should be observed as in the case of any semiconductor.

CMOS Logic

Circuits which show excellent resistance to ESD-type damage are classified as category "B" of MIL-STD-883C, test method 3015, and withstand in excess of 4000V typically. It is guaranteed to have 2000V ESD immunity on all inputs and outputs. Parts do not require any special handling procedures, however, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 23 shows the ESD test circuit used in the sensitivity analysis for this specification. *Figure 24* is the pulse waveform required to perform the sensitivity test.

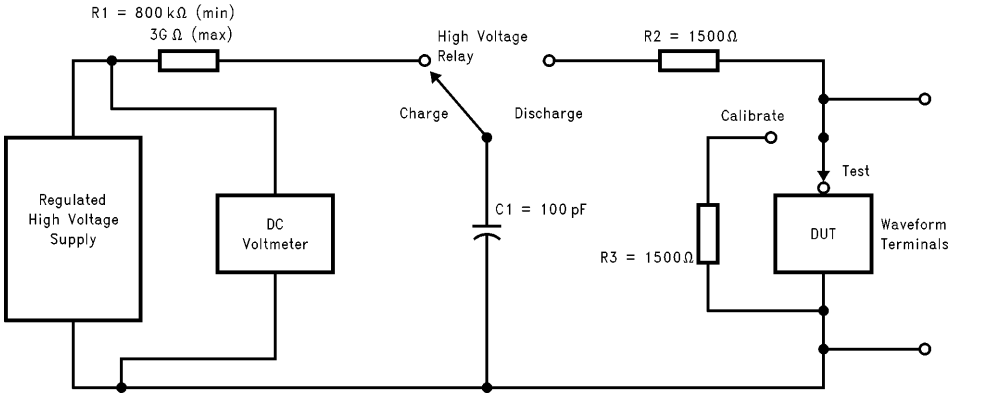

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FIGURE 23. ESD Test Circuit

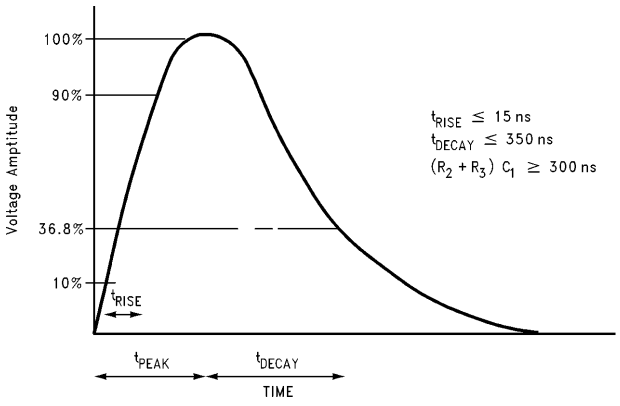

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FIGURE 24. ESD Pulse Waveform

Power Sensitivities for Minimum Geometry Products

The demand for high performance process technology capable of sub 4 ns speeds, minimal noise and lower operating voltages drives the microelectronics industry towards decreasing layout geometries. Advanced process technology minimizes gate widths, gate oxide thickness and junction depths to improve gate switching speeds. In contrast, the decreased geometries reduce the ability of the devices built on advanced processes to resist electrical overstresses. As geometries decrease, emphasis shifts towards the reduction of environmentally induced electrical overstresses to ensure system and component reliability.

Market trends continue to drive the need for smaller geometries with reduced power supply voltages. Current 5.0V technologies are migrating towards 3.0V technologies while 3.0V technologies have shown a greater sensitivity to electrical overstresses. Sensitivities to electrical overstresses have been observed in as large as 1.0 μm geometries.

Device damage from electrical overstresses vary and the categories include, but are not limited to: Electrical-Over-Stress (EOS) due to excessive current or voltage exposure and Electro-Static-Discharge (ESD) be it exposure by Human Body Model, Charged Device Model or Machine Model. Sources of electrically induced overstresses are difficult to determine; however, investigation of failures from small geometry devices may show that environmental hazards such as unregulated and unconditioned power supplies in the field exceed ''Absolute Maximum Ratings'' causing unrecoverable device damage.

Advanced processes such as BiCMOS include small dimension current density limited geometries that are sensitive to electrically induced overstresses. The combination of internal bipolar and CMOS gates provides current capabilities for maximum device performance. In an unconditioned supply environment, the bipolar section of a BiCMOS circuit can source excessive current through the CMOS section and cause damage due to the CMOS circuit's current density limited geometries.

In an effort to resolve device sensitivities to electrical overstresses, designers and engineers can reference device databooks. Databook specifications include ''Absolute Maximum Ratings'' and adherence to this specification is essential in ensuring component and system level reliability.

1. A. Amerasekera, A. Chatterjee, *''An Investigation of BiCMOS ESD Protection Circuit Elements and Applications in Submicron Technologies''*, EOS/ESD Symposium, p5B.6.1.

Latchup Testing

Latchup in CMOS and bipolar circuits can vary in severity from being a temporary condition of excessive I_{CC} current and functional failure, to total destruction requiring a new unit. The latchup condition is usually caused by applying a stimulus that is able to cause a regenerative condition in a PNP-NPN structure. For a more detailed description of definitions and causes of latchup, see National Semiconductor Application Note 600 (located in the ''FACT Advanced CMOS Logic Data book'' Lit. # 40019).

BiCMOS Logic

National has characterized its Advanced BiCMOS logic for robustness using the JEDEC 17 method and an IMCS 4600 Automated Latchup Test System. The automated test equipment approach to latchup provides a repeatable test setup and application of test conditions, reduces the amount of time for evaluation, and provides a more comprehensive set of vectors and stimuli over a shorter period of time.

The JEDEC 17 method is a standard measurement procedure for the characterization of CMOS integrated circuit latchup susceptability/immunity, measured under static conditions. The method allows for overcurrent/overvoltage stressing of inputs and outputs to detect latchup.

In short, the JEDEC 17 method follows a sequence of:

1. Apply power
2. Setup I/O conditions to place device in desired state
3. Apply trigger source for desired duration
4. Measure supply current
5. Remove power supply if $I_{CC} \geq$ test limit
6. Inspect for electrical damage

The time for each parameter as well as the temperature is critical for correlation of latchup. National characterizes latchup on the Advanced BiCMOS family at 125°C and with the critical timing parameters on Table III. Close correlation can only be accomplished by using the same trigger duration, V_{CC}, test temperature, and magnitude of trigger stimulus.

TABLE III. Critical Timing Parameters

Symbol	Parameter	Time
T_W	Trigger Duration	500 μs
t_{COOL}	Cool Down Time	10 ms

Latchup Testing (Continued)

For BiCMOS ABT products, logic states are checked for a susceptability to latchup with all outputs high, all outputs low and all outputs in TRI-STATE. If the device is a bidirectional device, then the logic states are tested in each direction. All inputs and outputs are tested for each logic state and direction.

Because the ABT and SCAN ABT family is designed for live insertion, a Positive Voltage Trigger (PVT) and a Negative Current Trigger (NIT) is applied to the inputs and outputs to check for latchup.

Forcing a current in the positive direction overstresses the inputs and outputs by causing a breakdown. Such breakdowns consume enough power in the breakdown area to cause the junction permanent damage. PVT stresses the inputs and output while keeping the input and output devices out of any breakdown region.

Finally all inputs and outputs have clamp diodes, requiring a negative current trigger as a stimulus for latchup. The clamp diodes are designed to allow current flow into ground without injecting carriers into the substrate that could cause a parasitic PNP-NPN. Supply and stimulus values used by National for latchup testing the ABT family are in Table IV.

TABLE IV. Supply and Stimulus Values

Stimulus	Parameter	V_{CC}	Stimulus
PVT	Positive Voltage Trigger	7.0V	V_{CC} + 3V (10V)
NIT	Negative Current Trigger	7.0V	−500 mA

Verification of any unusual observations is performed with a curve tracer manually. For example, when ABT outputs are brought below ground, the NMOS transistor feeding current to the bipolar output will turn on and current from V_{CC} will come out of the output pull-down device. This condition is unavoidable by design and is not latchup. Thus good analysis of observations will tell one whether latchup has occurred.

Due to the high trigger stresses, devices used for latchup testing should be discarded and not used for design, production, or other tests. Latchup testing is potentially destructive and may limit the life of a device.

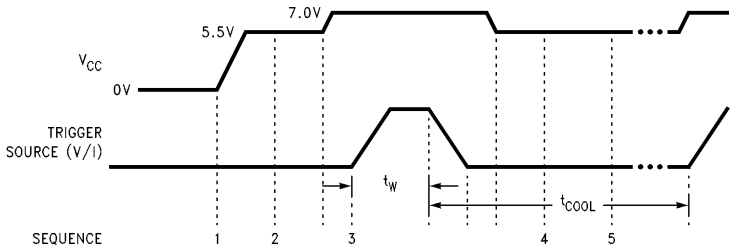

FIGURE 25.

Latchup Testing (Continued)

CMOS Logic

In the past a major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. SCAN CMOS logic is guaranteed not to latch-up with dynamic currents of 300 mA forced into or out of the inputs or the outputs under worst case conditions (T_A = 125°C and V_{DD} = 5.5 V_{DC}). At room temperature the parts can typically withstand dynamic currents of close to 1A. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

SCAN CMOS devices have been specifically designed to reduce the possibility of latch-up occurring; National Semiconductor accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

The test procedure is as follows; five pulses, each of at least 2000V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. Devices that result in ESD immunity in the 2000V–3999V range are listed as ESD Class 2. Devices that result in ESD immunity in the 4000+V range are listed as ESD Class 3.

For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

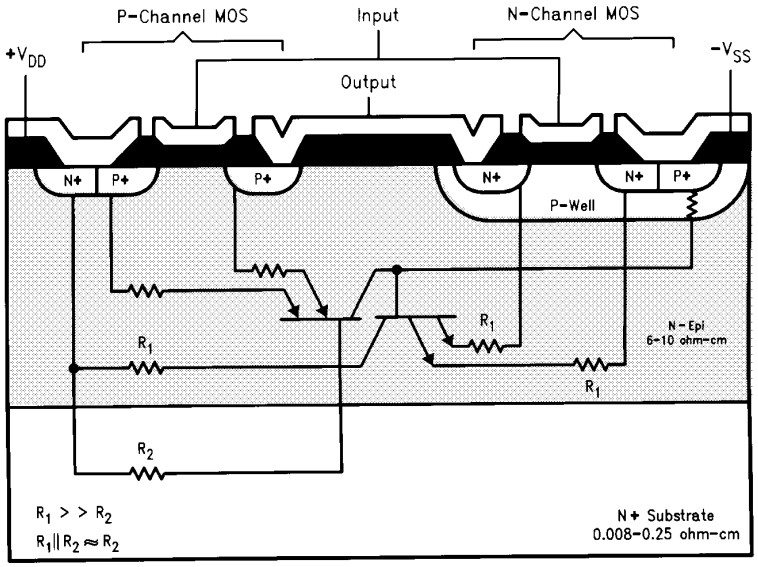

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FIGURE 26. Advanced CMOS EPI Process Cross Section with Latch-up Circuit Model