An Overview of LVDS Technology

National Semiconductor
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INTRODUCTION

Recent growth in high-end processors, multi-media, virtual reality and networking has demanded more bandwidth than ever before. But the point-to-point physical layer interfaces have not been able to deal with moving information at the data rates required. Some of today's biggest challenges that remain to be solved include: the ability to transfer data fast, lower power systems than currently available, and economical solutions to overcome the physical layer bottleneck. Data Transmission standards like RS-422, RS-485, SCSI and others all have their own limitations most notably in transferring raw data across a media. Not anymore. Low Voltage Differential Signaling (LVDS) is a high speed (>155.5 Mbps), low power general purpose interface standard that solves the bottleneck problems while servicing a wide range of application areas.

This application note explains the key advantages and benefits of LVDS technology. Throughout this application note the DS90C031 (LVDS Quad CMOS Differential Line Driver) and the DS90C032 (LVDS Quad CMOS Differential Line Receiver) will be used to illustrate the key points.

STANDARDS OVERVIEW

There are two key industry standards that define LVDS. One is a IEEE (Institute for Electrical and Electronics Engineering) standard and the other is a TIA (Telecommunication Industry Association) recommended standard.

IEEE 1596.3 SCI-LVDS

SCI originally referenced a differential ECL interface within the SCI (Scalable Coherent Interface) 1596-1992 IEEE standard. But, this only addressed the high data rates required and did not address the low power concerns. Thus, SCI-LVDS was defined as a subset of SCI, and is specified in IEEE 1596.3 standard. SCI-LVDS specifies signaling levels (electrical specifications) for the high speed/low power physical layer interface. It also defines the encoding for packet switching used in SCI data transfers. Packets are constructed from 2-byte (doublet) symbols. This is the fundamental 16-bit symbol size. No media is specified and the data rate can be in the order of 500 MT/s based on serial or parallel transmission of 1, 4, 8, 16, 32, 64,.... bits.

SCI-LVDS also supports RamLink for super low power data transmission in a restricted environment. The IEEE 1596.3 standard was approved in March 1994. National Semiconductor held the Chairperson position for this standard.

TIA PN-3357

This is a proposed standard under the Data Transmission Interface committee TR30.2. The Electrical characteristics of the TIA standard are similar to SCI-LVDS. This standard defines driver output and receiver input characteristics. Functional specifications and/or Protocols are not within the scope of the TIA standard. It specifies a recommended maximum data rate of 655 Mbps and a theoretical maximum of 1.923 Gbps based on a loss-less media. Minimum media specifications are also defined within the standard. It also discusses failsafe operation of the receiver under fault conditions and other configurations issues such as multi-receiver operation. National Semiconductor also holds the editor position for this standard.

Both the IEEE and the TIA standards allow for external termination or internal termination with the resistor(s) integrated within the Receiver package.

LOW VOLTAGE DIFFERENTIAL SIGNALING

LVDS technology uses differential data transmission. The differential scheme has a tremendous advantage over single-ended schemes as it is less susceptible to common mode noise. Noise coupled onto the interconnect is seen as common mode modulations by the receivers and is rejected. The receivers respond only to differential voltages.

LVDS technology is not dependent on a specific power supply, such as +5V. This means there is an easy migration path to lower supply voltages such as +3.3V or even +2.7V while still maintaining the same signaling levels and performance. Technologies like ECL or PECL are more dependent on the supply voltage. This feature is highly desirable in any application that foresees moving to lower supply voltages without substantial redesign or worrying about mixed voltage operation (+5V/+3.3V) on system boards.

To achieve high data rate, low power, and to reduce EMI effects, signaling levels have to be reduced. The DS90C031/C032 chipset's limitation on data rate is mainly dependent on the technology driving the LVDS drivers. The aggregate bandwidth that LVDS technology can drive is in the Gbps range with a loss-less media. Data rates in the 500–600 Mbps are possible and this limitation is primarily dependent on the media being driven.

SIGNALING LEVELS

As the name implies, LVDS features a low voltage swing compared to other industry data transmission standards. The signaling levels are illustrated in *Figure 1,* and a comparison to PECL levels is also shown as reference. Because of the low swing advantage, LVDS achieves a high aggregate bandwidth in point-to-point applications.

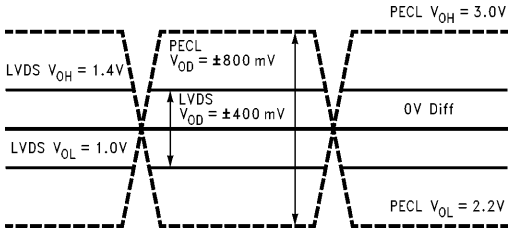

FIGURE 1. PECL vs LVDS Signal Swing

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It is impossible to achieve high data rates and provide low power without utilizing low voltage swings. LVDS signaling levels are smaller (50%) than PECL levels as shown in *Figure 1.* EMI effects are also reduced as the signaling swings are much smaller than traditional CMOS, TTL or even PECL.

LVDS TERMINATION

LVDS uses a constant current mode driver to obtain its many features. The value of the current source for the DS90C031 is a maximum of 4.5 mA. The transmission media must be terminated to its characteristic impedance to prevent reflections. Typically this is between 100Ω–120Ω and is matched to the actual cable. *A termination resistor is required* to generate the Differential Output Voltage (V_{OD}) across the resistive termination load at the receiver input (see *Figure 2a*). Data transmission from the driver to receiver without the termination is not recommended. The simplicity of the LVDS termination scheme makes it easy to implement in most applications. The user may also use a cable damping resistor as shown in *Figure 2b* with a capacitor to ground. It is recommended to have a single 100Ω termination between the driver outputs, and the use of surface mount components is also recommended to reduce the effects of parasitics. Proper termination not only avoids reflection problems but also reduces unwanted electromagnetic emissions. ECL and PECL require more complex terminations than the ''one'' resistor solution for LVDS. PECL drivers require 220Ω pull down resistors from each driver output to ground along with the 100Ω across the driver outputs as shown in *Figure 2c.*

COMMON MODE RANGE

An LVDS receiver can tolerate a minimum of ±1V ground shift between the driver's ground and the receiver's ground. Note that LVDS has a typical driver offset voltage of +1.2V, and the summation of ground shifting, driver offset voltage and any longitudinally coupled noise is the common mode voltage seen on the receiver input pins with respect to the receiver ground. The common mode range of the receiver is +0.2V to +2.2V, and the recommended receiver input voltage range is from ground to +2.4V. For example, if a driver has a V_{OH} of 1.4V and a V_{OL} of 1.0V, and a +1V ground shift is present (driver ground+1V higher than receiver), this will become +2.4V (1.4+1.0) as V_{IH} and +2.0V (1.0+1.0) as V_{IL} on the receiver inputs (+2.2V V_{CM}). Similarly, with a −1V ground shift and the same driver levels results as 0.4V (1.4−1.0) V_{IH} and 0.0V (1.0−1.0) V_{IL} on the receiver inputs (+0.2V V_{CM}). This is shown graphically in *Figure 3.*

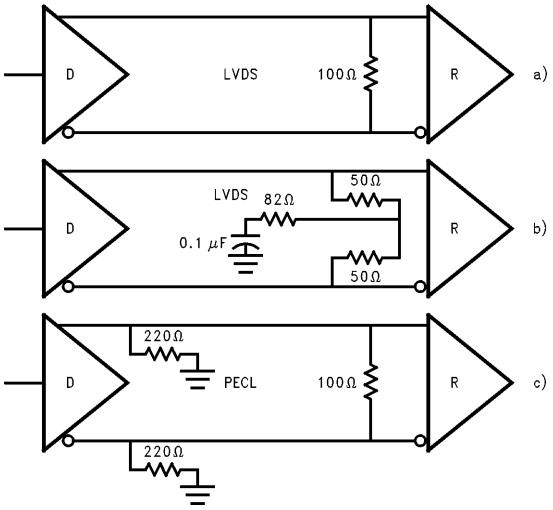

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FIGURE 2a, b, c. Termination Schemes

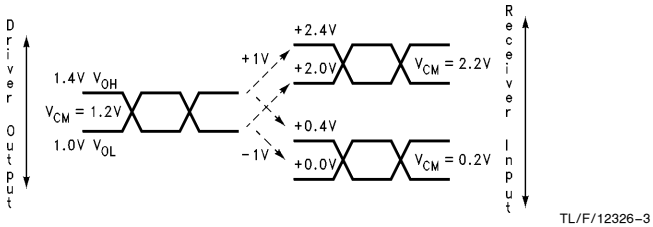

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FIGURE 3. Common Mode Voltage Range

FAILSAFE FEATURE

Failsafe is a receiver feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. This occurs when the inputs of the receiver are either open, shorted or terminated.

In some applications, not all receivers of the Quad DS90C032 may be used. In this case, the unused receiver inputs should be left *open.* If the receiver does not support failsafe and the inputs are left *open* (See *Figure 4a*), any external noise above the receiver threshold can trigger the output and cause can error on the communication line. Since the DS90C032 supports open input failsafe, the receiver output will provide an output High for this case.

Another fault condition can occur if the cable gets accidentally *shorted* (See *Figure 4b*). Due to environmental hazard conditions or poorly planned construction work, it is not uncommon to short a communication line by cutting through the cable. Under the above condition, the receiver output will also be at logic High and not in an unknown state.

Another case could occur if the driver is either powered off, in TRI-STATE® or even removed from the line while the receiver stays powered on with inputs *terminated* by the 100Ω termination resistor.

The receiver output will provide a logic high under all the above mentioned conditions.

Because all three (open, short and terminated) failsafe conditions are supported on the receiver, external biasing resistors are not required. This saves valuable board space, cost and design headaches compared to receivers that do not support failsafe. A receiver without failsafe can go into oscillation under certain fault conditions described above.

POWER ON/OFF REQUIREMENTS

On a point-to-point application, it is important to understand the behavior of the DS90C031 driver and the DS90C032 receiver under different conditions, such as power on/off. As shown in *Figure 5,* the driver is ON and the receiver is OFF, current flows from the driver output to the receiver input. This is not recommended as the ESD protection diode on the receiver input stage turns on and clamps the line to a diode drop above GND. This is the case where power supplies present a low impedance path to GND when powered off. But even when this occurs the driver limits the current flowing through the diode to less than 5 mA (short circuit current), preventing any thermal problems.

On the other hand, if the driver is OFF and the receiver is ON as shown in *Figure 6,* there is no leakage path from driver output to receiver input or from the receiver input to the driver output (and the line is not clamped). Under this condition, the failsafe feature of the receiver will guarantee a logic High output.

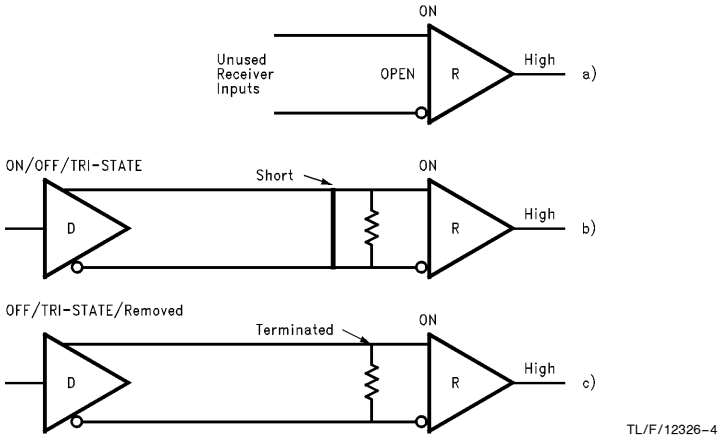

FIGURE 4a, b, c. Failsafe Operation

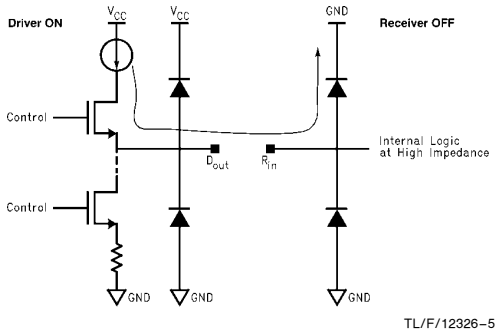

FIGURE 5. Driver ON and Receiver OFF

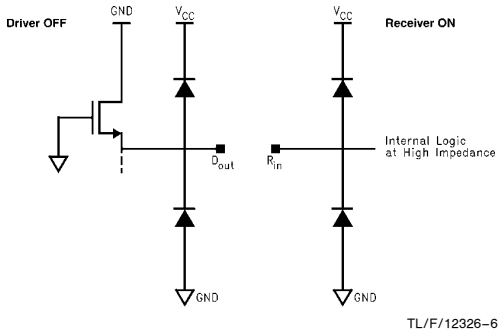

FIGURE 6. Driver OFF and Receiver ON

POINT-TO-POINT CONFIGURATIONS

For interfaces where the transition time of the driver is substantially shorter than the time delay of the media, the interconnection must be considered a distributed load, not a lumped load. The distributed elements of a transmission line (media) can greatly affect signal quality.

More explicitly, transmission line theory dictates that if the transition (rise or fall) time of the driver is less than four times the line delay, the media must be treated as a distributed load, not a lumped load, and careful attention must be paid to any impedance discontinuities and stubs. For a given driver, if $t_r < 4\ t_d$ (where t_r = driver rise time, t_d = delay of the line) or $t_d > ¼\ t_r$ the line should be considered as a lossy line. This is usually true if the t_r of drivers are in the sub nanosecond range. A quick calculation will clarify this rule of thumb. For example: the DS90C031 driver has a typical t_r of 350 ps, and a microstrip built with FR-4 material has a t_d of 147 ps for one inch of PC trace. This calculates that, an inch of FR-4 microstrip will act as a transmission line ($350 < 4*147$) when driven by the DS90C031 driver. *Figure 7* includes a stub between the termination resistor and the receiver input, this length must not be longer than one inch in length, and should be kept as short as possible. Stub lengths of 1 inch or greater will cause the propagating signal to bounce off the high impedance end of the stubs and degrade the signal. Multiple reflections can travel up and down the line causing ringing, overshoot and undershoot which reduces the noise margin too.

The fast t_r of the DS90C031 allows the driver to achieve a higher bandwidth, but transmission line characteristics can easily crop up on a system board if not handled properly at these edge rates. To make the device work to its fullest capability, the LVDS DS90C031 and the DS90C032 should be operated in a point-to-point configuration with minimum discontinuities on the transmission line. This ensures no stub problems on the line. The media ***must*** be terminated by a 100Ω line-line termination at the far end. A 100Ω termination terminates the two differential line in its characteristic impedance and also provides the differential voltage (V_{OD}) for the current mode driver. Under the above conditions the driver can drive a twp (twisted pair) wire over 10m at speeds in excess of 155.5 Mbps (77.7 MHz).

BI-DIRECTIONAL APPLICATION ON ONE TWP

In a bi-directional application data can flow in only one direction at a time (see *Figure 8*) over the single twisted pair, however the bus needs to be terminated at both ends. This requires two 100Ω terminating resistors, assuming the cable impedance is 100Ω (one direction at a time). In *Figure 8,* Rt1 terminates the signal when D1 is driving, and Rt2 terminates the signal when D2 is driving. But, since the drivers are current mode (~4 mA), the two resistors in parallel will load down the driver ($100 \parallel 100 = 50\Omega$) which cuts the signal in half. This reduces systems noise margin to only 25 mV, as the minimum driver V_{OD} is now 125 mV, and the receiver threshold is 100 mV.

Another issue to be considered for a bi-directional configuration is that the DS90C032 receivers on the line in *Figure 8* must be left powered ON all the time. If they are powered OFF while a driver on the bus is ON, the internal protection diodes of the receiver input structure can turn ON and clamp the line to a diode drop above GND. This will disrupt the bus.

Since the driver output swing is severely attenuated due to dual parallel termination load, the bi-directional approach over one twp is not recommended. A separate twp should be used for the opposite direction.

A possible solution is to use 200Ω resistors in place of the 100Ω resistors at both ends of the cable to solve the loading problem. Even though this setup will obtain the correct V_{OD}, the line will not be properly terminated. Most cables are not available with 200Ω differential impedance. Typical cables are between 100Ω to 150Ω. This mismatch in impedance creates positive reflections which degrades signal quality severely. Once again, this setup is also not recommended.

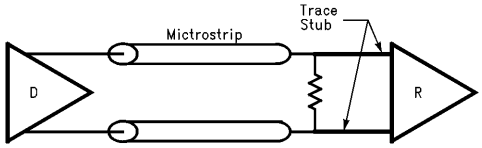

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FIGURE 7. A Point-to-Point Configuration Using LVDS

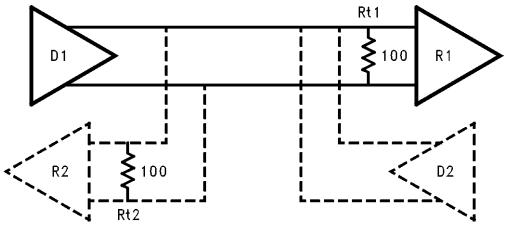

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FIGURE 8. Bi-Directional Application over One Pair of Twp

MULTI-DROP CONFIGURATION

In a multidrop configuration (see *Figure 9*), 10 receivers or more can be tied to the bus. Unused receivers (DS90C032) should be disabled and not powered OFF as explained previously. A powered OFF receiver input presents a low impedance to the bus. When the receiver is powered ON, the receiver input presents a high impedance and multiple parallel receivers on the bus will not adversely load down the line. Also, the stubs between the line and each receiver have the potential to create reflections if they are too long, or cause an impedance discontinuity.

SIGNAL QUALITY ACROSS CABLE

There are numerous ways of determining signal quality on the transmission media. Bit Error Rate (BER), Jitter, Eye Pattern, ratio of rise time and unit interval are some of the different ways designers use to determine signal quality. In this article, Eye pattern will be used to demonstrate signal quality for LVDS driver and receiver.

In order to create an Eye pattern, a PRBS (Pseudo Random Bit Sequence) of 511 ($2^9 - 1$) bits NRZ data was used to drive the LVDS driver inputs. The LVDS driver was connected to a LVDS receiver with a 10m, 25 pair, 28AWG, twp cable (SCSI grade cable). The Eye was plotted on the differential driver output at 155.5 Mbps and also at the receiver input at the end of the cable (see *Figures 10a* and *10b*).

A random data pattern is more prone to Inter Symbol Interference (ISI). There is a greater chance of errors occurring from Inter Symbol Interference as duration of pulses get shorter and shorter. A bit arriving at the receiver input might not have enough time to cross the threshold before the arrival of the next bit, resulting in lost data.

A PRBS with a pattern depth of 511 bits or 2047 ($2^{11} - 1$) or 32767 ($2^{15} - 1$) minimum should be used to generate Eye pattern. The Eye pattern is then used to characterize inter symbol interference issues. The opening of the Eye determines the signal quality, and jitter can be measured at the crossing point. Other Industry standards, SONET/SDH for example, specifies Eye patterns for signal quality analysis. LVDS technology demonstrates a wide eye opening at 155.5 Mbps over the 10m top cable. Also refer to application note AN-808 ''Long Transmission Line and Data Signal Quality'' for more discussions on signal quality.

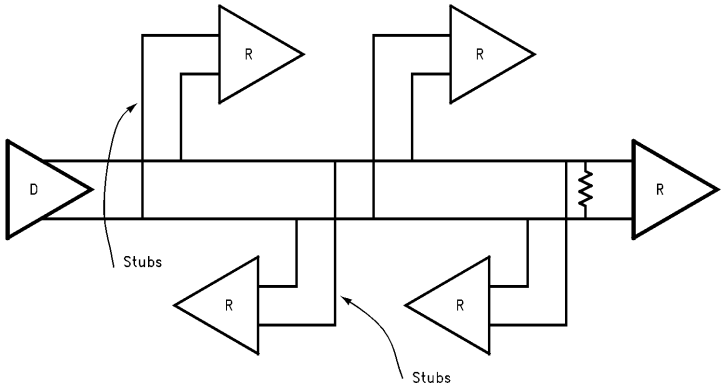

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FIGURE 9. Multi-Drop Configuration for LVDS

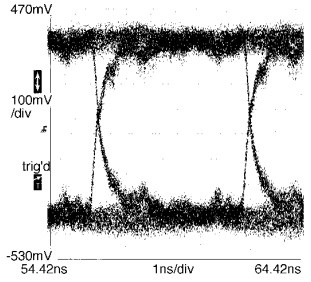

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FIGURE 10a. Eye Pattern at Driver Output

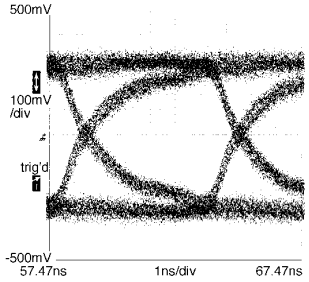

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FIGURE 10b. Eye Pattern at Receiver Inputs with 10m Cable

LVDS ASIC CELL

LVDS ASIC cells are low in power, operate at high data rates and are implemented using CMOS technology. These are characteristics that ASIC designers look for to satisfy their design requirements.

LVDS ASIC Leaf cells and Macro cells are available through National Semiconductor's SCLO8 ASIC library. The leaf cell is the smallest form of cell available for ASIC designs and the Macro cell combines different combinations of the Leaf cell. *Figure 11* illustrates the use of LVDS ASIC cells within an ASIC Core device.

The receiver leaf cell has inputs to the external world and the receiver cell output is an internal node to the ASIC Core. The driver cell's outputs are external to the world while the driver's input in an internal node.

The ASIC cells are fully compatible with the SCI-LVDS and the TIA LVDS standards.

By MUX'ing and DeMUX'ing signal lines within the ASIC core, higher data rates can be achieved that are impossible with standard TTL/CMOS. The data rate of the LVDS DS90C031/C032 is mainly limited by the technology that drives it. ASICs can achieve data rates beyond 622 Mbps by transporting data through LVDS I/O's.

CONCLUSION

LVDS technology solves the ever increasing data rate problem while decreasing power dissipation and can be widely used in Telecom, Routers, Intelligent Hubs, LCD displays, Copiers and numerous other exciting applications. LVDS technology provides the best solution for power budget requirements in today's designs. This high speed interface allows designers to implement a simple point-to-point link without complex termination issues. ASIC availability allows for the integration of standard controller functions and single chip solutions. LVDS technology provides solutions for what designers are looking for in a Physical Layer point-to-point interface.

REFERENCES

To order a copy of IEEE SCI standard contact:
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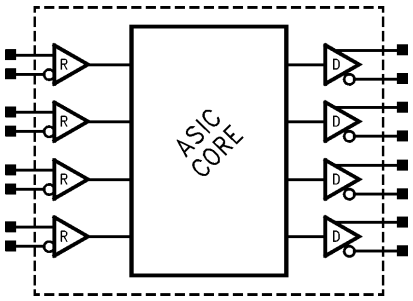

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FIGURE 11. ASIC Cell Implementation of LVDS

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