National Semiconductor

NM95MS15 User's Guide

The User's Guide contains the description of certain internal registers and Plug and Play resource data registers in EEPROM. The Internal Registers are used by the chip for Power On Configuration. The Plug and Play resource data registers are for Plug and Play resource allocation.

Power-On Configuration Load for the NM95MS15

Power-on defaults for certain internal registers which determine some fundamental characteristics of the NM95MS15 are loaded from the EEPROM. The details of the addresses and their settings are indicated below. The on-chip EEPROM for the NM95MS15 has 16-bit wide data registers. The table below therefore assumes 16-bit wide data registers.

Word Address	Byte Address	Purpose of the 16-bit Register
00	0000	I/O Decode Qualification Bits
01	0002	DMA Level Selection Bits
02	0004	Interrupt Level Selection-A
03	0006	Interrupt Level Selection-B
04	0008	Chip Select 0 Decode Size
05	000A	Chip Select 1 Decode Size
06	000C	Chip Select 2 Decode Size
07	000E	Chip Select 3 Decode Size
08	0010	Reserved for Future Use
09	0012	Reserved for Future Use
0A	0014	Reserved for Future Use
0B	0016	Reserved for Future Use
0C	0018	Reserved for Future Use
0D	001A	Reserved for Future Use
0E	001C	Reserved for Future Use
0F	001E	Reserved for Future Use
10	0020	Vendor ID
11	0022	Vendor ID
12	0024	Serial Number
13	0026	Serial Number
14 (LSB)	0028	LSB = Checksum of (Vendor ID + Serial Number)
14 (MSB)	0029	MSB = Start of Resource Data Structure

Each of the above registers is now discussed in detail below.

I/O DECODE QUALIFICATION REGISTER:

15–14	13	12	11–10	9–8	7–4	3	2	1	0
RFU	MRW1	MRW0	RFU	MS	RFU	RWQ3	RWQ2	RWQ1	RWQ0

RWQ <3:0>: Read, Write Qualify: If this bit is set to 0, then the I/O chip selects are qualified by IOWR in a write cycle and IORD in a read cycle. If 1, the I/O chip selects are derived from addresses only.

MS: Mode Select Bits. If these bits are set to ''00'', then Normal DMA mode is selected. When set to ''01'' Extended Interrupt/Chip-select expansion mode is selected. When set to ''10'', then Extended DMA mode is selected.

MRW <1:0>: MEMORY Read, Write Qualify: If this bit is set to 0, then the MEMORY chip selects are qualified by SMEMW* in a write cycle and SMEMR* in a read cycle. If 1, the MEMORY chip selects are derived from addresses only.

RFU: Reserved for Future Use: Must be set to ''0''.

DMA LEVEL SELECTION REGISTER:

15–9	8–6	5–3	2–0
RFU	ISA DRQ2	ISADRQ1	ISA DRQ0

ISADRQ<2 : 0>: These pins will be physically connected to ISA DRQ lines. This will allow the user to customize his choice of 3 out of 7 available ISA DRQ channels on the bus. For example if ISADRQ0 is connected to DRQ5 on the ISA bus then bits ''2–0'' should be set as ''101'' meaning ISADRQ0 is assigned to DRQ/DACK 5.

This register is valid only for Normal DMA mode (MODE ''00'') and Extended DMA mode (MODE 02). For Mode ''01'' all of the bits of this register are Don't care.

RFU: Reserved for Future Use: Must be set to ''0''.

INTERRUPT LEVEL SELECTION REGISTER—A:

15–12	11–8	7–4	3–0
IRQOUT3	IRQOUT2	IRQOUT1	IRQOUT0

INTERRUPT LEVEL SELECTION REGISTER

15–12	11–8	7–4	3–0
IRQOUT7	IRQOUT6	IRQOUT5	IRQOUT4

Power-On Configuration Load for the NM95MS15 (Continued)

IRQOUT[7:0]: These pins will be physically connected to the ISA IRQ lines on the bus as specified in the registers above. This will enable the user to customize his choice of 8 out of 11 available ISA IRQ channels. For example, if IRQOUTO is assigned to IRQ7 on the ISA bus, then bits ''3–0'' should be set as ''0111'', meaning IRQOUT0 is assigned to IRQ7. In DMA mode bits (8–15) of Interrupt Level Selection Register-B are Don't Care.

IRQOUT[10: 8]: These pins are hard coded to IRQ10, IRQ11, IRQ12 on the ISA bus.

CHIP SELECT DECODE SIZE REGISTER <3:0>:

15–8	7–0
RFU	Chip Select Decode size

Chip Select Decode Size: These bits function as masks in the chip select decode function and will set the size of the decode (from the base address) according to the selections as shown.

Chip Select Decode Size Bits:	Decode Size
00000000	1 byte
00000001	2 bytes
00000011	4 bytes
00000111	8 bytes
00001111	16 bytes
00011111	32 bytes
00111111	64 bytes
01111111	128 bytes
11111111	256 bytes

RFU: Reserved for Future Use.

Vendor ID Registers: The lower address contains the least significant word of the Vendor ID (as defined in the Plug and Play Standard) and the higher address contains the most significant word.

Serial Number Registers: The lower address contains the least significant word of the Serial number of the Card (as defined in the Plug and Play Standard) and the higher address contains the most significant word.

Checksum Register: This 8-bit quantity occupies the lower 8-bits of the word at address 0014 (Byte address 0028). This checksum is the LFSR checksum of the vendor ID and the Serial Number. Please refer to the P and P standard on how to compute this checksum.

Start of Resource Data Structure: The resource data structure begins at the MSB of word address 0014 (Byte address 0029).

Plug and Play Registers Implemented on the NM95MS15

TABLE A. Plug and Play Standard Registers

Name	Address Port Value	Definition
Set RD__DATA Port	0x00	Writing to this location modifies the address of the port used for reading from the Plug and Play ISA cards. Bits[7:0] become I/O read port address bits[9:2]. Reads from this register are ignored.
Serial Isolation	0x01	A read to this register causes a Plug and Play cards in the ***Isolation*** state to compare one bit of the boards ID. This process is fully described above. This register is read only.
Config Control	0x02	Bit[2]—Reset CSN to 0 Bit [1]—Return to the ***Wait for Key*** state Bit[0]—Reset all logical devices and restore configuration registers to their power-up values. A write to bit[0] of this register performs a reset function on all logical devices. This resets the contents of configuration registers to their default state. All card's logical devices enter their default state and the CSN is preserved. A write to bit[I] of this register causes all cards to enter the ***Wait for Key*** state but all CSNs are preserved and logical devices are not affected. A write to bit[2] of this register causes all cards to reset their CSN to zero. This register is write-only. The values are not sticky, that is, hardware will automatically clear them and there is no need for software to clear the bits.
Wake[CSN]	0x03	A write to this port will cause all cards that have a CSN that matches the write data[7:0] to go from the ***Sleep*** state to either the ***Isolation*** state if the write data for this command is zero or the ***Config*** state if the write data is not zero. Additionally, the pointer to the byte-serial device is reset. This register is write-only.
Resource Data	0x04	A read from this address reads the next byte of resource information. The Status register must be polled until bit[0] is set before this register may be read. This register is read only.
Status	0x05	Bit[0] when set indicates it is okay to read the next data byte from the Resource Data register. This register is read-only.
Card Select Number	0x06	A write to this port sets a card's CSN. The CSN is a value uniquely assigned to each ISA card after the serial identification process so that each card may be individually selected during a Wake[CSN] command. This register is read/write.
Logical Device Number	0x07	Selects the current logical device. All reads and writes of memory, I/O, interrupt and DMA configuration information access the registers of the logical device written here. In addition, the I/O Range Check and Activate commands operate only on the selected logical device. This register is read/write. If a card has only 1 logical device, this location should be a read-only value of 0x00.

Plug and Play Registers Implemented on the NM95MS15 (Continued)

TABLE A-1. Plug & Play Logical Device Control Registers

Name	Address Port Value	Definition
Activate	0x30	For each logical device there is one activate register that controls whether or not the logical device is active on the ISA bus. Bit[0], if set, activates the logical device. Bits[7:I] are reserved and must return 0 on reads. This is a read/write register. Before a logical device is activated, I/O range check must be disabled.
I/O Range Check	0x31	This register is used to perform a conflict check on the I/O port range programmed for use by a logical device. Bit[7:2] Reserved and must return 0 on reads Bit[1] Enable I/O Range check, if set then I/O Range Check is enabled. I/O range check is only valid when the logical device is inactive. Bit[0], if set, forces the logical device to respond to I/O reads of the logical device's assigned I/O range with a 0x55 when I/O range check is in operation. If clear, the logical device drives 0xAA. This register is read/write.
Memory base address bits[23:16] descriptor 0	0x40	Read/write value indicating the selected memory base address bits [23:16] for memory descriptor 0.
Memory base address bits[15:8] descriptor 0	0x41	Read/write value indicating the selected memory base address bits [15:8] for memory descriptor 0.
Memory control	0x42	Bit[1] specifies 8-/16-bit control. This bit is set to indicate 16-bit memory, and cleared to indicate 8-bit memory. Bit[0], set always indicates the next field is the upper limit for the address. Bit[0] is read-only.
Memory upper limit address bits[23:16] or range length bits[23:16] for descriptor 0	0x43	Read/write value indicating the selected memory high address bits[23:16] for memory descriptor 0. If bit[0] of memory control is 0, this is the range length. If bit[0] of memory control is 1, this is upper limit for memory address (equal to memory base address plus the range length allocated).
Memory upper limit address bits[15:8] or range length bits[15:8] for descriptor 0	0x44	Read/write value indicating the selected memory high address bits[15:8] for memory descriptor 0, either a memory address or a range length as described above..
I/O port base address bits[15:8] descriptor 0	0x60	Read/write value indicating the selected I/O lower limit address bits[15:8] for I/O descriptor 0. If a logical device indicates it only uses 10 bit decoding, then bits[15:10] do not need to be supported.
I/O port base address bits[7:0] descriptor 0	0x61	Read/write value indicating the selected I/O lower limit address bits[7:0] for I/O descriptor 0.
I/O port address descriptors 1–2	0x62–0x65	I/O base addresses for I/O descriptors 1–2
I/O port base address bits[15:8] descriptor 3	0x66	Read/write value indicating the selected I/O base address bits[15:8] for I/O descriptor 3. If a logical device indicates it only uses 10 bit decoding, then bits[15:10] do not need to be supported.
I/O port base address bits[7:0] descriptor 3	0x67	Read/write value indicating the selected I/O base address bits[7:0] for I/O descriptor 3.

Plug and Play Registers Implemented on the NM95MS15 (Continued)

TABLE A-2. Interrupt Configuration

Name	Register Index	Definition
Interrupt request level select 0	0x70	Read/write value indicating selected interrupt level. Bits[3:0] select which interrupt level is used for Interrupt 0. One selects IRQL 1, fifteen selects IRQL fifteen. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
Interrupt request type select 0	0x71	Read/write value indicating which type of interrupt is used for the Request Level selected above. Bit[I]: Level, 1 = high, 0 = low Bit[0]: Type, 1 = level, 0 = edge If a card only supports 1 type of interrupt, this register may be read-only.
Interrupt request level select 1	0x72	Read/write value indicating selected interrupt level. Bits[3:0] select which interrupt level is used for Interrupt 0. One selects IRQL 1, fifteen selects IRQL fifteen. IRQL 0 is not a valid interrupt selection and represents no interrupt selection.
Interrupt request type select 1	0x73	Read/write value indicating which type of interrupt is used for the Request Level selected above. Bit[1]: Level, 1 = high, 0 = low Bit[0]: Type, 1 = level, 0 = edge

TABLE A-3. DMA Channel Configuration

Name	Register Index	Definition
DMA channel select 0	0x74	Read/write value indicating selected DMA channels. Bits[2:0] select which DMA channel is in use for DMA 0. Zero selects DMA channel 0, seven selects DMA channel 7. DMA channel 4, the cascade channel is used to indicate no DMA channel is active.
DMA Channel Select	0x75	Read/write value indicating selected DMA chanels. Bits[2:0] select which DMA channel is in use for DMA 1. Zero selects DMA channel 0, seven selects DMA channel 7. DMA channel 4, the cascade channel is used to indicate no DMA channel is active.

Programming Interface

TABLE A-4. Programming E2PROM Register

Name	Register Index	Definition
Status and Command Register	0xF0	Bit[I:0]—OP Code bits 10—Read operation 01—Write operation 11—Erase operation Bit[2]—GA (Go ahead bits) If set to I, the programming will continue Bit[3]—Status/Busy Since EEPROM is a slow device, this bit is provided to show that EEPROM is still BSY and the previous data is getting programmed. The user program should poll this bit and should proceed only if this bit is 0. If it is set to 1, it means BSY. Bit[6:4]—Reserved, should be 0 Bit[7]—It provides A8 of the address [A0–A7] is provided by Address Reg.
Address Register	0xF1	Address Register [A0–A7]
Data Register	0xF2	Data Byte [MSB]
Data Register	0xF3	Data Byte [LSB]

Programming Interface (Continued)

EEPROM PROGRAMMING METHOD

A total of 8k bits of EEPROM is available on-chip. Of this, 4k bits are dedicated for the Plug and Play Access and the 4k bits are available for access externally. For purposes of programming the contents of the EEPROM, the entire 8k bits are accessible via the ISA bus.

Specifically, the contents of the EEPROM may be altered by putting the device in the Config State (as defined in the Plug and Play Standard). Under this state, the following registers detailed above are accessible. The data to be programmed is loaded in registers at address 0xF3 and 0xF2 (LSB and MSB respectively). The address to be programmed is loaded in register at address 0xF1. Addressing 8k bits of memory requires 9 bits of address. The ninth bit of address is provided through the register at address 0xF0.

Both read and write operations are possible. The opcodes are as indicated in the table. The actual operation does not begin until the Go Ahead (GA) bit is set. Programming a word takes approximately 10 ms. The status of the operation can be polled by the status bit. This bit is set when the operation is in progress and will be reset when complete.

AVAILABILITY OF EXTRA 4k EEPROM

The Extra 4k EEPROM built into NM95MS15 for the Functional logic to be used for other purposes becomes available after the DO pin on the EEPROM Microwire port becomes high. This DO pin is pulled low when the EEPROM is accessed internally by the Plug and Play logic.

LEGACY ISA SYSTEMS

The LEGACY system collectively refers to Older ISA cards or Systems that are not Plug and Play compatible (Motherboard BIOS being Non Plug and Play compliant)

In a LEGACY system there can be two of the following situations where NM95MS15 will be used.

a) NM95MS15 on a Non Bootable ISA ADD-ON Plug and Play Card.

   Under this situation, the card will be Powered ON inactive. Once the system is Booted, NM95MS15 can be configured by the O/S (Windows'95) or by the external P and P utilities.

b) NM95MS15 on a Bootable ISA ADD-ON Plug and Play Card.

   Since the card cannot on its own come up active unless some P and P Software configures it, NM95MS15 cannot be used for a Bootable card on a Legacy system.

EEPROM CHARACTERISTICS (FOR EXTERNAL ACCESS)

Symbol	Parameter	Conditions	Min	Max	Units
f_{SK}	SK Clock Frequency		0	1	MHz
t_{SKH}	SK High Time		250		ns
t_{SKL}	SK Low Time		250		ns
t_{SKS}	SK Setup Time		50		ns
t_{CS}	CS Low Time (min)		250		ns
t_{CSS}	CS Setup Time	Relative to	50		ns
t_{DH}	DO Hold Time	Relative to	70		ns
t_{DIS}	DI Setup Time	Relative to	100		ns
t_{DIH}	DI Hold Time	Relative to	20		ns
t_{PD1}	Output Delay to "1"	Relative to		500	ns
t_{PD0}	Output Delay to "0"	Relative to		500	ns
t_{SV}	CS to Status Valid	Relative to		500	ns
t_{DF}	CS to DO in TRI-STATE	$CS = V_{IL}$		100	ns
t_{WP}	Write Cycle Time	$CS = V_{IL}$		10	ms