Bus Switches in the Presence of Undershoot

National Semiconductor
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Bus switch products have become a powerful tool in the modern desk top and portable personal computer. They have a number of positive attributes relative to standard bus transceivers. The bus switch parts are faster, consume a negligible amount of power, and introduce none of the noise issues associated with the typical high drive transceiver. In most applications, use of the bus switch will alleviate all the problems of the bus transceiver without creating new ones.

However, in the presence of large amounts of undershoot, typically associated with unterminated transmission lines, bus switches can misbehave. Most people's concern with undershoot pertains to latchup. The bus switch has been characterized for latchup and exceeds 500 mA, the limit of our tester. The issue at hand is data corruption for a small percentage of applications.

This application note will outline the specifics of the applications that can cause problems, list ways of avoiding the problem with system initiatives, and display the ''Undershoot Hardened'' design that is now available.

In the application of *Figure 1* the bus switch is used as a pathway for data from the A-Bus to move to the B-Bus, or vice versa. When the pin $\overline{BE}$ is a logic one, the two busses are expected to be isolated with any combination of activity that occurs on the two busses.

Assume, for the moment, that $\overline{BE}$ is a logic one and Bus-A is switching as data is written from one storage device to another. Also assume that Bus-A is either unterminated, or poorly terminated. If Bus-A transitions from a 0V to V_{CC}, the end of the bus will try to double to 2 * V_{CC}. This positive excursion, while probably not healthy for the system, will not bother the bus switch. A low going transition is a different story. In the low-going case, V_{CC} to 0V, the voltage swing will attempt to double to $-V_{CC}$. Their exists a clamp diode on the input of the bus switch that will limit the undershoot voltage to approximately -0.65V, but by then the fault has occurred.

For most functions found in family logic data books, a path from input to output exists where the signal must propagate through any number on inverters or complex logic gates. The bus switch is special in that its path is exceedingly simple. The data passes through a simple, but big, N-channel transistor. When $\overline{BE}$ is a ''1'', the gate of this transistor is at 0V. If the switching bus undershoots ground, the source of the transistor will be lower than the gate by $\approx$ 0.65V. The NMOS V_T for National Semiconductor's process is approximately 0.65V, thus enabling the bus switch to activate weakly and pass a logic ''0'' to a bus from which it is supposed to be isolated. If the B-Bus during the isolation, is passively pulled to a logic high as shown in *Figure 1.* The undershoot on the A-Bus may result in B-Bus's signals being pulled low. Were the B-Bus being actively driven, data corruption would be unlikely. The bias conditions during the undershoot makes the N-channel (N1), when it does turn on, weak in comparison to an output buffer.

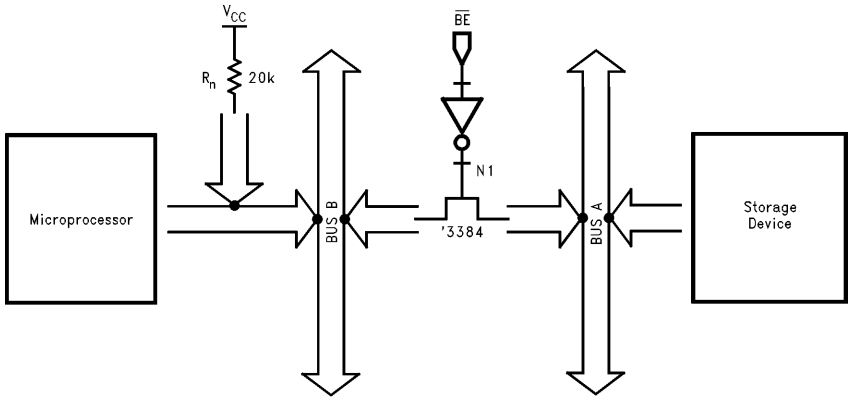

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FIGURE 1. '3384 Application

Sometimes, the standard solutions listed below are not feasible:

- Parallel or Thevinen terminate the bus—Can handle the increase in system power associated with these termination schemes.
- Series terminate the bus—Not enough room for the chip resistors on the printed circuit board.
- Integrate the series terminator within the peripheral storage devices, either as discrete resistors or intergated into the silicon drivers—The storage devices are being supplied by multiple third party vendors to existing industry standards.

When these system-type solutions are not possible, an ''Undershoot Hardened'' silicon approach should be pursued. One silicon technique, used by some vendors, is to increase the effective NMOS V_T of the bus switch. This is done by pumping the substrate to a voltage below ground. Data sheets with I_{CC} currents that are specified in mA, one well known vendor or has a limit of 3 mA, are likely to use this technique.

A product like the bus switch is likely to be used multiple times in a system, either to link various busses or to handle wide busses. Incurring a 3 mA penalty per usage can be very limiting for battery operated products. To solve the undershoot problem, without incurring an increase in I_{CC}, the 74LVX3L384A extended input voltage bus switch architecture was modified to that shown in *Figure 2.*

When $\overline{BE}$ is a logic ''1'', both N1 and N2 transistors are off and the PMOS (P1) on. The intermediate point between the N1 and N2 is actively pulled to V_{CC} by P1. When severe undershoot is present, the NMOS on the side with the undershoot may turn on. However, now P1 will hold the intermediate point high enough to prevent the opposite side NMOS from switching on by keeping $V_{GS} < V_{TN}$. This solution has been verified in the problematic applications to completely isolate the two busses.

Specification Changes for the 74LVX3L384A

- R_{ON} @ 0V — From 7Ω–10.5Ω
- R_{ON} @ 2.4V — From 15Ω–25Ω
- T_{PZL} — From 6.5 ns–6.7 ns

The ''Undershoot Hardened'' circuitry does force some datasheet specification changes. The changes include an increase in R_{ON} from using two FET's in series, and a marginal increase in T_{PZL} due to the extra capacitive load on the $\overline{BE}$ inverter. The marginal increase in phase delay through the bus switch as a result of RON's change, coupled with the ZL delta, should be attractive relative to a factor of 100 (3 μA–3 mA) increase in I_{CC}.

Many unattractive behaviors can result from neglecting transmission line theory. Use of the 74LVX3L384A should be considered as an aid to get through a marginal termination situation, not as a substitue for sound engineering practice.

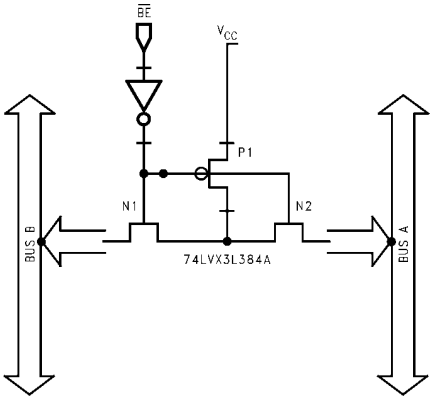

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FIGURE 2. 74LVX3L384A ''Undershoot Hardened'' Bus Switch

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