Phase-Locked Loop Based Clock Generators

National Semiconductor
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INTRODUCTION

As system clock frequencies reach 100 MHz and beyond, maintaining control over clock becomes very important. In addition to generating the various clocks for the CPU, the clock generator must also provide other clocks for the peripheral interfaces such as PCI, video and graphics, and peripheral devices like FDC, KBD (Key Board Clock), etc. (see *Figure 1* below). This note will show the advantages of using the Phase Locked Loop (PLL) and also describe the precautions required for designing circuits employing Phase-Locked Loops.

Today's system places stringent requirements on the clock generators which involve shortest possible rise/fall times and propagation delay, tighter skew specifications, and minimum jitter.

The PLL-based Clock Generator provides a cost effective solution for generating various frequencies that are required in today's system and it meets the demand for tighter specifications of important parameters like skew and jitter.

FREQUENCY SYNTHESIS AND FREQUENCY DIVIDERS

A frequency synthesis technique and frequency dividers are used to generate multiple frequencies from an accurate reference frequency, usually a crystal oscillator. PLL is best suited for the frequency synthesis. Examples of the dividers are: counters, prescalers, etc. PLL uses digital frequency dividers. Since it is difficult to obtain a crystal resonating at a very low frequency, the output frequency in the example below is obtained by dividing a higher crystal frequency by n.

Figure 2 shows a frequency synthesizer in a simple form. For a fixed input frequency f_{IN} the desired output frequency f_O is generated by selecting the proper integer n. In actual designs, programmable counters and dividers are used in place of n.

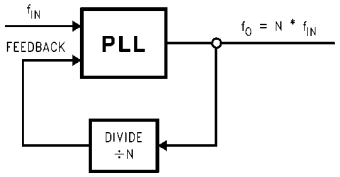

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FIGURE 2. PLL with Simple Divider

Figure 3 shows two dividers: one in the reference path and one in the feedback path. In this configuration the output frequency will be: $f_{OUT} = (m/n)\ f_{IN}$. In this manner, the non integer frequencies can be developed. Also note that when using the prescalar, jitter will increase due to slower update rate.

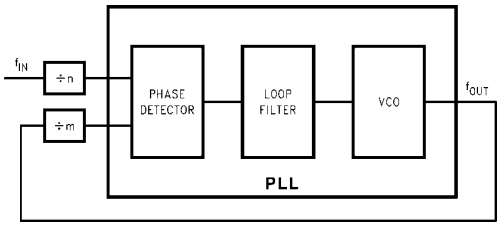

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FIGURE 3. PLL with Dividers/Counters

FUNCTIONAL DESCRIPTION OF PHASE-LOCKED LOOP

A phase-locked loop is basically an oscillator whose frequency is locked onto some frequency component (f_{IN}) of an input signal. The phase detector compares the phases of the input signal f_{IN} and the VCO output and generates current pulse for the loop filter whose width is proportional to the phase error. This voltage is applied as a control voltage

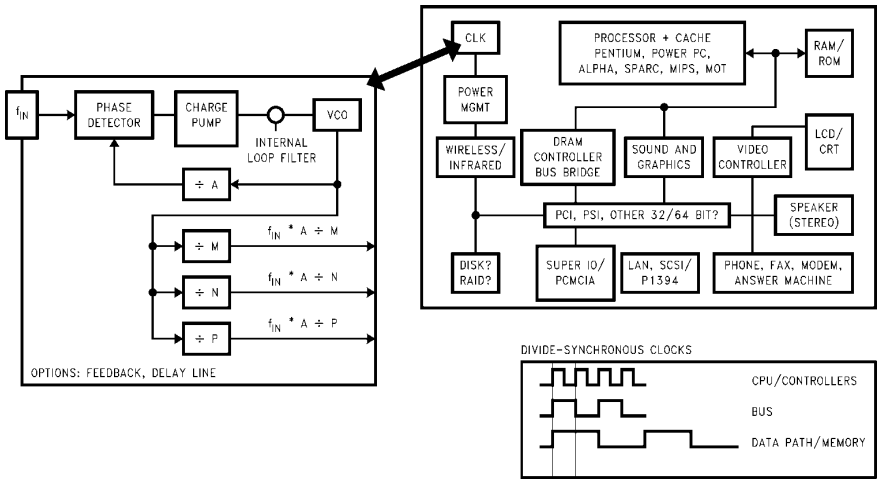

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FIGURE 1. Typical System Diagram

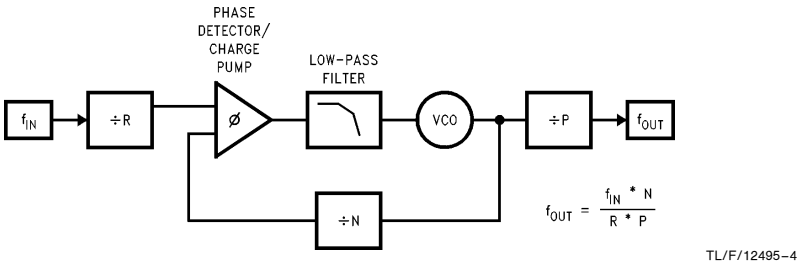


FIGURE 4. Block Diagram of PLL

to adjust the oscillator frequency. Through negative feedback, the PLL causes the input reference frequency and the VCO output frequency to be equal (with minimum phase error). Thus, both the phase and the frequency of the oscillator are locked to the phase and the frequency of the input signal. The basic elements of the PLL are:

1. Reference input source
2. Phase Detector
3. Digital frequency divider
4. VCO (Voltage Controlled Oscillator)
5. Loop Filter

The reference source frequency is usually supplied by the crystal. The phase detector acts as a multiplier and produces a sum frequency component as well as the difference component. The Phase detector consists of:

1. Digital Phase comparator
2. Charge Pump for pumping the charge up or down in the VCO

A typical digitally controlled analog PLL consists of a reference counter (R), feedback counter (N), post-scaling counter (P), and the core analog blocks which include a phase detector/charge pump, low-pass loop filter and the VCO itself. The R and P counters provide additional programming resolution in the system and are optional.

A charge pump is usually associated with the phase detector. The function of the charge pump is to convert the logic states of the detector into analog signals appropriate for controlling the VCO. The charge pump (in off state) and the input section of the VCO must have very low leakage tendency; otherwise, a voltage integration will occur at the loop filter between phase comparison events.

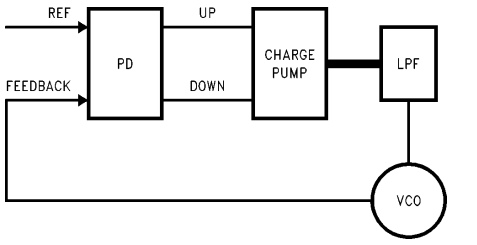


FIGURE 5. Block Diagram of Charge Pump

The phase detector provides a signal to charge pump to decrease or increase the control voltage of the VCO. The change in control voltage will in turn change the frequency/phase of the VCO. The detector involves a set of latches or flip-flops. Either configuration includes a common reset path for terminating the pump-up and pump-down output pulses simultaneously at the end of a phase comparison event. The overlap region of the output pulses should be sufficiently wide so that the charge pump current sources always reach 100% of their final value before being gated off.

LOOP FILTER

When two AC signals are multiplied together, the result is a DC signal and an AC signal at twice the frequency of an original signal. The Loop Filter is a low pass filter and is added to remove the 2x frequency component from the signal. Loop filters can either be integrated on the chip or can be external to the device, depending on their size, impedance and application requiring user control. The on-chip filters are less subject to noise. However, they can consume significant die area. Off-chip filters require more pins on the device.

FREQUENCY DIVIDERS AND SCALARS FOR MULTIPLE FREQUENCY GENERATION

With the implementations of post scalars/dividers, various output frequencies can be generated as shown in *Figure 6*.

When generating multiple output frequencies, there is a trade off between the jitter and the frequency accuracy. If the preschooler has a smaller value, the reference frequency and hence the update rate will be higher. This will result in lower jitter; however, the desired output frequency in this case may not be the exact frequency. The frequency error is described in PPM as shown below:

$$\text{PPM} = \frac{\text{Actual Frequency—Required Frequency}}{\text{Required Frequency}}$$

IMPORTANT PARAMETERS ASSOCIATED WITH PLL

When designing circuits using PLLs, the skew and jitter are the critical parameters and proper care should be taken in the design and layout of the circuit to minimize both the skew and jitter.

CLOCK SKEW

Skew between the outputs of the clock generator is a result of the difference in the propagation delay between the various circuit components inside the chip.

As the clock signal propagates through the different stages in the device, it is delayed by the logic sections and interconnects. Clock skew is the tolerance in the arrival time of the active edge of the pulse. Skew is introduced in the device by:

1. The propagation delay tolerances due to transistor mismatching
2. Parasitic mismatching in interconnect
3. Package parasitic mismatching

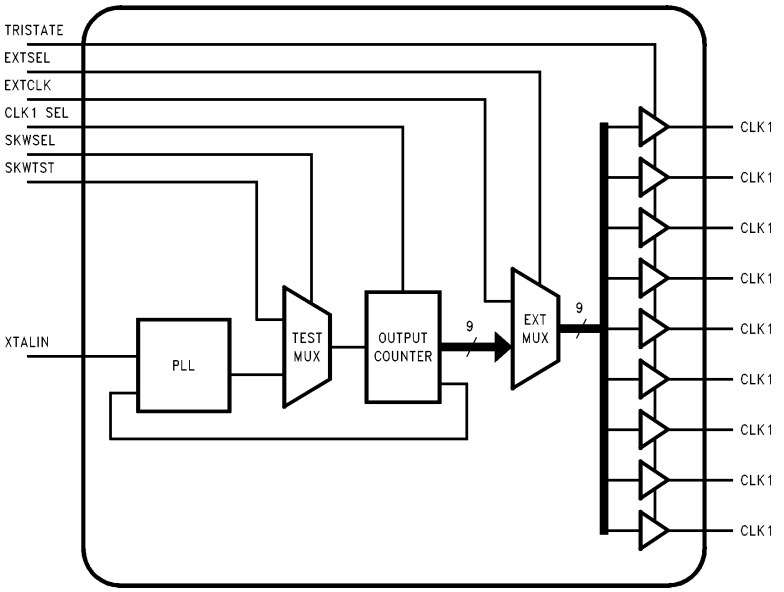


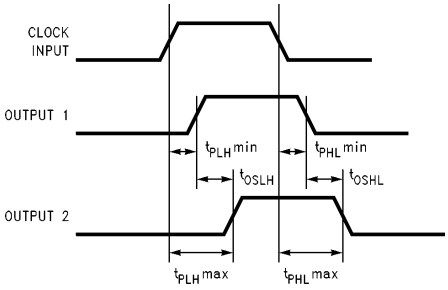
FIGURE 6. PLL-Based Clock Generator (CGS700)

The following four types of skews are defined by JEDEC:

1. Pin-to-pin skew (output skew)
2. Input skew
3. Pulse skew
4. Process skew (part-to-part skew)

PIN-TO-PIN SKEW (Output Skew)

Output skew is the difference in propagation delay between the fastest and the slowest output for a single device having a single input clock.



Output Skew for Low-to-High Transaction $t_{OSLH} = t_{PLH}$ max $- t_{PLH}$ min

Output Skew for High-to-Low Transaction $t_{OSHL} = t_{PHL}$ max $- t_{PLH}$ min

FIGURE 7. Waveform Showing Skew

INPUT SKEW

Input skew is the difference in propagation delay for a specific device output that can emanate from more than one input to the device. This skew applies to a multiple input gate.

PULSE SKEW

Pulse skew is the difference between the propagation delay of t_{PHL} and t_{PLH} specifications on the same output for a device at identical operating conditions.

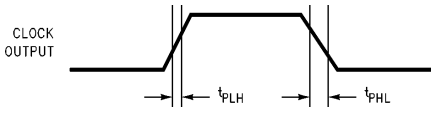


FIGURE 8. Pulse Skew

PROCESS SKEW

Process skew is the difference in the propagation delay between outputs of two equivalent devices when the devices have a common input clock. This skew is also referred to as part-to-part skew.

JITTER

Jitter is another critical performance parameter of the PLL-based clock generators. Since the VCO is locked to a low jitter reference, usually a crystal, most of the jitter at the output results from noise sources feeding back on the phase detector, loop filter and VCO. However, with proper care in the PLL design, the VCO is the most dominant component responding to the noise which results in jitter.

Jitter can be contributed by many sources. Injection of unwanted signals from other parts of the circuits through the power supply can also contribute to jitter. Designing differential stages, for example, takes care of common mode noise on power supplies. Normally, when the design is optimized, the main source of the timing jitter could be thermal noise or shot noise of the active or passive device.

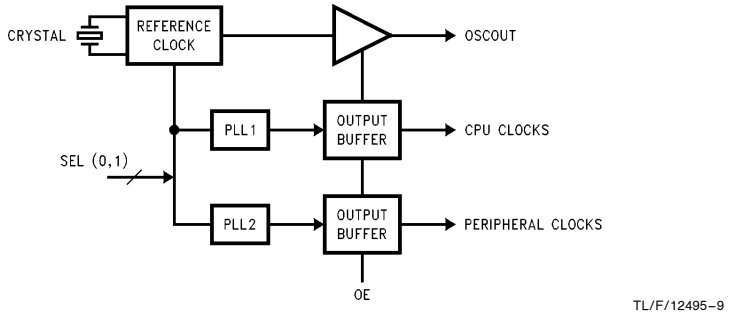


FIGURE 9. Dual PLLs

The total jitter seen at the output of a PLL-based clock generator contains two components; the intrinsic loop jitter and the effects of any reference jitter whose spectrum falls within the passband of the PLL. Generally, a PLL with narrow bandwidth can reject the input jitter but cannot correct the VCO timing errors quickly. The resultant output jitter is VCO noise limited. A PLL with wider bandwidth can correct VCO errors however, if the bandwidth is too wide, the resultant system will be input jitter limited.

When multiple frequencies are required in a system, it becomes difficult for a single PLL to generate several different frequencies with the same accuracy (i.e., minimum PPM values). In such cases, dual loops can be used for generating several multiple frequencies. When the clock generator is designed using dual PLLs, for example, one loop can generate fixed frequencies for the peripherals such as: PCI, FDC etc., while the other loop can generate variable frequencies for the CPU.

The advantages of dual loops over single loop are:

1. Dual loops can keep the design on a lower performance but more cost effective process.
2. Reduce the high frequency harmonics emitted by the loop.
3. Secondary effect: reduced I_{CC}, since CMOS power is directly related to the frequency of operation.
4. Can produce a signal for peripheral clocks (such as: FDC, KBD, etc.) at a fixed rate while other clocks (e.g., CPU clock) may change to support power management.
5. Offers flexibility. Allows a designer to change the peripheral frequencies without changing the other loop dynamics.

DESIGN CONSIDERATIONS

Several precautions are required when designing the Phase-locked loop based clock generators. Here are some of the major considerations for avoiding noise and jitter problems.

VCO

The ideal VCO has a constant linear frequency response for a change in tuning voltage, or V_{FILTER} practical implementations may include high-frequency ''roll-off'' and an idle condition. Idling the VCO at zero tuning voltage assists in reacquisition of lock since the oscillator is not required to start-up (see *Figure 10*).

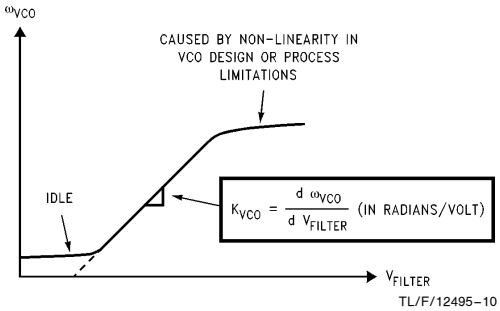


FIGURE 10. Typical VCO Tuning Characteristics

PHASE DETECTOR

In this functional representation of a type 4 phase detector, a simple delay element is inserted in the reset path to stretch the pump up and pump down pulses to the charge pump thereby ensuring zero-deadband. The type 4 phase detector will respond to any phase error from 0°–360°. Therefore, the phase detector/charge pump gain (Kp) is equal to the charge pump current divided by 2π.

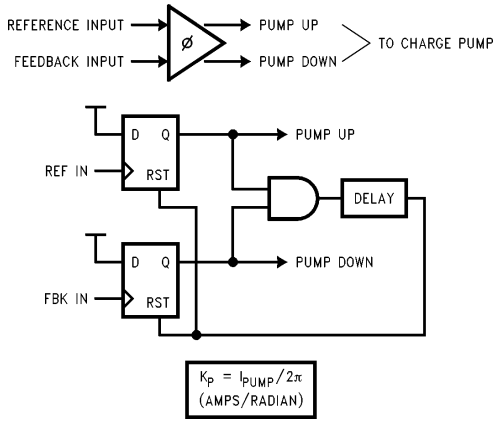


FIGURE 11. Simple Type 4 Phase Detector

PHASE DETECTOR DEADBAND

When the phase correction is not linear, it may cause the phase detector to have a deadband as shown in *Figure 12*.

In lock, REF and FBK active edges occur nearly simultaneously. Since pump-up or pump-down is active only during the time between these active transitions, practical charge pump implementations cannot respond linearly near the zero-phase condition.

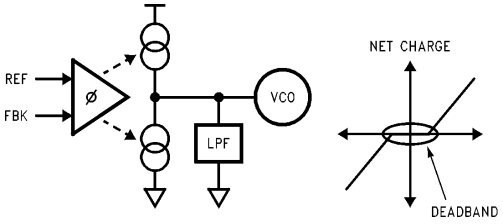


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FIGURE 12. Phase Detector Deadband

The problem of deadband in the phase detector can be eliminated by making certain that both pump-up and pump-down sources have come on before resetting the phase detector logic. This guarantees a more linear response to small phase errors since the charge pump current waveform is allowed to fully develop every reference cycle (see *Figure 13*).

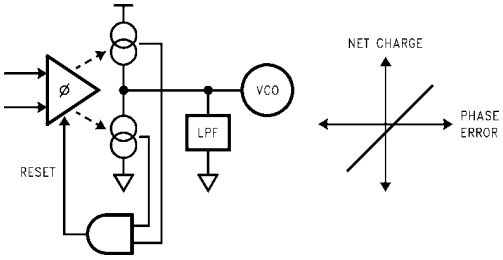

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FIGURE 13. Zero-Deadband Phase Detector

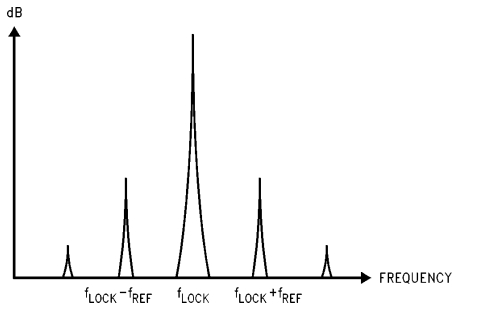

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FIGURE 14. Synthesizer Output Viewed in Frequency Domain

The spectral plot in *Figure 14* show signs of being frequency modulated at the phase detector rate. Undesirable ''reference spurs'' are caused by continuous pumping into and out of the loop filter. This condition is exacerbated by the deadband region in the phase detector/charge pump block. Increasing the loop passband towards the reference frequency will tend to reduce the amplitude of the reference spurs at the expense of increased low frequency jitter in the VCO.

LAYOUT TECHNIQUES

Figure 15 illustrates an example of the most essential layout techniques for low jitter PLL's. The use of separate, dedicated analog V_{CC}/GND pins for the core analog blocks helps isolate them from supply variations. Guard-rings (P+ and N+) surround the analog blocks and are tied to analog supplies to quiet the substrate. The external filter pin (if used) is placed between the analog power to avoid stray coupling outside the chip and magnetic coupling via bond wires. The critical blocks are placed at the corner of the die because in this way substrate resistance to the rest of the chip is maximized. If possible, use of ''white space'' between the analog blocks and the noisy areas of the die can be helpful.

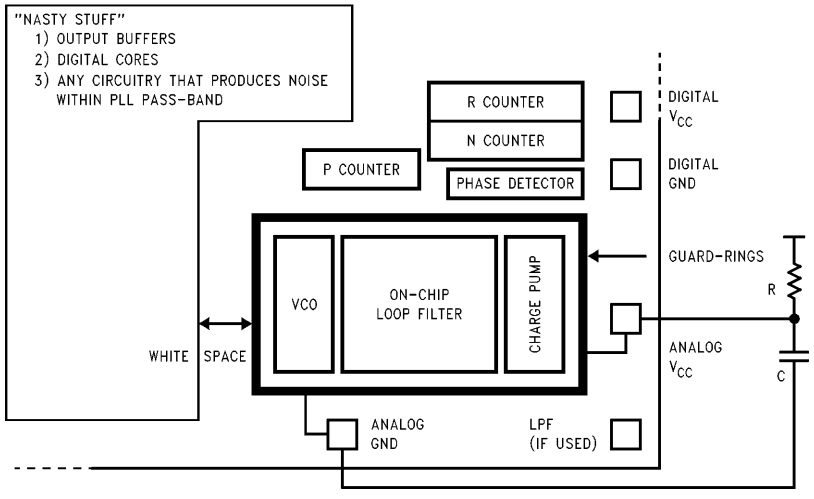

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FIGURE 15. Mixed-Signal Layout Techniques

Additionally, an off-chip analog supply filter can be used. The pole of the RC filter shown should be well below the cutoff frequency of the PLL. Keep in mind that the resistor will create a DC voltage offset which may limit its maximum value.

CONCLUSION

With strong core competencies in the mixed signal design area, and National's PLL Center of Excellence (providing synergy and sharing of PLL technology company wide), National is providing PLL-based solutions in a variety of applications.

The Clock Generation and Support (CGS) family product offerings include several PLL-based clock generators with tighter design and layout rules. These clock generators have extremely low skew and jitter. National's CGS product strategy is to develop devices to meet customer needs for high speed clock generation and support applications.

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