Controlling Low Probability "False Write" Data Corruption in Serial EEPROMs

National Semiconductor
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EEPROMs are useful because they are non-volatile memories that can be updated easily and quickly in a system without being physically removed. System designers working with early EEPROMs quickly learned that in addition to remembering data that they were asked to record, EEPROMs have the unique ability to ''record'' a history of unintended events experienced by the system. ''False-Write'' is such a common problem that virtually all types of EEPROMs have some type of accidental overwrite protection scheme.

Common false-write protection schemes are effective at controlling common and predictable problems, but EEPROMs are used in so many types of systems in so many environments that false-write data corruption is still a consideration for a systems designer. False-write problems are often so rare that they are frequently made visible only by field return statistics. Usually nothing can be found amiss with either the EEPROM or the system, other than the data in the EEPROM seems to be wrong. Functional test will typically reveal that both the EEPROM and the system are working flawlessly.

Designing a reliable system that includes an EEPROM, requires an awareness of common false-write problems, and an awareness of some subtle aspects of electronic systems environments. Basic problems are easily found and fixed at the design and debug stage. However, cut and try techniques can be an expensive way of eliminating low probability failures in the field.

COMMON FALSE-WRITE CAUSES

Other than defective software, and defective hardware timing design, there are three simple and common causes for malfunctioning digital circuits of all types. These are: V_{CC} glitches due to fast logic switching, etc., false power-on reset caused by temporary drops in V_{CC} due to motor start ups, etc., and low V_{CC} due to low batteries and other causes. These three can cause malfunctions in any digital system but are particularly dangerous for systems with EEPROMs. If a write operation occurs in an EEPROM as a result of any of these causes, reset alone cannot fix the problem. These three causes have equal probability of confusing either the EEPROM internal logic or the microcontroller attached to and controlling the EEPROM. Determining which component has triggered a false write problem is rarely practical.

In addition to the standard digital logic problems described above, EEPROMs have one unique avenue for data corruption, V_{CC} interruption during a write. Correct EEPROM operation assumes that V_{CC} rises monotonically at power up and stays in its specified range until after the last write event is complete. After a write operation has been requested, completion of the write requires as much as 10 ms. 10 ms is a very long time from the perspective of other digital components. A common microcontroller can execute 10,000 memory cycles in this time. If V_{CC} is shutdown in the 10 ms time period, the write operation may be incomplete, i.e. garbage will have been written. If a V_{CC} glitch occurs in this time period, the EEPROM logic may prematurely drop out of write mode, i.e. false reset, with the same result.

Since EEPROMs usually spend a only a tiny fraction of their lives actually writing or erasing data, the chance of having the power shut off during a write is usually small. Unfortunately this type of shutdown can create problems even if it occurs only one time in the life of a system. In practice many systems routinely provide dangerous V_{CC} dips and glitches. It is very rare to find false write problems without a nearby source of chronic noise, such as small motors, on board mechanical relays, etc. In battery powered systems, V_{CC} can be expected to fall out of specification repeatedly in the life of the device. Such events are harmless for most electronics but a hazard for systems with EEPROM. Even in non-battery powered systems, transient low voltage conditions should be anticipated in the life of any digital system.

COMMON FALSE-WRITE CONTROL SCHEMES

Serial EEPROMs are not susceptible to the most basic sources of false-write experienced by parallel EEPROMs. The control logic in serial EEPROMs powers up in a reset condition and can only be put into a write mode with a specific serial sequence enabling the write mode. Serial EEPROMs cannot be put into a write condition by the uncontrolled flailing of write or chip enable strobes during power up. Thus they do not need features such as V_{CC} sensitive write protect, and power on write delay which are standard features in most parallel EEPROMs. These basic power up write protection schemes are internal and invisible to the user in serial EEPROMs.

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Secondary false-write protection features for serial EEPROMs include write inhibit input pins and write zone protection schemes. Both of these features are included in Nationals ''NM93CSxx'' series of serial EEPROMs (see AN-716 and AN-871). Both of these techniques offer bullet proof false write protection in appropriate situations. Thus a concerned designer should first evaluate his system to see if these features can be used. **Determining NM93CSxx Family Applicability.**

The National ''NM93CSxx'' series EEPROMs have a flexible set of hardware write inhibit features that can eliminate the possibility of false write in many common serial EEPROM applications. The write inhibit input pins and write zone protection on the ''NM93CSxx'' series EEPROMs can be used in the following situations:

1. The EEPROM or a part of the EEPROM will be programmed one time only. Electronic serial numbers and date of manufacture codes are examples of this type of usage. National's ''CS'' series serial EEPROMs allow all or part of the EEPROM array to be permanently write protected.
2. The EEPROM will be reprogrammed only in the factory or when a user is present to enable the write operation with an external switch or jumper. A thermostat with a button to allow the temperature setting to be changed or an alarm clock a button to allow the alarm time to be changed are examples. National's ''CS'' series serial EEPROMs allow all or part of the EEPROM array to be protected except when new data actually must be entered. During reprogramming the write protection feature is disabled, to all or part of the array, via an external switch or jumper.

GENERAL PURPOSE FALSE WRITE CONTROL STRATEGIES

Electronic automobile odometers and electronic utility meters are examples of systems that do not fit into either of the above two categories allowing the use of ''CS'' series parts. Further, the use of an external push button as described in category number two above, may not be cost effective or may be impractical for other reasons. Designers working on these types of applications need to explore other techniques if false write is a problem.

LOGIC CONTROLLED SHUTDOWN

High quality portable electronics, such as cellular phones (and some personal computers) use logic controlled shutdown. One benefit of logic controlled shutdown is its ability to preserve the integrity of data being written to EEPROM or other nonvolatile memory (such as a hard disk). If a simple manual power switch is used to shut down the power supply abruptly, while data is being written, both data sets and individual data words, can be corrupted.

It is a somewhat simple task to provide enough power to allow one write operation to complete after the power is shut off (see Interrupt Isolated Power Supply below). This is adequate if the data set being written is contained in a single write word. However in general data sets are larger than one word and several words must be written successfully as a group to correctly update the data set in an EEPROM. ''Logic controlled shutdown'' is a technique that can be used to provide time for the system to write all the data required before shutting down the power supply.

To implement logic controlled shutdown, a logic controlled power switch, controls the power provided to the microprocessor system. A mechanical switch is provided which can turn the power relay on, but cannot be used to shut it off directly. A second switch that can be read by the microprocessor is provided for shutdown (possibly the same physical switch as the turn on switch). When the system is to be shut down, the shutdown switch position is sensed and, after all necessary write sequences are complete, the microprocessor system shuts itself off. Because microprocessor systems ''have been known'' to malfunction, an emergency shutdown switch is usually provided in case the software shutdown fails for any reason. Alternative emergency techniques include ''pulling the plug'' and ''taking out the batteries''.

POWER SUPERVISORS

Higher quality portable electronics, such as cellular phones, often use both logic controlled shutdown and power supervisors. National Semiconductor makes voltage regulators with integrated power supervisory provision that provide: voltage regulation, a low voltage indication, controlled fast power-up, and controlled fast power-down. These features can be used to create a well managed power environment for a microprocessor system. This greatly reduces the chance of accidental overwrite for an EEPROM in the system. These devices are particularly effective in managing battery powered systems. The LP2953 is a representative of this family, as shown in *Figure 3*. Datasheets can be found in the 1993 ''Power'ICs Databook'' or call National's Customer Response Center for the latest information and datasheets.

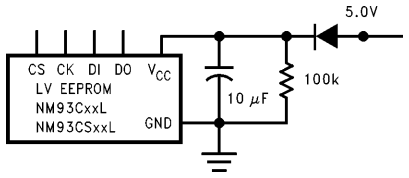

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FIGURE 1. V_{CC} Isolation Using a Diode, Capacitor and a National Semiconductor Low Voltage Serial EEPROM

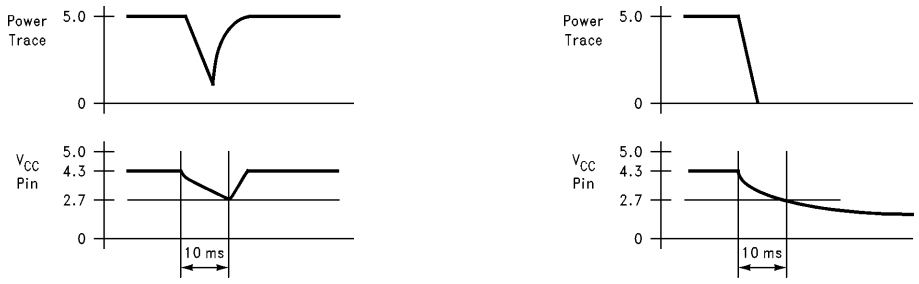

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FIGURE 2. Power Supply and V_{CC} Pin Waveforms, for a Short Dip in Power Supply Voltage, and Abrupt Power Supply Shut Off Using the Circuit Shown in *Figure 1.*

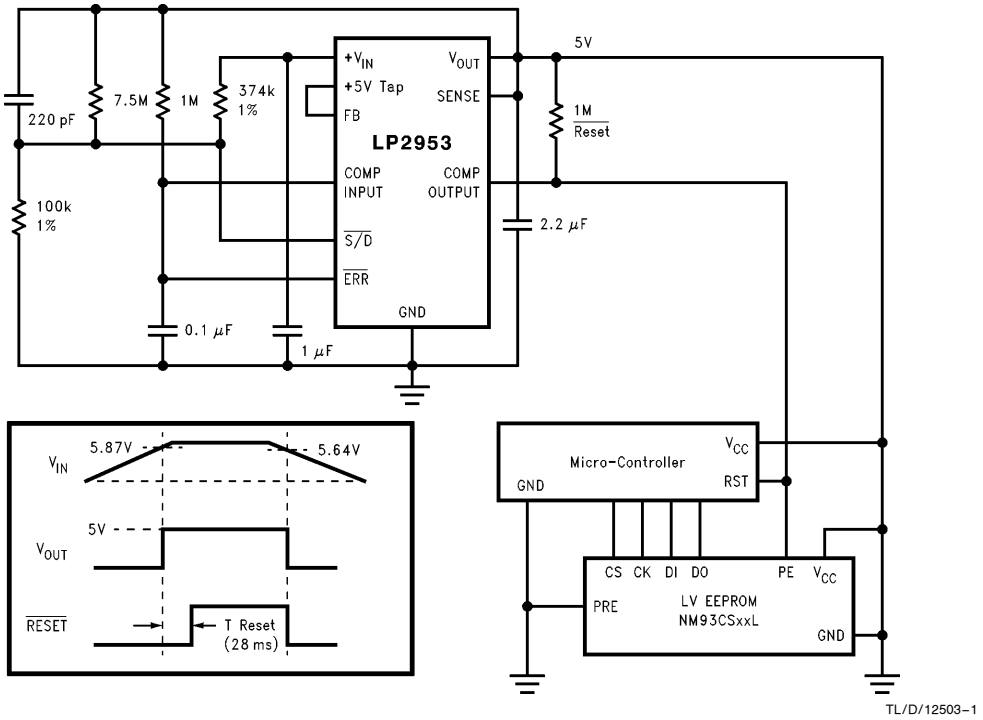

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FIGURE 3. The complete power supervisor. Voltage regulation, snap-on, snap-off 5V supply, microcontroller reset and EEPROM Program Enable (PE) signal generation via the National LP2953.

INTERRUPT ISOLATED POWER SUPPLY

Figure 1 shows a power supply isolation scheme that may be helpful in reducing susceptibility to write drop out caused by brief V_{CC} dips or V_{CC} dropping off at power down while a write operation is in progress. The capacitor can supply enough power to complete the write even if V_{CC} drops to 0V abruptly because the power has been shut off. Use of National's low voltage part in a 5V circuit provides adequate margin for the EEPROM to work even with the voltage drop created by a diode. Further, the EEPROM will work reliably until V_{CC} at the V_{CC} pin drops to 2.7V or lower (depending on which low voltage part is used).

The circuit shown in *Figure 1* can provide protection against short V_{CC} dips and abrupt power off events that happen to be coincident with write cycles. It will not be of benefit if the power dips are longer than 10 ms or the source of false write is a malfunctioning processor. It may be used in combination with a power supervisor.

It is assumed that when power to this circuit is removed, that it will stay off for several seconds. This allows the capacitor to discharge completely during power down. (This is generally true for EEPROMs in any case. Although "V_{CC} low time" is not specified in the datasheet it is assumed that V_{CC} will stay low for at least 2 seconds once it has come down below V_{CC} min. to affect a complete reset of internal circuitry.)

Since false write is normally a rare event, often detectable only as field return statistics, it may be desirable to provide for this type circuit on the production PC board even though it isn't expected to be used. The capacitor, diode, and resistor can be deleted in normal production and the diode can be replaced with a 0Ω resistor. If a problem is detected in the field, the circuit can be used as an aid in field diagnostics or as a field fix to the problem. This circuit is not a cure all, but it is a potential tool for a designer with a certain class of false write problem.

TRIPLE DATA REDUNDANCY

Writing the same data into three or more locations in a memory provides the simplest method of error detection and correction for small data sets. Since false write usually affects only data in one write word, triple word redundancy can also be used to recover data from some types of false write. In addition to allowing the correction of data corrupted by a false write event, it allows the detection of the hard single bit errors that are characteristic of endurance failure.

When data is written to the EEPROM, it is copied and written three times, on three separate write blocks. In the NM93C46 for example the write page width is 16 bits. When reading stored data, all three locations are read, and if any difference is found in one of the three bytes, the data in that byte is immediately overwritten with the data contalned in the other two locations.

False write normally occurs on data blocks the size of a normal write word width. The write word width for the NM93Cxx family is two bytes. Thus the smallest quantity that can be used on the 93C46 is 3 × 2 bytes = 6 bytes. i.e. writing redundant bytes into adjacent 8-bit addresses will not work since they are included on the same write word and both would be lost during a false write event.

Since three different words must be written each time data is changed with this system, care must be taken to prevent power down of the system until all three data words have been written. One way to assure this is logic controlled shutdown (see above). This can be used to preserve the integrity not only of individual write words but of entire strings and data sets.

Triple data redundancy is simple and effective for small data sets. It in addition to allowing the correction of data corrupted by a false write event, it allows the detection of the hard single bit errors that are characteristic of endurance failure. Once a chronic hard endurance error is detected, the data set can be moved to an new unused EEPROM location.

SUMMARY

False write is usually a rarefied data corruption problem common to all EEPROMs. There are simple hardware solutions for some classes of false write. The features of National's NM93CSxx EEPROMs are completely effective false write control for some types of applications. Power supervisory circuits can be effective to control false write in other types of systems. Software only error correction approaches exist that may be cost effective in other classes of systems. Hundreds of millions of EEPROMs are installed in electronic systems each year. False write events create problems for only a small number of these systems. However, EEPROMs are used in such a wide variety of systems, that the need for false write control measures should always be considered during the design of a new system.

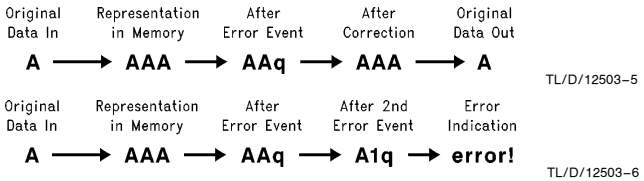
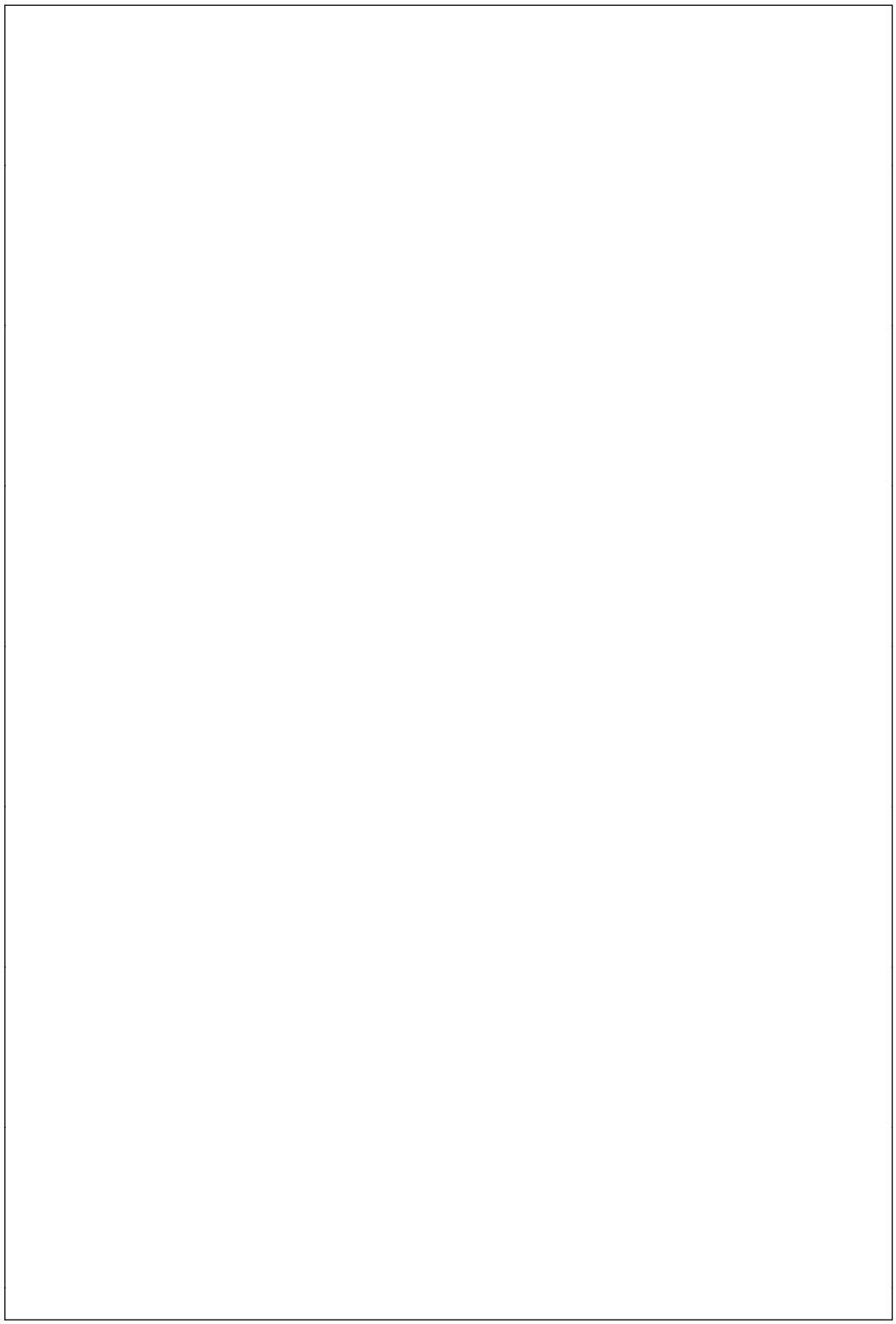


FIGURE 4. Single Word Error Correction and Double Word Error Detection with Triple Word Redundancy



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