EEPROM Endurance Prediction

National Semiconductor
Application Note 1009
Robert Stodieck
September 1995

ENDURANCE

The number of write/erase cycles an EEPROM can withstand before a bit in the memory fails.

RETENTION

The length of time an EEPROM can reliably retain data after programming.

There are no formal industry standards for determining the techniques or the parameters of endurance claims found in datasheets. The datasheet claims of different manufacturers for the endurance of the same product would vary by factors in excess of ten. To make sense of endurance claims requires a little background knowledge on endurance testing, EEPROM failure characteristics, and a look at the qualification data for the EEPROM type in question. (A copy of the qualification data packet for the EEPROM family of your choice can be obtained with a call to Nationals customer response center.)

In a large fraction of the applications for EEPROM, the write-erase endurance limits of these devices are never even approximated. In others, endurance is the key equation determining the practicality and the economics of EEPROM usage. By understanding the endurance characteristics of EEPROMs, designers can both lower the cost and improve the reliability of their systems.

Manufacturers typically claim endurance levels of 10,000 to 1,000,000 cycles. The meaning of such claims is quickly obscured when a designer is faced with predicting the endurance of such a part in a real system. The system may have never have existed before and the usage statistics may not be well known. If usage statistics are well characterized, there is still mystery in translating the meaning of manufacturers claims in relation to a given usage pattern. It is the purpose of this applications note to illuminate these issues for the designer as much as possible.

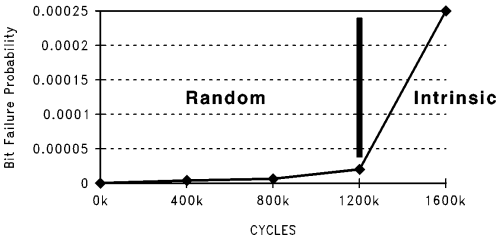
WHAT DOES AN ENDURANCE CLAIM OF 1,000,000 CYCLES MEAN?

National Semiconductor products are normally guaranteed for 1 million cycles. This means that the ''intrinsic'' failure mode of National EEPROMs begins after 1 million cycles. *Figure 1a* and *1b* shows averaged cumulative endurance bit failure statistics for 2,700 EEPROM samples taken from each of 27 production die runs of the NM93C46N serial EEPROM (100 samples from each run).

National currently uses two different EEPROM architectures. Products based on the CS160 process use a unique direct write memory cell. No pre-erase cycle is ever required when writing to these devices. With these devices all bits in the memory are erased (to ''1'') and then written (to ''0'') to count as one endurance cycle. On products based on CS100 technology, a pre-erase cycle is required but the memory cells are automatically erased prior to being written. The erase cycle is transparent to the programmer. Thus a write of ''0'' data to the memory constitutes an endurance cycle. (By convention, National EEPROM cells are in the ''erased'' state when they indicate ''1'' data and written when they indicate ''0''.)

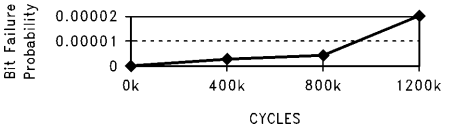
A common definition of ''failure'' is the failure of a single bit in one memory chip. In the case of the NM93C46, a one bit failure in a 1k bit memory. (Note that by this criterion 100% failure could mean that only one bit in each memory has failed. i.e., only one bit in 1000 has failed.) At National, cycling is done at room temperature, failures are limited to 2% at the 1 million cycle level. National EEPROMs are guaranteed 10 years for data retention. Since it is not practical to wait for 10 years to run production tests, the parts are baked after cycling, at 150°C for two hours, to accelerate leakage prior to testing for failures.

As can be seen in *Figure 1a,* at cycle counts below about 1 million cycles, the failure level is non-zero but very low. Well after 1 million cycles, the failure rate increases rapidly. Failures in the post 1 million cycle region are called ''intrinsic'' failures. Failures at lower cycle counts are ''random'' failures. While the onset of intrinsic failures clearly delineates the end of useful life of an EEPROM, the end of useful life must be declared somewhere before the EEPROM is cycled into this region. The ambiguity of exactly where to draw the line creates some of the large differences in the claims of different makers.



TL/D/12504–1

FIGURE 1a. Averaged Endurance Bit Failure Probabilities for 27 Production Die Runs



TL/D/12504–2

FIGURE 1b. Averaged Endurance Bit Failure Probabilities at Less Than 1.2 Million Cycles

©1995 National Semiconductor Corporation RRD-B30M115/Printed in U. S. A.

FOCUS ON NON-INTRINSIC FAILURES

The accumulation of failures in the random area is approximately linear. 100 samples are taken from each die run and tested to failure. A vendor who quotes endurance at 100k cycles because there are typically no failures observed at all in 100 piece lots at 100k cycles, risks misleading a designer. Failures below 100,000 cycles are not non-existent, nor are failures at above 100,000 cycles common. Failures below a few hundred thousand cycles are simply below the threshold of the screening procedure, and actually failure probabilities increase more or less linearly from cycle one to cycles one million plus, where a real increase in failure rates does occur. A customer who is looking only at endurance claims may have a false impression that he needs a different product and may in fact end up buying an inferior product. The designer must bypass the endurance claims and proceed to the qualification data for better information.

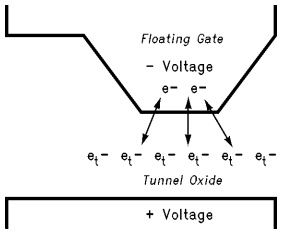
If required, in the area of random failures, simple error detection and correction schemes maybe used such as writing triply redundant data fields or using an error correction code. In the intrinsic failure region, practical error correction techniques are quickly overwhelmed. The only way of extending the number of times a data field may be rewritten, past the intrinsic limit, is to relocate the location of the data field on schedule, before the intrinsic cycling limit is achieved. National Semiconductor rejects all die run lots if there are any simultaneous multiple bit failures. Failures of this type indicate failure in the peripheral logic, not in the EEPROM cells. This guarantees that any errors that occur due to endurance cycling are isolated one bit failures. Single bit failures are correctable or at least detectable with elementary software based error detection and correction techniques.

Oddly enough elementary bit error statistics do not track across different densities of product even though the manufacturing process is the same. A 2k bit memory is not twice as likely to have a bit fail as a 1k bit memory at 1 million cycles. The test statistics for each memory type and density and process technology must be consulted individually.

WHAT CAUSES ENDURANCE FAILURE?

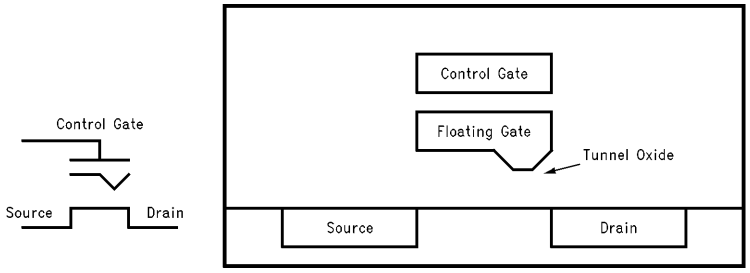
Figure 2 shows a schematic and a cross section representation of an EEPROM cell. During programming the control gate is made positive relative to the source-drain area. The floating gate is capacitively coupled to the control gate, and when sufficient voltage is generated, and the tunneling threshold is exceeded, electrons tunnel through the thin ''tunnel'' oxide window into the floating gate. This negative charge then remains trapped in the floating gate since inadequate voltage exists, normally to allow the electrons to tunnel back out. To erase the cell the process is simply reversed. To read the cell, the control gate, and source, are brought to predetermined reference voltages and the current through the cell is measured. The transistor of a programmed cell is ''on'' and the transistor of an erased cell is ''off''.

Two basic types of failure occur when EEPROM cells are repeatedly written and erased: dielectric failure, and charge trapping. Dielectric failures are the source of the very low level random failures that were discussed above. They are caused by leakage through minor unscreenable flaws in the tunnel oxide. On contemporary production EEPROMs dielectric failures are typically too rare to be noticed by standard lot sampling techniques until several 100 thousand write-erase cycles. After this they create a very low but visible level of random bit failures.



TL/D/12504–4

FIGURE 3. Negative Charge, Trapped in the Tunnel Oxide due to Write-Erase Cycling, Created a Potential Barrier to the Flow of Electrons Raising the Apparent Tunneling Voltage.



TL/D/12504–3

FIGURE 2. A EEPROM Cell Schematic and Idealized Cross Section of an EEPROM Cell

Charge trapping is the effect that creates intrinsic failure in EEPROMs. During write-erase cycling, small amounts of isolated negative and positive charge become trapped in imperfections in the tunnel oxide. Once trapped, the charge is no longer free to tunnel out of the oxide. In practice electrons are more commonly trapped, and their presence creates a barrier to the tunneling of other electrons through the tunnel oxide. The apparent voltage needed to tunnel in either direction through the oxide increases. This reduces the amount of charge that can be moved in and out of the floating gate. When the accumulation of trapped charge becomes severe enough it is no longer possible to move enough charge to clearly distinguish a one from a zero. (The presence of trapped electrons also permanently shifts the threshold voltage of the cells transistor somewhat.) At this point the memory cells involved must be abandoned.

It is desirable to be able program EEPROMs as fast as possible. However accelerating the programming of EEPROM cells can only be achieved by using higher programming voltages. It turns out that using high voltages accelerates the charge trapping mechanism and generally degrades the endurance of the EEPROM. Thus programming speed, and endurance are trade offs.

DATA RETENTION AND ENDURANCE

It might seem intuitive that tunnel oxide might degrade with endurance cycling and that data retention would suffer as a result. But the effect of cycling on the retention characteristics of EEPROM memory is very slight. That that does occur is not due to increasing leakage through normal tunnel oxide, but the statistical influence of the random failures which are in fact caused by leakage through rarefied defects. The effect of cycling on the retention characteristics of before reaching the intrinsic limit of EEPROM memories is so slight, in fact, that it is usually ignored.

SUMMARY

EEPROMs are nearly perfect memorys in the sense that they retain data of long periods of time with no power. They are less than perfect in that they have a finite ability to survive data changes and write speeds are limited. The end of useful life of an EEPROM is a slow process without clear indicators of failure. The end of reliable operation must be estimated by the designer and, if it is likely to be approached in service, must be compensated for by the designer. Both the techniques of wear leveling, i.e., moving data sets to distribute cycling wear, and error correction techniques may be used.

The meaning of different manufacturers endurance claims must be treated with caution. The designer must understand the basic endurance characteristics of EEPROMs to intelligently design with them and the designer must have real data to evaluate. National sales offices have full qualification data available for all National EEPROMs.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.