100BASE-TX Unmanaged Repeater Design Recommendations

National Semiconductor
Application Note 1010
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1.0 INTRODUCTION

This application note provides the information necessary to design an unmanaged 12-port 100BASE-TX repeater based on National Semiconductor's DP83850, DP83840, and DP83223 integrated circuits. The DP83850 is a full featured Repeater Interface Controller (RIC™) capable of supporting up to 12 100BASE-X ports. The DP83840 PHY device with the DP83223 twisted pair transceiver combine to provide the 100BASE-TX compliant Physical Layer and Physical Medium Dependent sublayer.

A design based on these three devices allows for a simple, low cost 12-port 100 Mb/s repeater solution.

While considerations such as Auto-Negotiation and 10/100 Mb/s operation are noted herein, detailed emphasis is placed on the fundamental design requirements, from the MDI (Medium Dependent Interface) to the MII (Medium Independent Interface), for an unmanaged 100BASE-TX repeater. System design aspects such as interconnection, clock distribution and physical layout are provided.

It is recommended that this application note be reviewed in conjunction with the latest version datasheets for the DP83850, DP83840, and DP83223 devices.

2.0 OVERVIEW

The block diagram in *Figure 1* illustrates the interconnection and layout for a 12-port 100BASE-TX repeater. Although the basic functionality of a 100BASE-TX repeater is similar to that of a 10BASE-T repeater, there are some important differences. These differences include data rate, signal encoding/decoding, and link integrity verification.

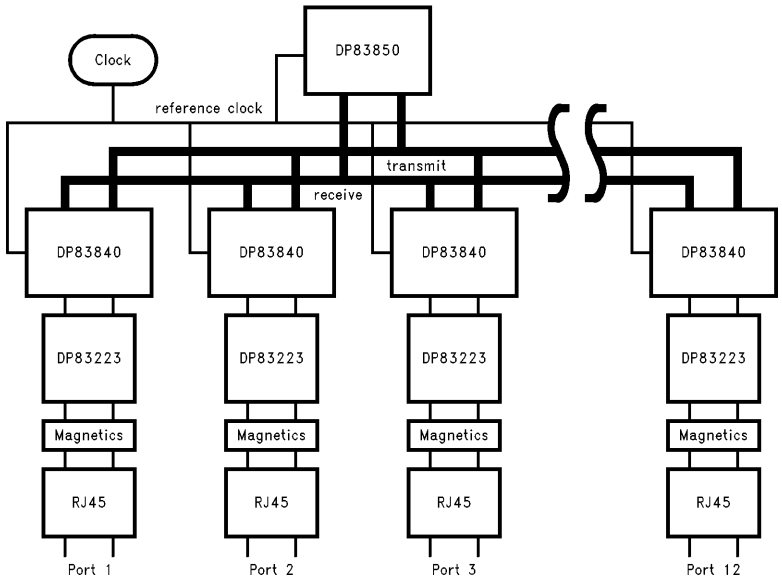

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FIGURE 1. 100BASE-TX Repeater

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10BASE-T data packets are transmitted as 2.5 Vpk Manchester encoded data at 10 Mb/s. 10BASE-T Link pulses are transmitted between data packets to ensure link integrity to the receiving station.

For 100BASE-TX transmission, which borrows from the ANSI X3T12 FDDI TP-PMD specification, packets are imbedded in a continuously scrambled 1 Vpk MLT-3 encoded datastream at an effective data rate of 100 Mb/s. Link integrity for 100BASE-TX is monitored via a Signal Detect function in conjunction with the synchronization status of the receive descrambler.

The majority of CSMA/CD operations remain unchanged between 10BASE-T and 100BASE-TX. Refer to the appropriate IEEE 802.3 specifications for further information.

A detailed review of this design is divided between the repeater's receive and transmit operations. Receive operations include all signaling from the RJ45 media connector to the DP83850 RIC device. Transmit operations include all signaling from the DP83850 RIC to the RJ45 media connector. Sections covering clock distribution and system layout issues are also included.

The 100BASE-TX transmit and receive operations are divided into four basic categories:

- Physical Medium Dependent (PMD)—DP83223
  The PMD sublayer section consists of the RJ45-8 media connector, an isolation transformer (magnetics), the DP83223 TWISTER™ transceiver, and the associated interconnections.
- Physical Layer (PHY)—DP83840
  The Physical Layer section consists of the DP83840 100BASE-X PHY device and associated support components.
- Medium Independent Interface (MII)
  The Medium Independent Interface section consists of receive signal timing parameters and special considerations.
- Repeater Controller—DP83850
  The Repeater Controller section describes the fundamental operations of the DP83850 100RIC device.

3.0 PMD

This section describes the receive and transmit signal paths between the twisted pair cable and the DP83840 Physical Layer device. The PMD design suggestion given in *Figure 2* should be implemented for each port in a multi-port 100BASE-TX repeater design.

The schematic in *Figure 2* provides electrical interconnection detail for a 100BASE-TX Physical Medium Dependent (PMD) circuit based primarily on the DP83223 TWISTER. Contact National Semiconductor for information regarding magnetics recommendations.

3.1 PMD Receive

The receive datastream is coupled from the twisted pair cable to the 100BASE-TX repeater port via pins 1 and 2 of the RJ45-8 media connector. The datastream is AC coupled from the RJ45-8 to the DP83223 twisted pair receiver by an isolation transformer. The DP83223 then equalizes the receive signal to compensate for signal degradation caused by the non-ideal transmission line properties of the twisted pair cable. The DP83223 then translates the equalized receive bit stream from MLT-3 to binary and outputs it to the Physical Layer as a Pseudo-ECL (PECL) logic level signal.

Additionally, upon reception of an appropriate input signal, the DP83223 generates a Signal Detect signal which indicates to the DP83840 Physical Layer device that a potentially valid 100BASE-TX signal is present.

3.2 PMD Transmit

The transmit datastream, as sourced by the DP83840 100BASE-X Physical Layer device, is a scrambled NRZI differential PECL signal that is directly connected to the DP83223 twisted pair transceiver device. The DP83223 translates the PECL signal into an MLT-3 encoded signal which is output to the magnetics as a current sourced differential datastream. The signal is AC coupled via the magnetics, to pins 3 and 6 of the RJ45-8 media connector where it is finally coupled to the twisted pair cable.

3.3 PMD Magnetics

The Magnetics Detail diagram given in *Figure 3* provides the required interconnection for the magnetics module within the PMD circuit. Magnetics modules suitable for use with the design outlined herein are available from Pulse Engineering (part# PE68515) and Valor Electronics (part# PT4171). National Semiconductor continues to qualify additional magnetics from various manufacturers. Please contact National Semiconductor for a current list of magnetics qualified for this design.

The schematic given in *Figure 2* does not include the common magnetics circuit as specified by National Semiconductor. This circuit is required to allow full support of Auto-Negotiation. Contact National Semiconductor for further information regarding the common magnetics application and NWay Auto-Negotiation.

The common mode termination circuit included in *Figure 3* suggests one method for decreasing impulse noise sensitivities as well as helping to control EMI radiated emissions.

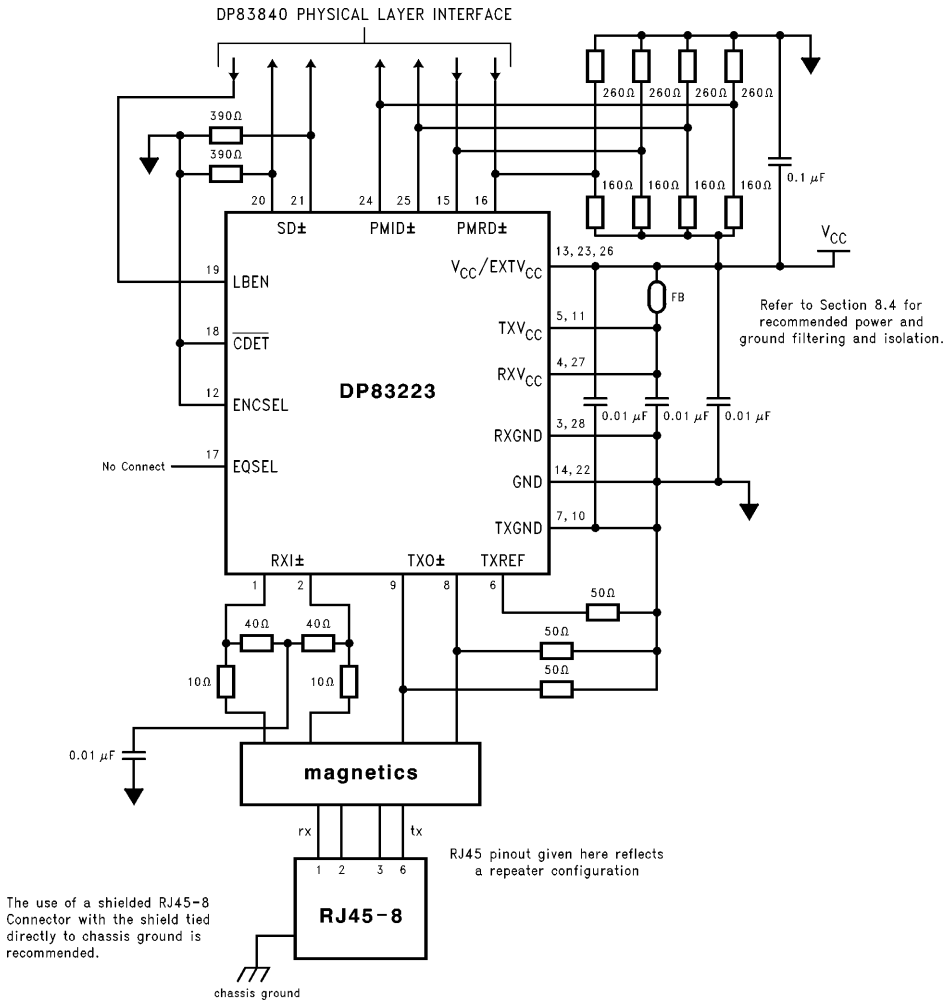

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FIGURE 2. 100BASE-TX PMD

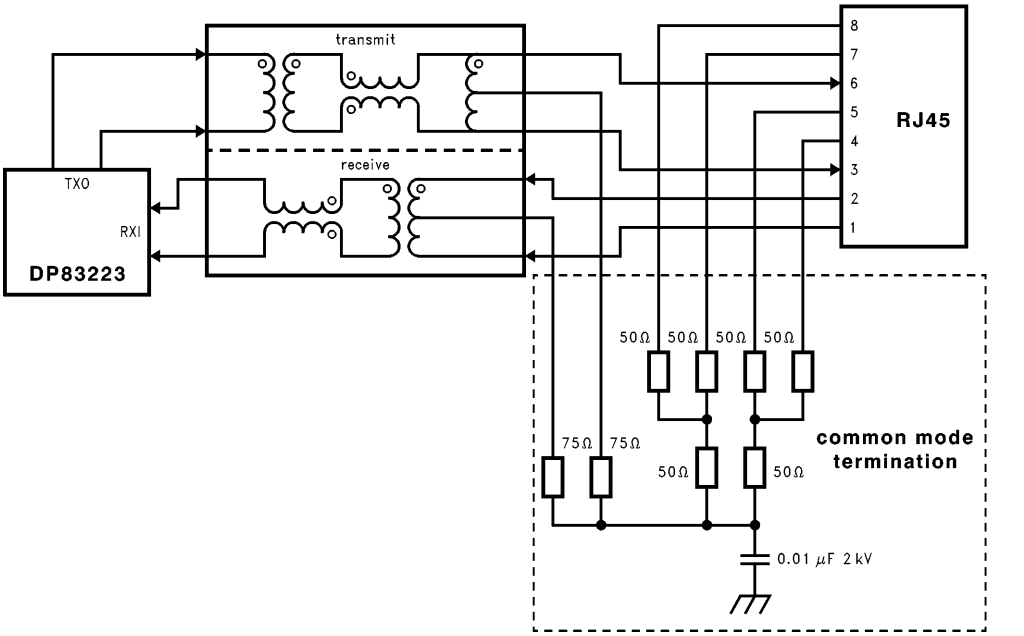

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FIGURE 3. PDM Magnetics

4.0 PHY

The DP83840 100BASE-X Physical Layer device incorporates many of the functions required for compliant 100BASE-TX signaling. A connection diagram for the DP83840 is provided in *Figure 4*.

4.1 PHY Receive

The flow diagram in *Figure 5* illustrates the functional blocks within the DP83840 100BASE-X receive channel.

The Physical Layer receive operation begins at the RD± and SD± inputs of the DP83840. These scrambled PECL signals, as generated by the DP83223 twisted pair receive circuit, are first routed to the integrated 125 MHz clock recovery module which extracts the receive system clock from the asynchronous receive datastream.

The receive data is subsequently converted from serial to 5-bit parallel and routed through the NRZI/NRZ decoder, the descrambler, symbol alignment, and finally the 4B/5B decoder. The nibble wide data is then routed to the MII receive bus outputs RXD[3:0] of the DP83840 where it is accompanied by a synchronous 25 MHz RX_CLK. Although all of these receive functions can be bypassed, this datastream ''conditioning'' is required because the DP83850 Repeater Controller IC employs a nibble wide interface.

4.2 PHY Transmit

The flow diagram in *Figure 6* illustrates the functional blocks within the DP83840 100BASE-X transmit channel.

The Physical Layer transmit operation begins at the transmit MII inputs TXD[3:0] of the DP83840. This nibble wide data, as sourced by the DP83850 Repeater Controller, is first block encoded to 5B symbol wide data, scrambled, and finally post encoded to NRZI format where it is then serialized and routed, MSB first, to the TD± outputs of the DP83840. All of these functions are synchronous relative to the internal clock generation module. The 25 MHz reference is used for all of the parallel data functions and a 125 MHz clock is used to serialize and clock out the scrambled datastream.

4.3 PHY Addressing and Serial Management

An unmanaged repeater does not normally require that each of its ports be individually addressed. However, the unique properties of the DP83840 device allow the system designer to benefit from PHY address assignment.

The DP83840 is designed such that the starting value of the transmit scrambler is dependent on the PHY address assigned. This ensures that any number of uniquely addressed DP83840 devices will not be transmitting identical datastreams simultaneously during a transmit operation. Each PHY will be transmitting the same encoded data but at a different scrambled state. This will help to reduce potential EMI radiation problems that may have otherwise resulted from as many as eleven ports simultaneously transmitting the exact same scrambled datastream.

The other benefit to including unique PHY addressing within the 100BASE-TX repeater design is to allow for easy conversion of an unmanaged design to a managed design. While this application note does not focus on the aspects of a managed repeater, a basic understanding of the MII serial management is provided.

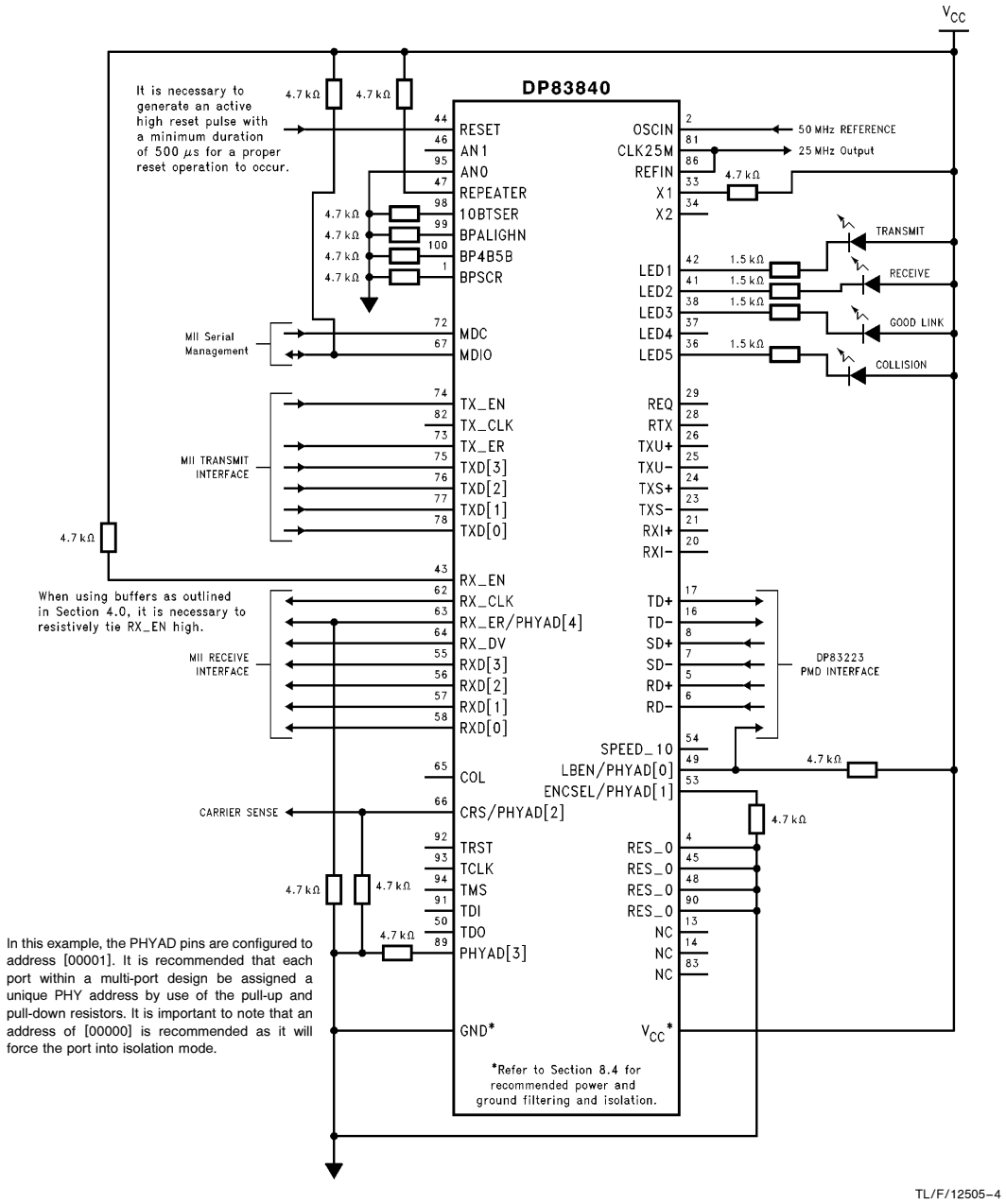

FIGURE 4. DP83840 Connection Diagram

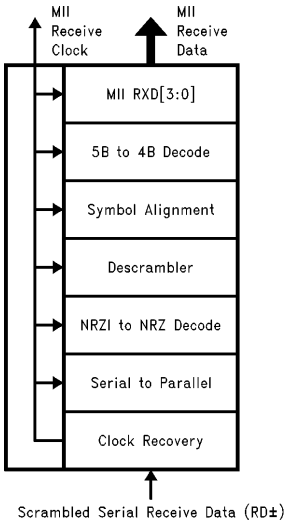

FIGURE 5. PHY Receive Channel

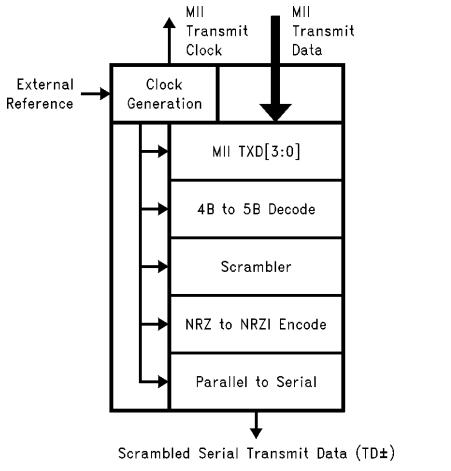

FIGURE 6. PHY Transmit Channel

PHY address assignment is necessary in a managed multiport repeater to allow the managing agent to uniquely identify any given port. Given an address, the managing agent can perform read and write operations through the serial access port as defined in Chapter 22 of the IEEE 802.3μ/D5 100BASE-T document. This access allows for both statistical gathering and port configuration through read and write operations to the PHY registers.

The address of the DP83840 device is set upon power up or reset and is defined by the pull-up or pull-down state at each of the PHYAD pins, PHYAD [4:0]. Assigning a PHY address of [00000] for any given PHY is not recommended as this will force the port into PHY isolation mode which will disable all transmit and receive activity at that port. For a 12-port repeater, assigning PHY addresses of one through twelve ([00001] through [01100] binary) is recommended.

4.4 PHY Clocking

The DP83840 is capable of operation at either 10 Mb/s (10BASE-T) or 100 Mb/s (100BASE-X). Because of this flexibility, a variety of clocking options exist for the DP83840. In the case of a 100BASE-TX application that does not support NWay Auto-Negotiation, the only external clock required is a 25 MHz reference. The DP83840 uses this reference to generate phase locked 25 MHz and 125 MHz to provide the clocks necessary for the 100-BASE-X transmit functionality.

Clock reference generation and distribution are covered in Section 7.0

5.0 MII

The Medium Independent Interface consists of three basic components. The Serial Management operation (which was briefly covered in Section 4.3), the receive operation and the transmit operation. Both the receive and transmit interfaces are based on a nibble wide data bus running at 25 MHz allowing a transfer rate of 100 Mb/s.

While the fundamental aspects of MII operation are included herein, a detailed operational description can be found in Chapter 22 of the latest IEEE 802.3μ specification for 100BASE-T Ethernet protocols.

5.1 MII Receive Operation

The Medium Independent Interface receive operation is a synchronous nibble wide data transfer from the DP83840 Physical Layer to the DP83850 Repeater Controller. This data transfer is initiated when the DP83840 asserts its CRS (Carrier Sense) output which indicates that data reception is in progress. With the REPEATER pin tied high, as shown in *Figure 4*, the DP83840 will only assert CRS during a receive event to ensure proper interoperation with the DP83850 device. The CRS output of the DP83840 is asynchronous to the RX__CLK output.

Upon reception of the CRS signal from an active port, the DP83850 will assert the corresponding RX__EN (Receive Enable) signal. This enables the RX__CLK, RX__ER, RX__DV, and RXD[3:0] outputs of the DP83840 to become active. These outputs are normally TRI-STATE when the RX__EN input is not asserted.

The relative timing of the MII receive signals is dependent on the quality of the receive operation. There are primarily three different receive scenarios which represent:

- Reception without error(s)
- Reception with error(s)
- False carrier Indication

These scenarios are illustrated by the timing diagrams in *Figures 7*, *8* and *9* respectively.

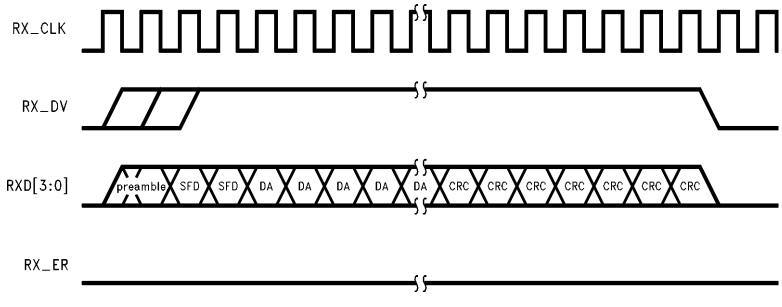

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FIGURE 7. MII Reception without Error(s)

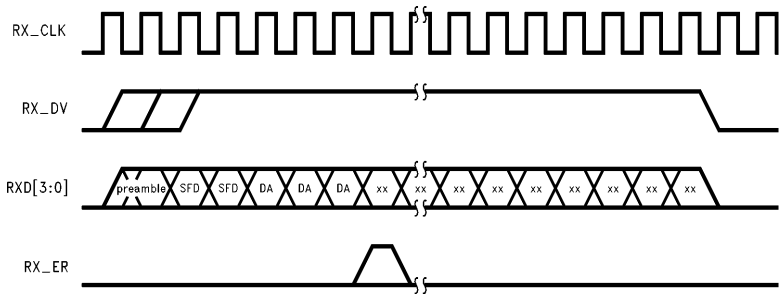

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FIGURE 8. MII Reception with Error(s)

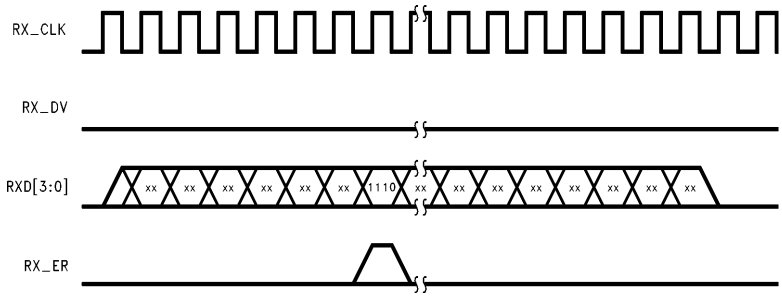

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FIGURE 9. False Carrier Indication

The relative timing for ''reception without error(s)'' illustrates the desired sequence of events which occur during reception. Upon the reception of a packet, the DP83840 asserts its CRS output signal. The DP83850 then responds by asserting its RX__EN output signal. Upon reception of the RX__EN signal, the DP83840 activates each of its MII receive outputs. RX__CLK will first begin to run at 25 MHz. RX__CLK will then begin clocking out the nibble wide data RXD[3:0]. Coincident with the preamble on RXD[3:0], RX__DV (data valid) will assert and remain so for the duration of the receive packet transmission to the DP83850. RX__DV will deassert immediately following the final data nibble. RX__ER remains low for the duration of the packet indicating an error free packet.

The relative timing for ''reception with error(s)'' is similar to the previous case except that the RX__ER signal is asserted during the packet reception operation. This indicates that the DP83840 Physical Layer device has detected some form of data error during reception. Errors resulting from improper frame alignment can cause assertion of RX__ER.

The third scenario, ''false carrier indication'', is an indication that the DP83840 detected invalid data code groups which proceeded the starting delimiter of the packet. Additionally, ''false carrier indication'' will occur upon detection of an invalid stream termination sequence.

For further detail regarding these MII data reception scenarios, refer to the latest version of the IEEE 802.3μ specification for 100 Mb/s Ethernet protocols.

5.2 MII Receive Physical Connection

The DP83850 Repeater Controller device is capable of supporting up to twelve DP83840 Physical Layer devices in conjunction with as many DP83223 transceiver devices. In a fully loaded architecture, where all twelve ports are designed in, there are special considerations regarding the physical layout of the MII receive interface.

5.2.1 MII Receive Bus Considerations

Due to the nature of the Ethernet Repeater architecture, where one repeater controller receives data from as many as twelve separate Physical Layers, each of the Physical Layer devices must share a common receive data bus. This bus terminates at the receive inputs of the repeater controller.

Specifically, twelve DP83840 devices share a single receive data bus for data transfers to the DP83850 Repeater Controller. The operation of the repeater configuration allows only one DP83840 MII receive output to be active at any given time. All inactive DP83840 devices TRI-STATE their MII receive data outputs. Theoretically, this would allow the single active DP83840 to transfer the receive packet to the DP83850 without interaction with the remaining inactive DP83840 devices. In practice, however, the DP83840 must not only drive the signal traces between itself and the inputs of the DP83850, but also the entire common data bus with all of the inherent distributed capacitance and trace routing aberrations.

The distributed trace capacitance, in addition to the capacitance of the TRI-STATE outputs of the inactive DP83840s can total to 150 pF or higher. This distributed capacitive load can cause waveform anomalies and reduce the signal integrity within the MII receive interface. The RXD[3:0], RX__DV, and RX__ER outputs of the DP83840 are all subject to this additional capacitive loading.

5.2.2 MII Receive Buffering

To significantly reduce the effects of the distributed capacitive loading, an octal buffer can be placed between each DP83840 and the DP83850 Repeater Controller device. Octal buffers such as the National Semiconductor ABT541 provide significant output current drive capability which effectively improves the signal integrity to help ensure robust MII receive data transfer.

While the DP83840 provides sufficient MII receive clock-to-data setup and hold times for the DP83850, this timing relationship can be optimized by utilizing a latch at the input of the DP83850 to re-time the data relative to the RX__CLK. Additionally, the use of an inverter for the RX__CLK will ensure virtually ideal set and hold timing for the DP83850 MII receive inputs. While issues such as repeater cascading (often referred to as stacking) are not specifically covered in this application note, it is important to understand that the inclusion of the latch and inverter as described herein is critical to ensure robust operation of a multi-repeater cascaded system.

Figure 10 provides the suggested interconnection for the receive MII (CRS is also shown) of a twelve port repeater design. This design approach includes recommendations for buffering, latching, and general component placement guidelines to help ensure robust interface performance.

The use of the ABT541 octal buffers requires that an active low $\overline{OE}$ signal be generated so that the active receive port can source its data to the DP83850. As illustrated in *Figure 10*, by inverting the RXE bus and connecting the inverted RXE signals to the appropriate ABT541 octal buffers, the active Receive MII data and clock is enabled. Since no more than one ABT541 octal buffer can be asserted at any given time, the remaining disabled ABT541 devices will TRI-STATE which eliminates contention on the shared bus.

The RX__EN inputs to the DP83840 devices should be tied high such that they are never allowed to TRI-STATE. The ABT541 buffers will perform the necessary bus TRI-STATE in place of the DP83840 devices. There are important design recommendations which, if incorporated, will help to ensure proper interface operation.

When a given design requires that multiple signal sources share a common bus with a single destination, it is difficult to maintain good signal transmission properties. The best way to reduce signal reflection anomalies in such a shared bus configuration is to minimize the signal trace lengths. By placing the ABT541 octal buffers and the ABT574 latch as close as possible to the DP83850, the area of shared signal routing for RXD[3:0], RX__DV, RX__ER, and RX__CLK is minimized. Allowing longer trace lengths from each of the DP83840 PHY devices to their respective ABT541 buffers is acceptable because each PHY now has only a fan-out of one (individual ABT541 input) per signal trace. Since the RXE and CRS signals, between the DP83850 and the DP83840s, are each routed separately (not a shared bus) good signal integrity is easier to achieve but not guaranteed. Noise coupling onto these lines can cause improper operation and must be considered during board layout. As with any relatively high speed design, it is helpful to minimize signal trace lengths and minimize crosstalk wherever possible.

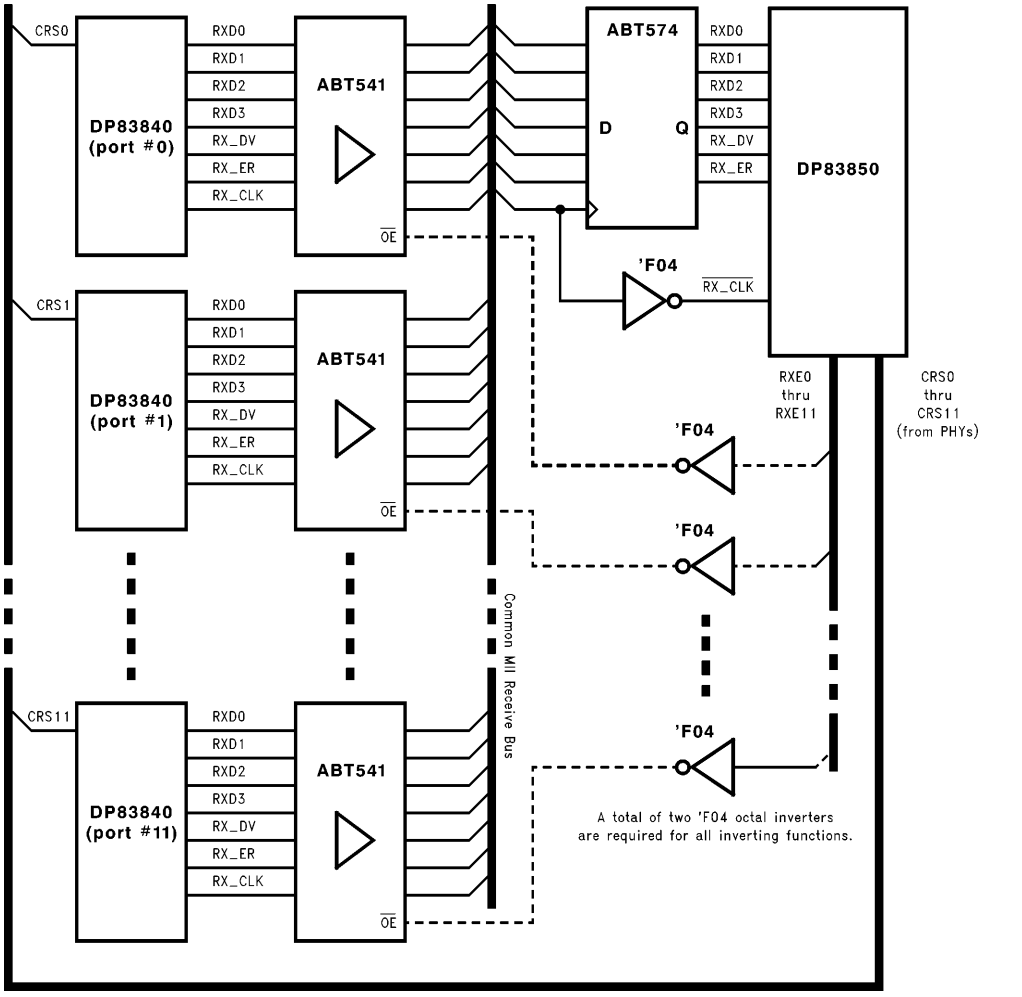

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FIGURE 10. MII Receive Connection Recommendation

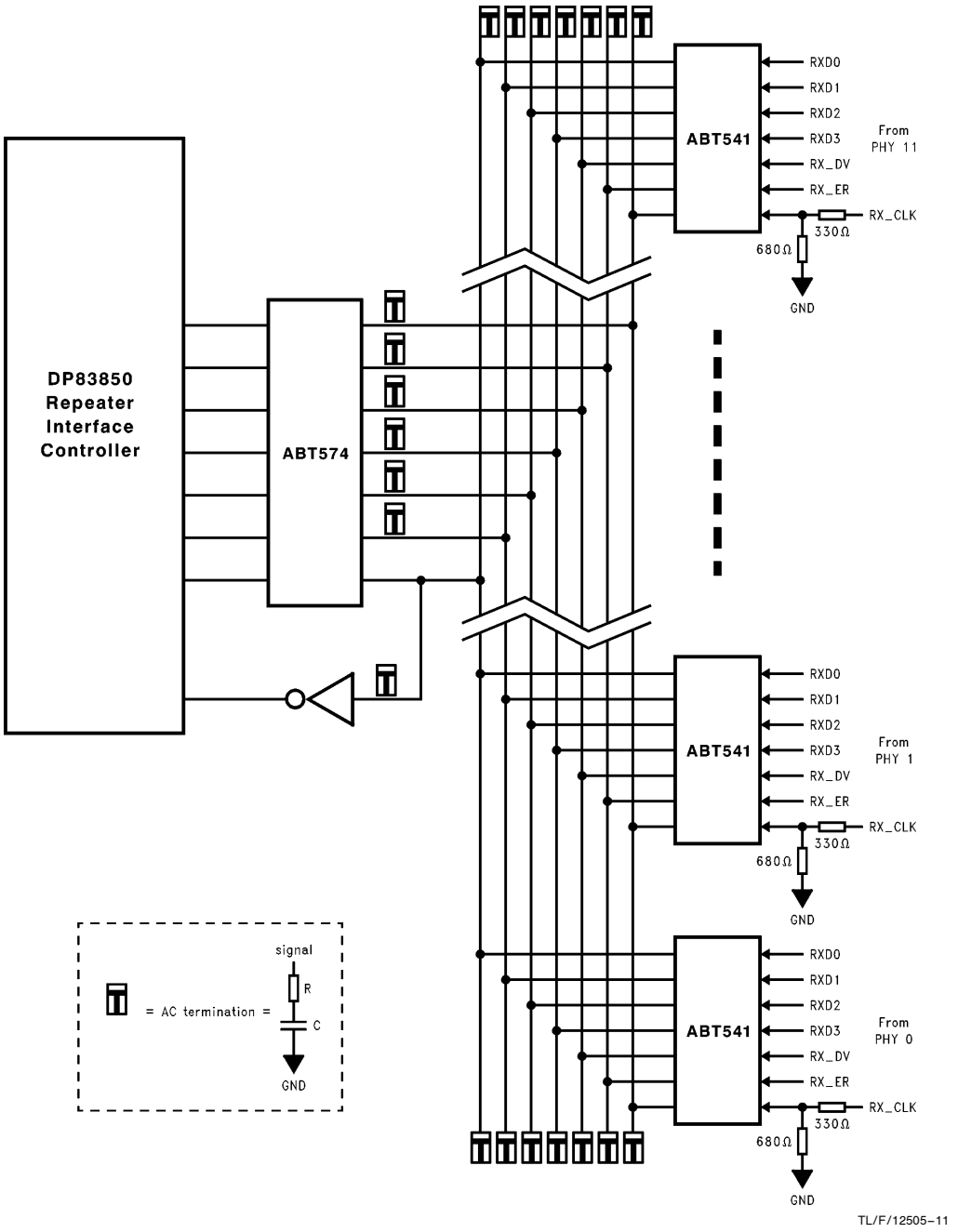

FIGURE 11. MII Receive BUS Termination

5.2.3 MII Receive Bus Terminations

The use of bus terminations may also be implemented in an effort to control signal integrity on the common MII bus. The option for AC terminators at both ends of the bus, as well as at the inputs to the DP83850 device, should be incorporated into the design as illustrated in *Figure 11*. By populating some combination of these AC termination components and by experimenting with the component values, the signal aberrations inherent to a given common bus layout may at least be partially compensated. A standard AC termination consisting of a series resistor and capacitor to ground should be used. Component values of 50 pF and 100Ω are good typical values to begin the empirical experimentation of finding the best possible AC termination values for a given layout design.

Placing AC terminations at each CRS input to the DP83850 as well as at the OE inputs ($\overline{RXE}$) of the ABT541 buffers will help to minimize signal aberrations on these traces as well as reduce noise that may couple from these traces onto other signals.

Another concern is the potential for duty cycle distortion of the RX__CLK signals. This can occur due to the fact that the CMOS level RX__CLK signal must travel through the ABT541 buffer as well as through the 'F04 inverter before it arrives at the DP83850 input. More specifically, the limited slew rate CMOS output of the DP83840 will be ''sampled'' at approximately 1.5V by the ABT541 buffer because the buffers input threshold is nominally 1.5V. This can result in duty cycle distortion that will then propagate on through the 'F04 inverter and into the DP83850 device. To minimize the potential for duty cycle distortion, it is recommended that a simple voltage divider be placed at the RX__CLK output of each PHY device. This voltage divider as depicted in *Figure 11* will provide the ABT541 input with a nominal 3V pk-pk clock signal which will help to minimize the potential for duty cycle distortion. This technique is not necessary at the related outputs of the ABT541 buffer or the 'F04 inverter due to their output drive characteristics.

5.3 MII Transmit Operation

The MII transmit operation is a synchronous nibble wide data transfer from the DP83850 RIC device to the DP83840 PHY devices.

Upon reception of CRS from the DP83840 PHY which is actively receiving data from the network, the DP83850 asserts the TXE (transmit enable) lines to all of the idle DP83840 PHYs. Along with the assertion of the TXE signals, the DP83850 also transmits the MII Transmit data consisting of TXD[3:0] and TX__ER. This data is then repeated out to the network via all of the active transmitting DP83840 devices.

The relative timing of the MII transmit operation is depicted in *Figures 12* and *13*. These timing diagrams illustrate a normal transmit operation without errors and a transmit operation with error propagation.

The relative timing for ''transmission without error(s)'' in *Figure 12* illustrates the desired sequence of events which occur during MII transmission.

The relative timing for ''transmission with error propagation'' is similar to the previous case except that the TX__ER signal is asserted during the packet transmission operation. This ensures that any receive packet error will be repeated in the transmit operation. By repeating the packet error to the destination node, that node can process the error without interdiction from the 100BASE-TX repeater system.

5.3.1 Transmission and Collisions

100BASE-TX repeater applications process collisions differently then 100BASE-TX node applications.

A 100BASE-TX node based on the DP83840 device will generate a CRS signal, which appears on the ''CRS'' output of the DP83840, for either packet reception or packet transmission. This indicates to the MAC Layer that the Physical Layer is operating properly. However, when CRS is asserted due to simultaneous packet transmission and reception, the DP83840 will assert its ''COL'' output which indicates a collision condition to the MAC Layer. This causes a JAM pattern to be transmitted and then attempts another transmission per the CSMA/CD back-off algorithm.

In a 100BASE-TX repeater based on DP83850 and DP83840 devices, only packet reception will cause the assertion of the CRS signal. CRS remains unasserted for transmission operations. In this case, simultaneous reception on two or more repeater ports will cause CRS to assert from two or more DP83840 devices. Multiple CRS signals are processed by the DP83850 RIC device and interpreted as a collision event (refer to *Figure 14*). Upon a collision event, the DP83850 will send a JAM pattern to all ports for the remainder of the transmission period.

To select between the node and repeater modes of operation, the DP83840 ''REPEATER'' input pin should be properly configured. As shown in *Figure 4*, a logic high level on this pin will configure the DP83840 for repeater operation. A logic low on the ''REPEATER'' input will configure the DP83840 to node mode.

5.3.2 MII Transmit Physical Connection

The physical connection between the DP83850 and the DP83840 required to support an MII transmit operation is illustrated in *Figure 15*. Unlike the MII receive bus, the transmit bus does not require special buffering. Since the signal path of the MII transmit section is essentially fixed, a single termination point at the end of each MII transmit signal is sufficient to provide good signal integrity.

TXD[3:0] and TX__ER are the only bussed MII transmit signals. Because the DP83850 provides twelve TX__EN outputs, these signals can be routed individually to each corresponding DP83840 device. The TX__CLK output of the DP83840 device need not be connected to the DP83850 input because both devices operate synchronously from the same master reference clock which is used for the MII transmit data transfer.

Every effort should be made to minimize the overall length of the MII transmit bus. Additionally, it is good practice to route each MII transmit signal as a single contiguous path from the DP83850 to the final AC termination point as shown in *Figure 15*. Additionally, by placing 22Ω series resistors at the beginning of each TXD signal line, potential signal aberrations can be further controlled.

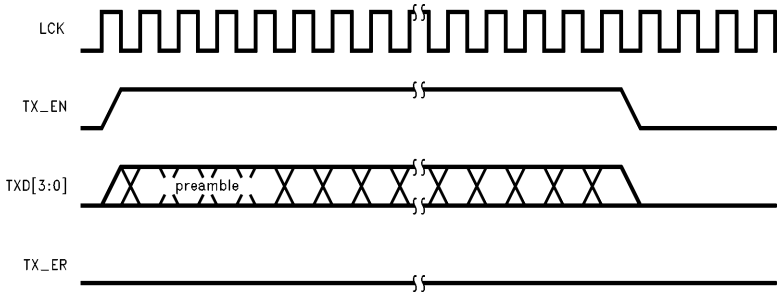

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FIGURE 12. MII Transmission without Error(s)

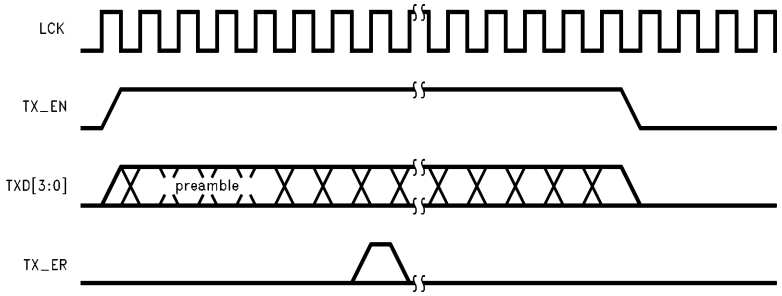

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FIGURE 13. MII Transmission with Error Propagation

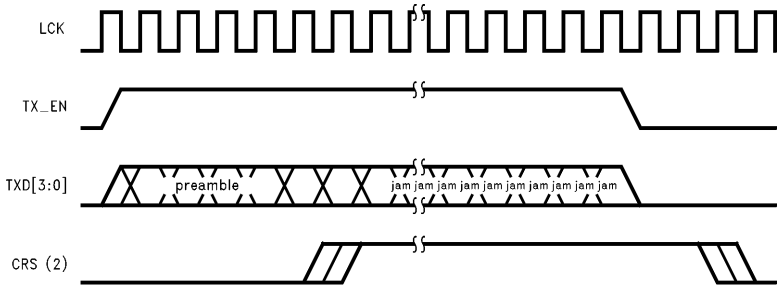

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FIGURE 14. MII Transmission with Collision

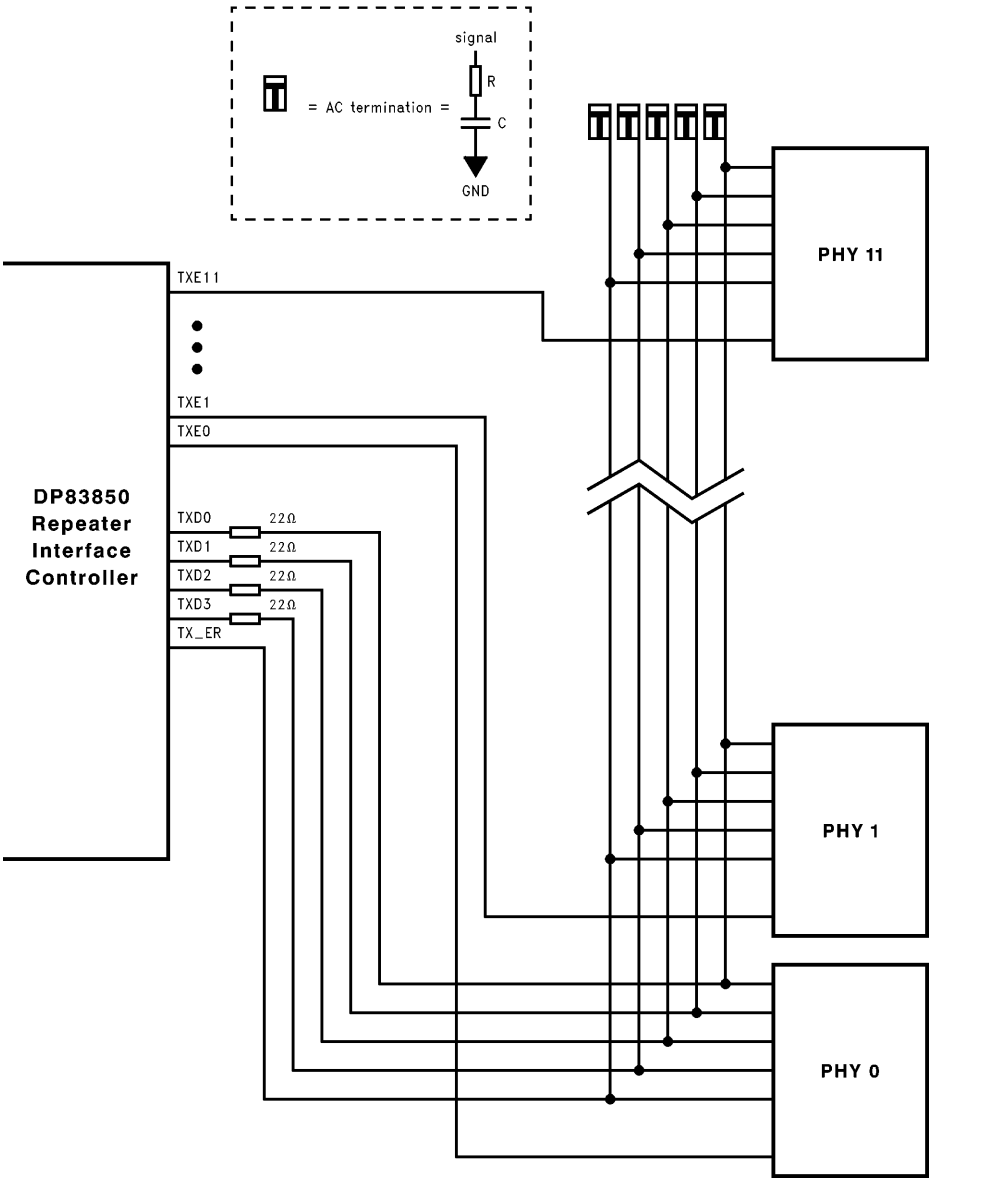

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FIGURE 15. MII Transmit BUS Physical Connection and AC Termination

6.0 100RIC REPEATER CONTROLLER

The DP83850 100RIC Repeater Controller IC provides the basic packet control for the 100BASE-TX repeater system. This controller includes a significant feature set which allows it to provide a number of different functions. For this 12-port unmanaged application, however, only those functions that are required for unmanaged operations are considered. Features relating to the Inter-RIC™ bus as well as connectivity to a Media Access Controller (MAC) of a Repeater Information Base (RIB) are outside the scope of this document. *Figure 16* provides the connection diagram for the DP83850.

The straightforward interconnect of the DP83850 to the MII results in a simple overall implementation. The only special connection considerations relative to the DP83850 pertain to the IR__VECT[4:0], ~IR__COL__OUT and ~IR__COL__IN pins as well as the ~IR__ACTIVE and ~ACTIVEO pins. These Open-Collector pins each require a 1 kΩ pull-up resistor to V_{CC} and should be connected as indicated in *Figure 16* to ensure proper operation in an unmanaged application. It is also important to connect ~IR__COL__OUT directly back to ~IR__COL__IN to ensure proper operation in an unmanaged application. Each Open Collector pin of the DP83850 is indicated as so with an "**(OC)**" as shown in *Figure 16*.

Those pins or groups of pins marked with the reference "**(MAN)**" are intended to support managed applications and the Inter-RIC bus. It is recommended that these pins be connected to a header strip or similar connector in order to provide an easy migration from an unmanaged to a managed repeater design. Please refer to the DP83850 datasheet for detailed information regarding a managed application.

7.0 REFERENCE CLOCK

The DP83840 and DP83850 devices require a reference clock in order to operate. This reference clock is used for all of the synchronous transmit operations of the 100BASE-TX repeater. While there are several methods for implementing the reference clock in a 100BASE-TX repeater application, the following methods provide robust and proven solutions for designs that support Auto-Negotiation as well as those that do not.

7.1 Reference Clock Option One

Figure 17 illustrates the circuitry and interconnection recommended for generating and distributing the system reference clock for an unmanaged 100BASE-TX repeater that does not support Auto-Negotiation.

A properly filtered 50 ppm 25 MHz oscillator will provide a stable source for the reference clock. The output of this oscillator should be routed first to the 74CT2525 and from there, to the DP83850 input. By including an option for AC termination at the input to the DP83850, potential signal reflections can be partially controlled.

In order to distribute the clock to multiple PHY devices, a low skew clock driver such as the 74CT2525 provides a simple method for deriving multiple synchronous phase aligned clocks with sufficient signal drive. With the proper clock signal routing, a single output from the 74CT2525 can effectively source two PHY devices. Additionally, the inclusion of an R/C network, placed as close as possible to each of the 74CT2525 outputs, will help to control the high frequency components of the reference clocks for EMI control purposes. As illustrated in *Figure 17*, by routing the clocks to the PHY devices in a daisy chain configuration and providing AC termination at the end of the signal paths, signal integrity can be maintained. It should be noted that for each PHY device the 25 MHz clock should be routed to both the REFIN and OSCIN inputs.

Supplying the clock to the REFIN input provides the PHY with the required reference. Supplying the clock to the OSCIN input is necessary to ensure proper initialization of the PHY device. While the OSCIN input normally requires a 50 MHz reference, a 25 MHz reference may be used when Auto-Negotiation is not included in the design.

7.2 Reference Clock Option Two

Figure 18 provides a recommended reference clock scheme for a 100BASE-TX repeater that does support Auto-Negotiation.

This clock generation and distribution scheme is similar to that given in Section 7.1 except that the PHY devices, in order to support Auto-Negotiation, must be sourced 20 MHz along with the required 25 MHz clock. Therefore, the second oscillator is required to generate the 20 MHz clock signal. While it would be possible to simply source a 50 MHz clock to each PHY for both 100 Mb/s and Auto-Negotiation functionality, the use of 25 MHz and 20 MHz clocks will keep distributed system clock signals below the 30 MHz limit imposed by the FCC for EMI purposes.

The R/C networks placed at each output of the 74F2525 must also be considered. In order to avoid too much high frequency attenuation the values for the resistors and capacitors must be selected to provide optimum frequency control for the 25 MHz signals being distributed. Similarly the AC terminations located at the end of each routed clock signal must also be selected to provide optimal termination relative to the 25 MHz clock signal.

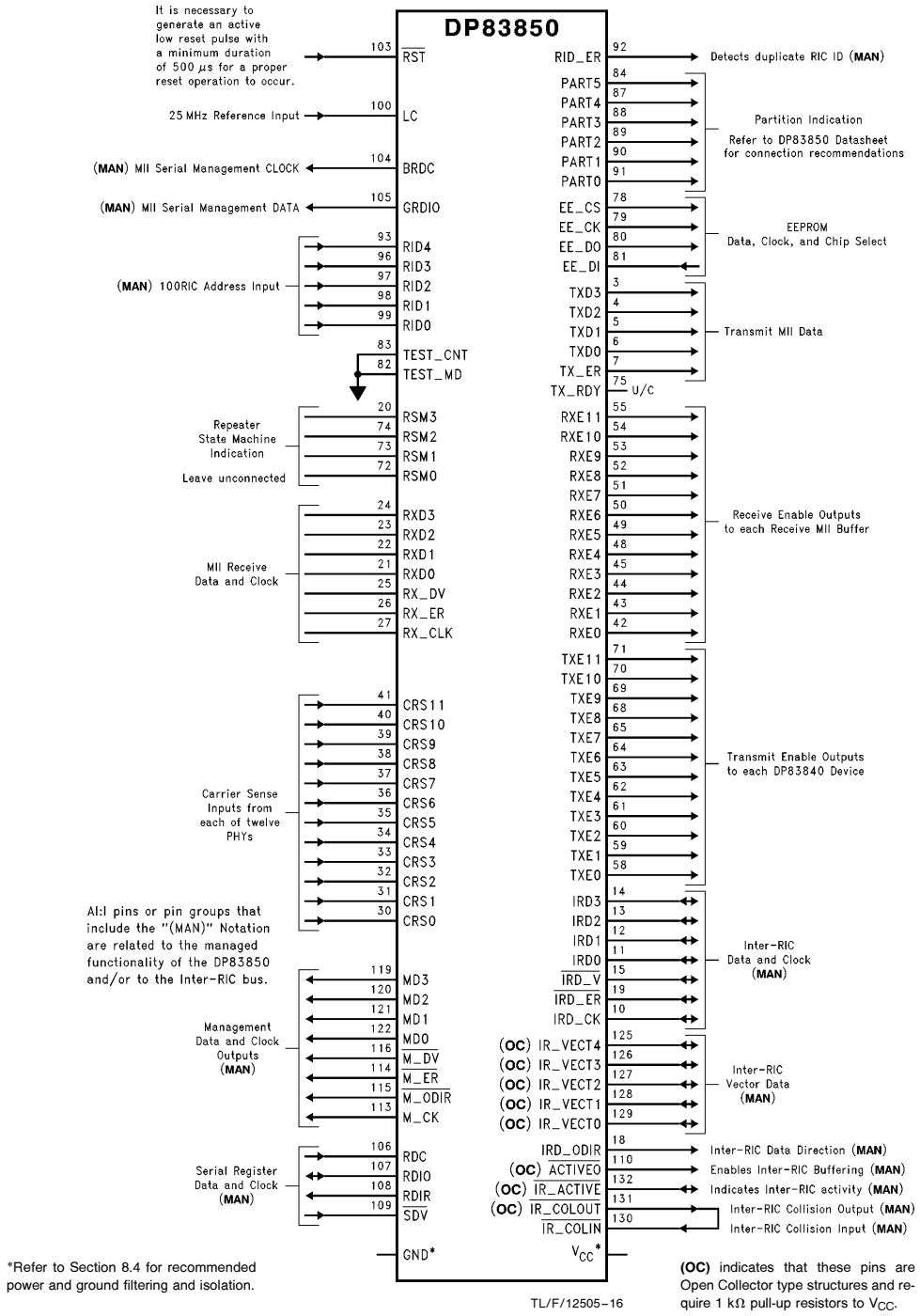

FIGURE 16. DP83850 Connection Diagram

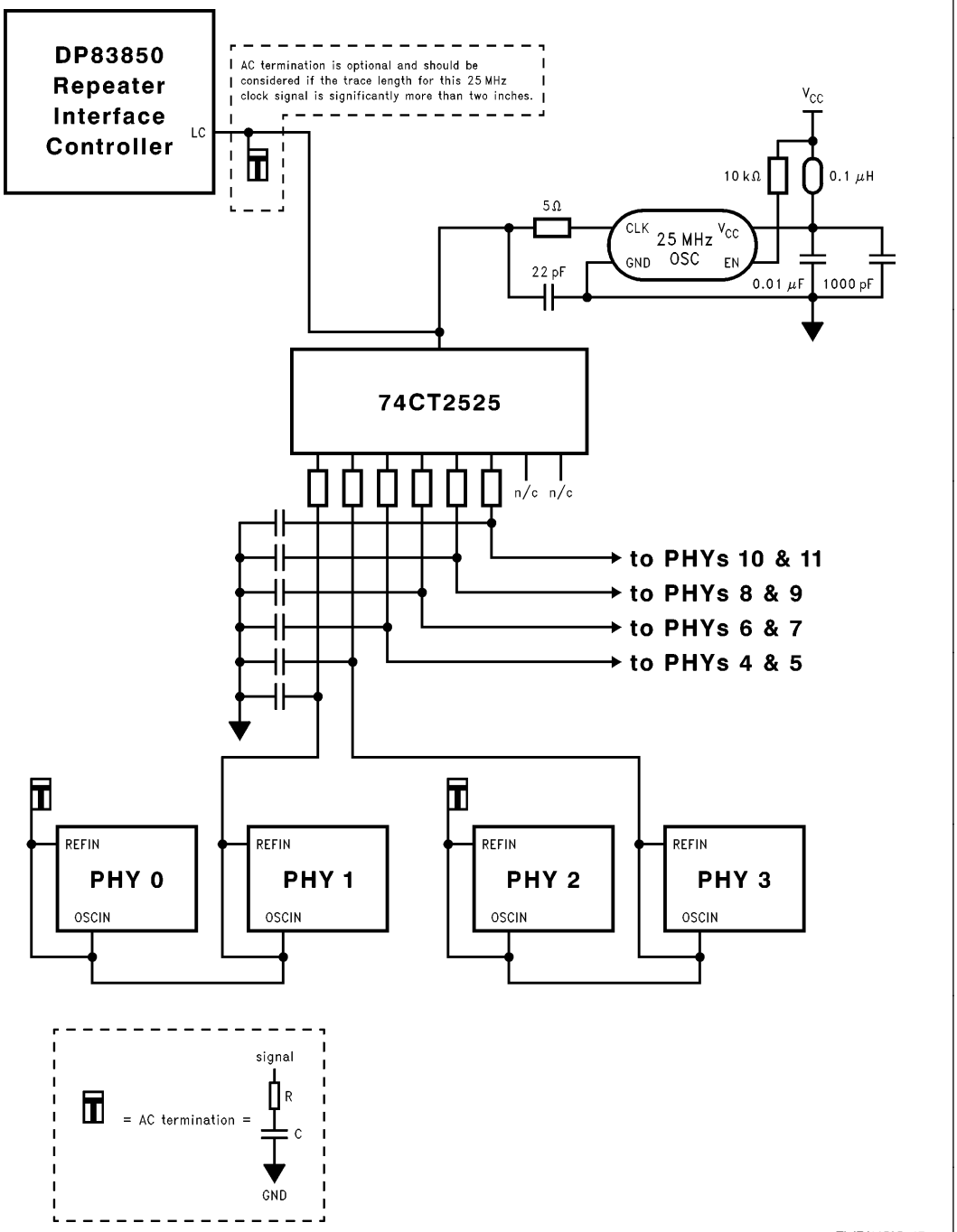

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FIGURE 17. Reference Clock Recomendation for a Non-Auto-Negotiating 100BASE-TX Repeater

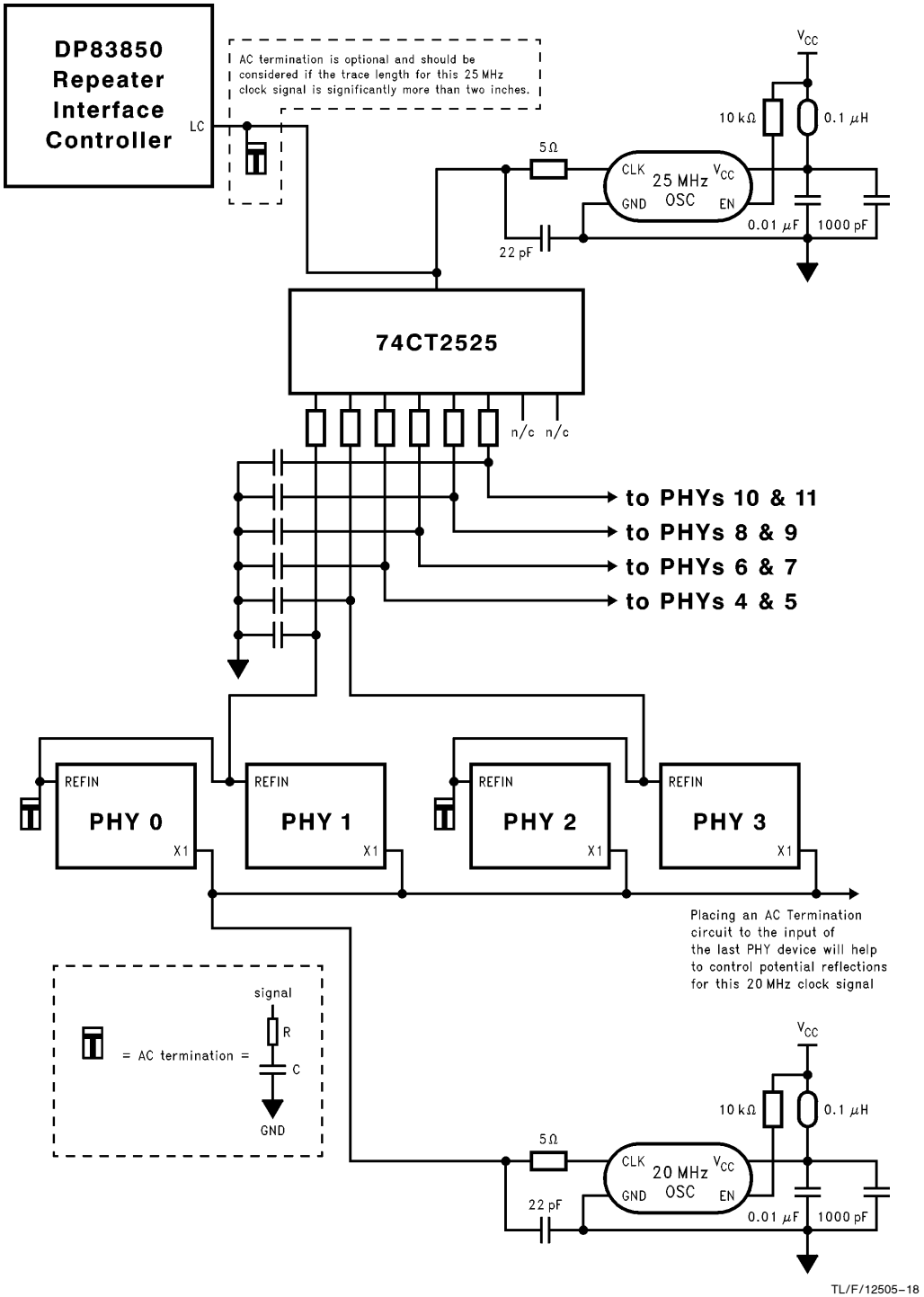

FIGURE 18. Reference Clock Recommendation for An Auto-Negotiating 100BASE-TX Repeater

8.0 PHYSICAL LAYOUT

The goal of any complex system design, especially one which includes both analog and digital functionality, is to achieve the most robust system performance possible. Performance aspects such as fault tolerance, bit-error-rate, EMI, synchronous timing, and general signal integrity must all be considered.

The right combination of component placement, signal routing practices, and power supply distribution will yield a robust and reliable system.

This section explores the physical design aspects that must be considered when designing an unmanaged 100BASE-TX repeater. The latest National Semiconductor 100k ECL Databook and Design Guide provides considerable detail regarding the theory and practice of system design. With focus on such areas as ''Transmission Line Concepts'' and ''Power Distribution and Thermal Considerations'', the EGL Design Guide provides substantial insight to many physical layout parameters and their subsequent effects on signal integrity.

8.1 Component Placement

The relative placement of the individual active and passive components within a 100BASE-TX repeater is essentially defined by some important design considerations: cost, board area, and performance.

Figure 19 illustrates one potential component layout approach that will yield good signal integrity and good overall performance. The intent of this layout is to minimize the required board area while still optimizing the relative component placement. The number of layers required to support this design may vary depending on the signal routing density. In general however, a six-layer board comprised of one ground, one supply, and four signal layers should suffice.

The layout of the dynamic transmit and receive signals at the twisted pair transceiver interface and the MII is critical. Optimizing the relative orientation of each DP83840 with its corresponding DP83223 helps to minimize the signal routing required for the 125 Mb/s serial data as illustrated in the detail diagram given in *Figure 19*. By placing the DP83850 RIC device near the first port of the repeater, the MII transmit signals can be routed easily as described in Section 5.3.2. Additionally, by clustering the ABT541 buffers close to the DP83850, the common MII receive bus size is minimized as described in Section 5.2.2

While relative component placement is important, board area constraints pose certain limitations. If the component placement suggestion given in *Figure 19* is implemented, there would be very little area remaining on the top side of the system board for the required passive components. By placing a majority of the passive components (resistors, capacitors, and ferrite beads) on the bottom side of the board, the system layout constraints can still be met.

8.2 Signal Routing

This section focuses on several aspects of signal routing which can contribute to robust signaling within the 100BASE-TX system design. *Figure 20* illustrates one signal routing example for the critical 125 Mb/s sections of the design. Considerations such as controlled impedance trace routing and termination techniques are important. Recommendations for both the high speed (125 Mb/s) and the lower speed (25 Mb/s) signals are provided.

8.2.1 Controlled Impedance of Signal Traces

It is important to incorporate controlled impedance routing for those signal traces which carry the 125 Mb/s serial data. Either standard micro-strip or strip-line techniques are recommended. Please refer to the latest F100K ECL Design Guide from National Semiconductor for detailed information regarding transmission line concepts.

It is important to choose an impedance of 50Ω for each trace that carries 125 Mb/s data between the RJ-45, the magnetics, and the DP83223 transceiver. This is necessary in order to match the 100Ω differential impedance of the unshielded twisted pair cable.

The 125 Mb/s PECL signals that connect between the DP83223 and the DP83840 can be routed as 100Ω impedance traces and terminated with 100Ω terminations to help reduce system power requirements.

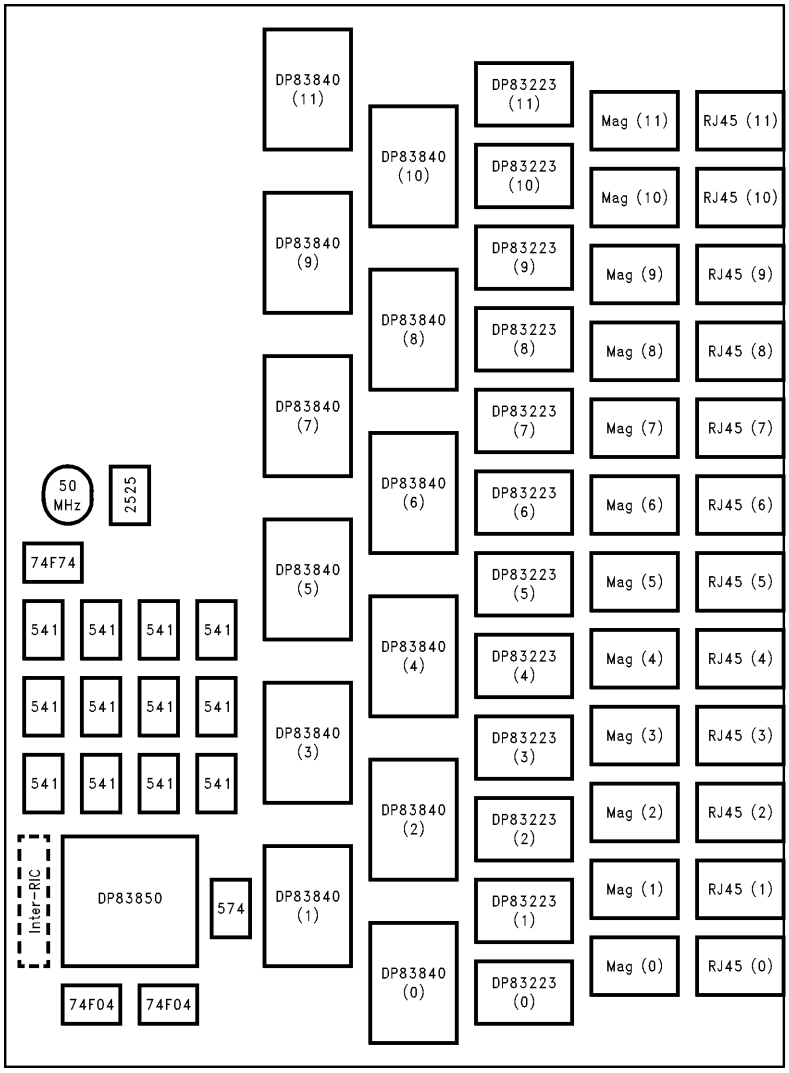

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FIGURE 19. Component Placement for a 12-Port 100BASE-TX Repeater

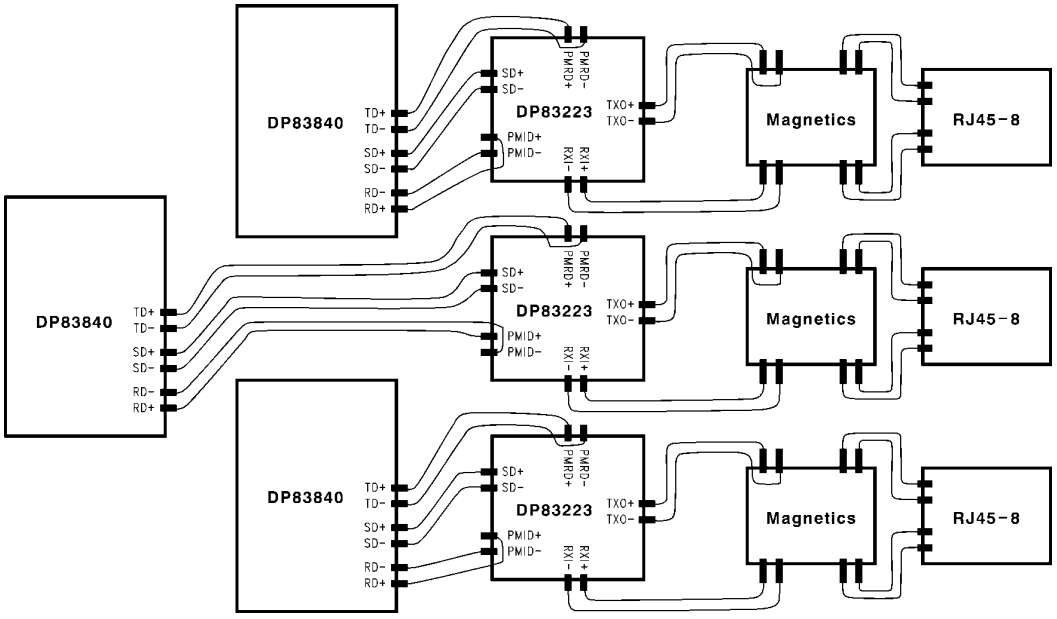


FIGURE 20. 125 Mb/s Signal Routing Example for Non-Auto-Negotiating 100BASE-TX Repeater

8.2.2 Signal Trace Termination

Proper termination of a high speed signal trace is essential in order to maintain an effective transmission line. In general, it is practical to regard any high speed (125 Mb/s) signal trace that is longer than one inch in total distance as a transmission line. High speed (125 Mb/s) signal traces less than one inch may still provide robust signal transfer without employing some of the transmission line design techniques. Additionally, lower speed signal traces (i.e. 25 Mb/s), do not usually require the added component cost and power requirements of controlled transmission lines. *Figures 21* and *22* provide two alternatives for Pseudo ECL Termination techniques. Either of which will provide good signal integrity for the 125 Mb/s signals routed between the DP83840 and the DP83223 devices.

8.2.3 General Guidelines

General guidelines regarding optimal signal trace routing practices include:

- Minimal length controlled impedance signal traces to minimize reflections and decrease noise sensitivities
- Matched length differential signal traces to minimize jitter
- Radiused routed trace corners of >45 degrees
- Minimized number of vias for any one given signal trace
- ECL terminations placed close to signal destination
- All controlled impedance traces routed directly over or under uninterrupted power or ground planes on adjacent layer(s)

8.3 Power Supply Recommendations

Careful power supply filtering and isolation practices can provide a minimized noise environment for each of the unique digital and analog sections of both the DP83223 and DP83840 devices. Additionally, providing substantial planes for both the system and chassis grounds will help to minimize potential noise sources that may detract from good EMI performance.

8.3.1 V_{CC} Plane Partitioning

Figure 24 illustrates the recommended V_{CC} plane partitioning. In this example, V_{CC} is separated into three distinct sources: Digital, PECL, and Analog. For purposes of reference, the Digital section is referred to as a plane whereas the PECL and Analog sections are referred to as islands.

The Digital V_{CC} plane supplies power to the main system which includes most of the digital devices such as the DP83850, buffers, inverters, and other potential devices. Additionally, the Digital V_{CC} also supplies power to a majority of each DP83840 device. Refer to Section 8.4 for detailed power supply connection information.

The PECL (Pseudo ECL) V_{CC} is divided up into one island per port. These islands supply power to the Pseudo ECL interface between each DP83223 and its corresponding DP83840. In this example, each port is given its own PECL island in order to minimize noise coupling between adjacent ports.

The Analog V_{CC} is also divided up into one island per port. These islands supply power to the sensitive analog Transmit and Receive sections of the twisted pair Transceivers. It is important to keep the power sources for these analog sections isolated from the Digital and PECL V_{CC} planes and islands in order to provide as much noise margin as possible. This helps to ensure robust signaling in extreme cases such as severely attenuated receive signals caused by very long (100 Meters) cable lengths between connections.

The separation between each V_{CC} plane and/or island on a single board layer should be at least 0.05 inches. This will help to reduce capacitive coupling which may occur as a fringe phenomenon at the edge of each segmented plane or island. Additionally, all island or plane corners >45 degrees should be radiused.

8.3.2 Ground Plane Partitioning

The ground plane should not be partitioned into separate islands. Partitioning of the ground plane can lead to increased EMI emissions which may make the system noncompliant to specific FCC regulations. *Figure 25* provides the recommended ground layout and specifies the division between and placement of the system ground versus the chassis ground.

By keeping the chassis ground back from the edge of the system motherboard by approximately 0.25 inches and simply voiding that gap of any copper will help to reduce any potential fringe radiation that may occur during system operation. This is permissible as no active traces need to be routed in this area anyway.

8.3.3 Board Layers

Figure 23 illustrates one potential option for board layer assignment. This option places particular emphasis on EMI concerns. The eight layer approach is recommended in order to accommodate the significant number of trace interconnections while still allowing sufficient area dedicated to power and ground planes and islands.

As denoted, Layer One (top layer) is normally the component side and this is where all or most of the active devices should be located. By minimizing the amount of trace routing on this layer and maximizing the system ground area, partial EMI shielding can be achieved. It is also important to route the Chassis ground, as shown in *Figure 25*, on this top Layer.

Layer Two should be dedicated to full system ground and chassis ground as illustrated in *Figure 25*.

Layer Three may be used as a signal routing layer. It is important to attempt to route any one continuous trace, or differential trace pair, on a single board layer. As an example, the designer may decide to route all or most of the 125 Mb/s traces on this layer and devote another layer to the slower MII signals.

Layer Four may be used as the V_{CC} layer where the Digital V_{CC} plane and each of the carefully designed V_{CC} islands, as depicted in *Figure 24*, will reside.

The next layer, Layer Five, may also accommodate signal routing.

Layer Six should be dedicated to full system ground and chassis ground as illustrated in *Figure 25*.

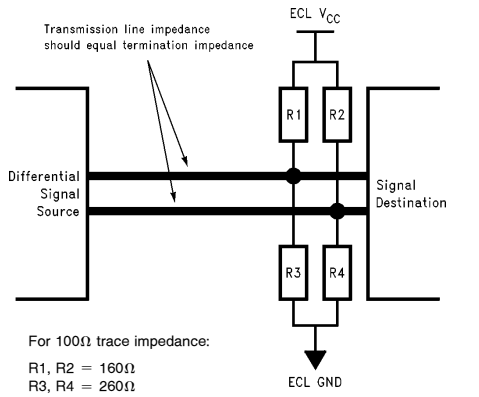
Layer Seven may also accommodate signal routing.

Layer Eight should be physically similar to Layer One. This is traditionally known as the solder-side of the board, however, this side will also carry many passive components. Therefore, the bottom layer doubles as a component side and solder side. As with Layer One, all undedicated space on this layer should be filled in with copper and tied to system ground, except where Chassis ground is located as illustrated by *Figure 25*. Signal routing should be minimized on this layer wherever possible.

By placing System and Chassis ground on both the top and bottom layers, a virtual Faraday cage is produced which will aid in the control of EMI emissions. If more than eight layers are required to accommodate the signal routing, it is

important to interleave these additional signal layers with ground or power planes in order to increase shielding and to achieve good trace impedance control.

Embedding the signal layers within the board does increase the number of vias which will be required to route to and from the active and passive components on the top and bottom layers. This will add some cost to the board and can result in transmission line traces that are marginally less than ideal. However, the potential for good EMI performance is worth the compromise.



For 100Ω trace impedance:

R1, R2 = 160Ω
R3, R4 = 260Ω

For other trace impedance:

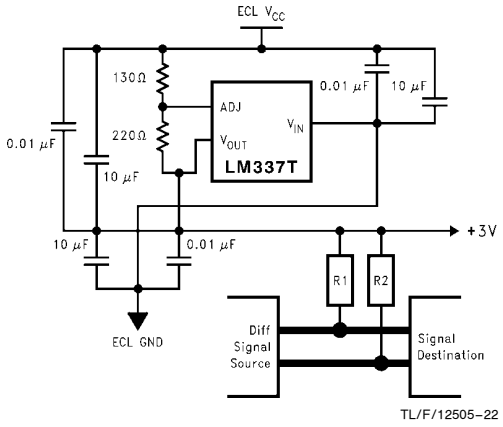
R1, R2 = 1.6 x desired impedance
R3, R4 = 2.6 x desired impedance

FIGURE 21. Thevenin Equivalent PECL Termination

8.4 Power Supply Isolation and Filtering

Proper power supply isolation and adequate filtering will help to reduce system noise sensitivities. The DP83223 and DP83840 devices posses unique analog and digital circuitry that require careful isolation and filtering techniques. *Figure 26* illustrates the V_{CC} and Ground isolation connections recommended for a each port within a typical 100BASE-TX repeater design. Recommended filtering for the DP83850 is also provided.

Due to power handling limitations of the Ferrite Beads, it is recommended that each port be configured as illustrated in *Figure 26*.



R1, R2 = 100Ω or desired resistance (Between 50Ω and 100Ω)

FIGURE 22. Direct PECEL Termination

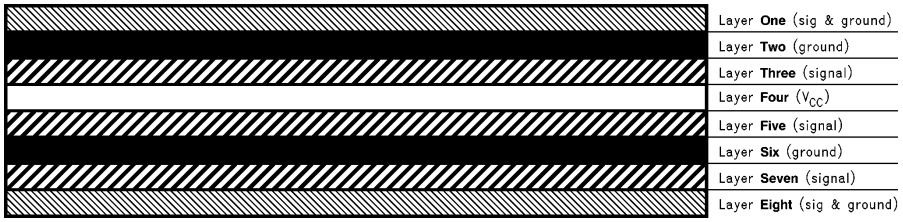


FIGURE 23. Board Layer Assignment Recommendation

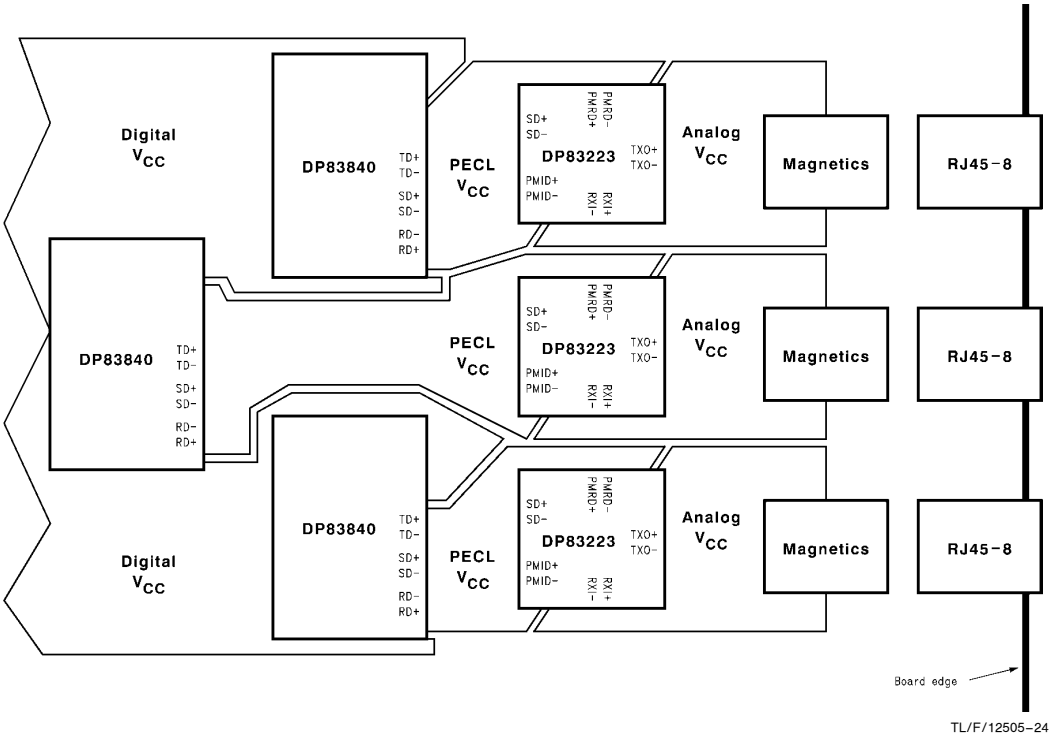


FIGURE 24. V_{CC} Plane Isolation Example for 100BASE-TX Repeater

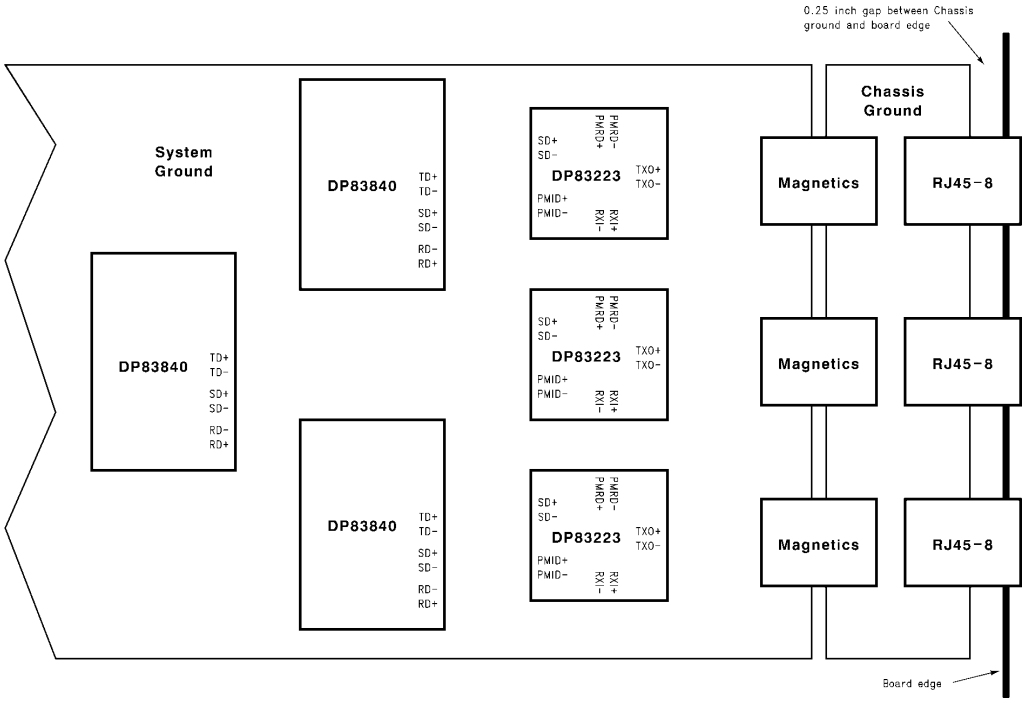


FIGURE 25. GND Plane Isolation Example for 100BASE-TX Repeater

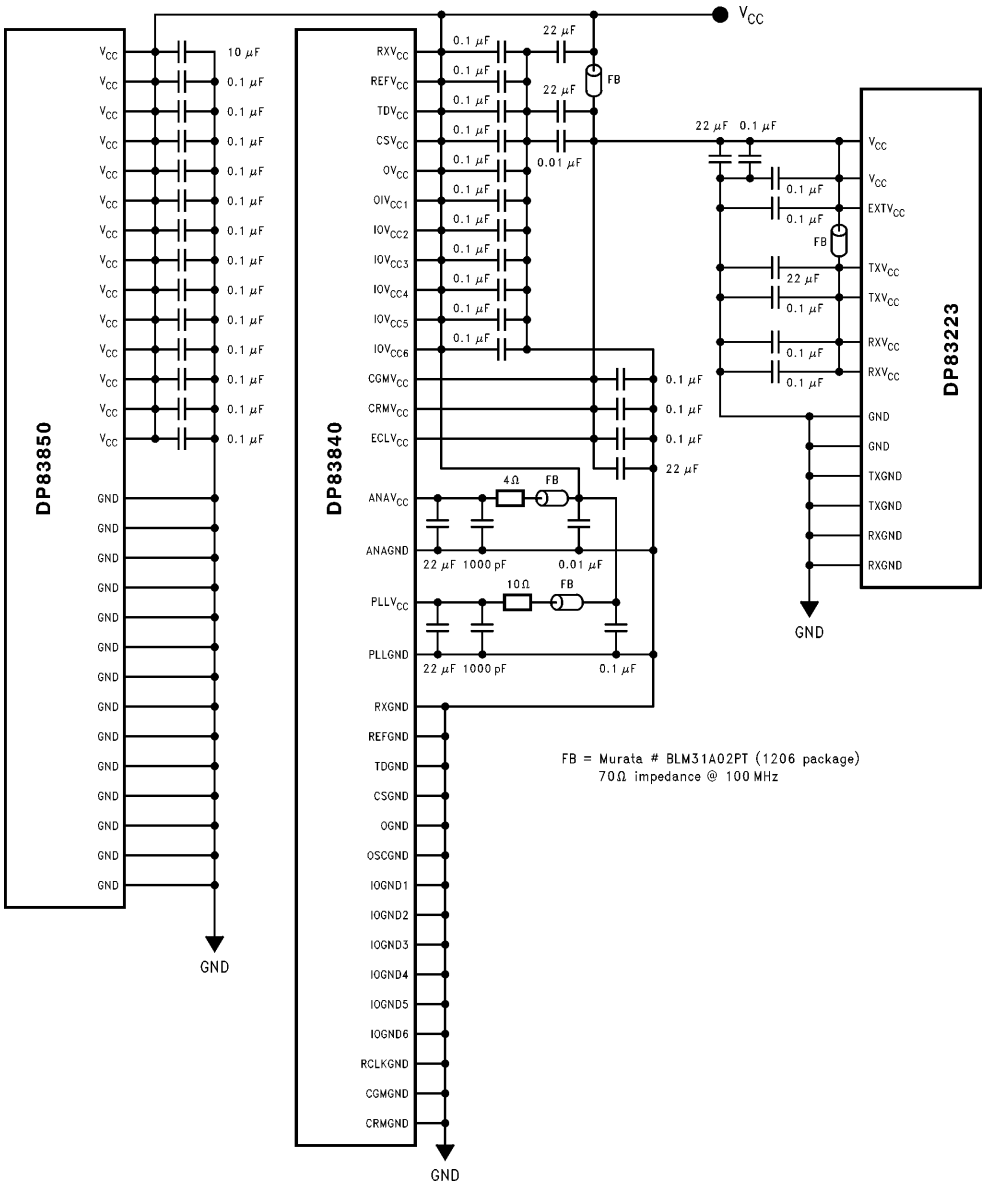


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FIGURE 26. Power Supply Isolation and Filtering Recommendation

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