An Introduction to FPD Link

National Semiconductor
Application Note 1032
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THE FPD LINK CHIPSET

The FPD Link (Flat Panel Display Link) chipset is a family of interface devices specifically configured to support data transmission from graphics controller to LCD panels. The technology employed, LVDS (Low Voltage Differential Signaling), is ideal for high speed, low power data transfer. This enables the implementation of high end displays such as SVGA (800 x 600) and XGA (1024 x 768).

The predominant issues limiting performance in these high end displays are speed, power, and EMI considerations. The user is also concerned with the physical interface to the display; the fewer wires the better. The FPD Link chipset addresses these issues with LVDS technology and muxing TTL signals to higher speed LVDS signals which allows a substantially narrower interface between host and display. In a typical application (see *Figure 1*), TTL-level RGB and control data from the graphic controller arrives at the inputs of the FPD Link transmitter. The parallel TTL data is muxed and converted to LVDS. The outputs of the FPD Link transmitter drive the LVDS data on the cable which connects the motherboard to the display. The LVDS data traverses the cable to the FPD Link receiver at the display. The received data is then demuxed, converted back to TTL levels and sent to the inputs of the timing controller. This muxing of parallel TTL signals allows the data to travel at faster speeds across a narrow interface, addressing needs associated with high bandwidth communication.

The FPD Link chipset consists of transmitters (TTL to LVDS) and receivers (LVDS to TTL) designed to support 18-bit and 24-bit color displays. Devices are available with falling edge or rising edge data strobe for a convenient interface to a variety of graphics and LCD panel controllers. The products initially being released operate with a 5V power supply at a clock frequency range of 20 MHz–40 MHz. Additional product offerings include devices supporting a 65 MHz clock, and parts operating with a 3V power supply. See *Figure 2*.

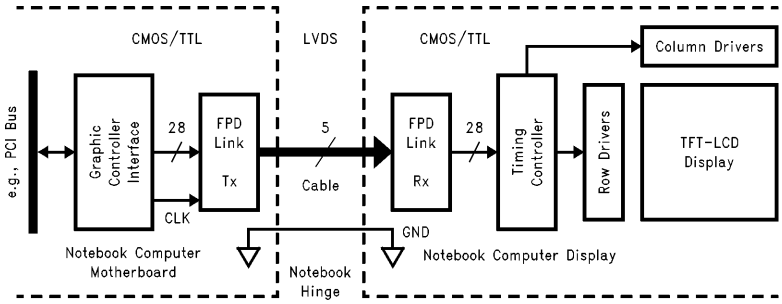

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FIGURE 1. Typical FPD Link Application (24-Bit Color)

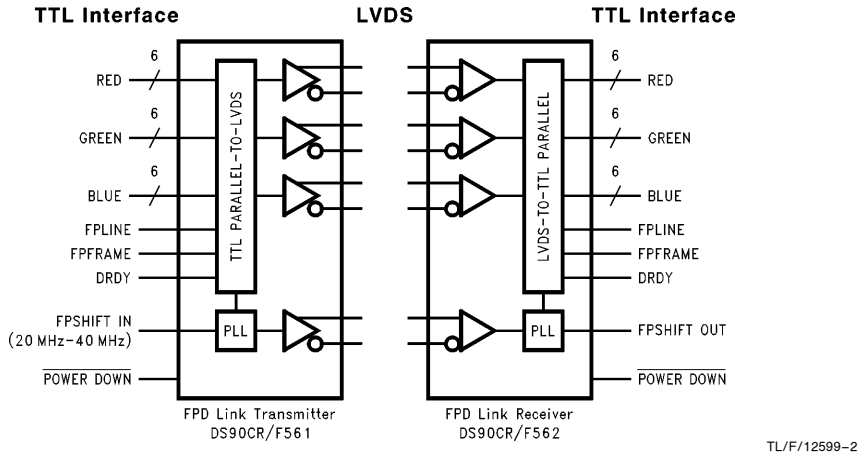

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FIGURE 2. FPD Link Chipset for 18-Bit Color

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Initial product offerings are:

DS90CR561/2 — transmitter/receiver, rising edge data strobe, 21-bit TTL interface (6 Red, 6 Green, 6 Blue, 3 Control bits), 4 pairs LVDS (3 data + clock)

DS90CF561/2 — transmitter/receiver, falling edge data strobe, 21-bit TTL interface (6 Red, 6 Green, 6 Blue, 3 Control bits), 4 pairs LVDS (3 data + clock)

DS90CR581/2 — transmitter/receiver, rising edge data strobe, 28-bit TTL interface (8 Red, 8 Green, 8 Blue, 4 Control bits), 5 pairs LVDS (4 data + clock)

DS90CF581/2 — transmitter/receiver, falling edge data strobe, 28-bit TTL interface (8 Red, 8 Green, 8 Blue, 4 Control bits), 5 pairs LVDS (4 data + clock)

LVDS—THE TECHNOLOGY OF CHOICE

LVDS is a differential signaling technology designed to support applications requiring high speed data transfer, common mode noise rejection, and low power consumption. The low signal swing (345 mV) and differential nature of the signals reduces noise impact (i.e., crosstalk) and allows high operating frequencies. The constant current source is designed for low power consumption: a single LVDS driver has a static I_{CC} of 4 mA and dynamic I_{CC} of 22 mA. These attributes contribute to the low EMI of LVDS.

DESIGNING WITH FPD LINK

The FPD Link chipset provides the support needed for high speed display interfaces such as SVGA(800 x 600) and XGA(1024 x 768). Care should be taken when designing with these devices to fully realize the benefits of the technology.

Board Layout. To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer must also maintain equal length on the signal traces for a given pair. As with any high speed design, the impedance discontinuities should be limited (reduce number of vias, no 90° angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. These considerations limit reflections and crosstalk which would adversely effect high frequency performance and EMI.

Termination. Use of current mode drivers requires a terminating resistor across the receiver inputs. The FPD Link chipset uses a single 100Ω resistor between the positive and negative lines of each receiver differential pair (see *Figure 3*). No additional pull-up or pull-down resistors are necessary as with some other differential technologies (PECL). Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

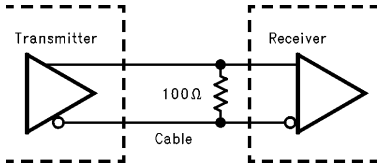

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FIGURE 3. FPD Link Termination

Decoupling Capacitors. Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. Decoupling capacitors (surface mount) between each V_{CC} and ground pin are recommended. Refer to *Figure 4* for an example of connections and capacitor values.

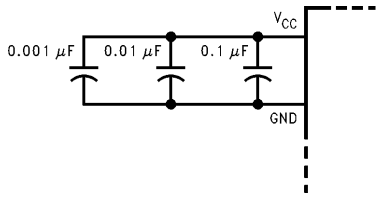

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FIGURE 4. Decoupling Configuration

Cables. A cable interface between the transmitter and receiver needs to support the differential LVDS pairs (2 wires/pair). The DS90CR581/2 and DS90CF581/2 require 10 signal wires; the DS90CR561/2 and DS90CF561/2 require 8 signal wires. This is a significant reduction in cable width as compared to the straight TTL interface which needs 28 or 21 signal wires. Shielded cables will reduce noise emissions that contribute to EMI. In addition, ground lines between each differential pair will provide further noise shielding. The grounding provides a barrier to noise coupling between adjacent pairs, thus reducing additive effects of the electrical fields. In addition to the noise shielding, the low impedance ground connection between the transmitter and receiver provides a common mode return path. A minimum of two ground conductors is recommended to provide this low impedance path.

An ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is recommended that cable skew remain below 350 ps to help maintain a sufficient data sampling window. Edge rate attenuation should also be limited to avoid signal degradation at high frequencies. Both skew and edge rate attenuation are a function of cable length. As the distance between host and display increases, a higher quality cable is needed to preserve signal integrity.

Though the interconnect between host and LCD is typically short, the FPD Link transmitters can drive cables over 5 meters long. This makes the FPD Link useful for remote display applications.

TTL TO LVDS TRANSLATION

The FPD Link transmitter translates 21 or 28 bit wide TTL data into LVDS data 3 or 4 bits wide and 7 bits deep. An additional pair of LVDS signals is used to transmit the clock. All 21/28 parallel TTL bits are transferred with a single data strobe. A single strobe also transmits all bits at the LVDS port. The clock to data relationship at the LVDS interface is shown in *Figure 5.* The clock at the LVDS ports is transmitted at the TTL clock input frequency (i.e., 40 MHz); the data is transmitted at 3.5 times the clock frequency (i.e., 140 MHz).

The TTL data bits are mapped into the 3 or 4 LVDS signal lines. *Figures 6* and *7* show the relationship of parallel TTL data bits to the LVDS link.

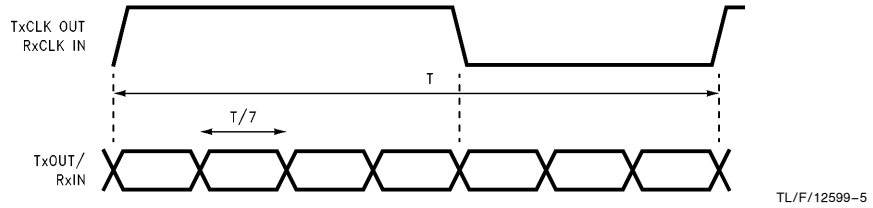

FIGURE 5. Seven Bits of LVDS in One Clock Cycle

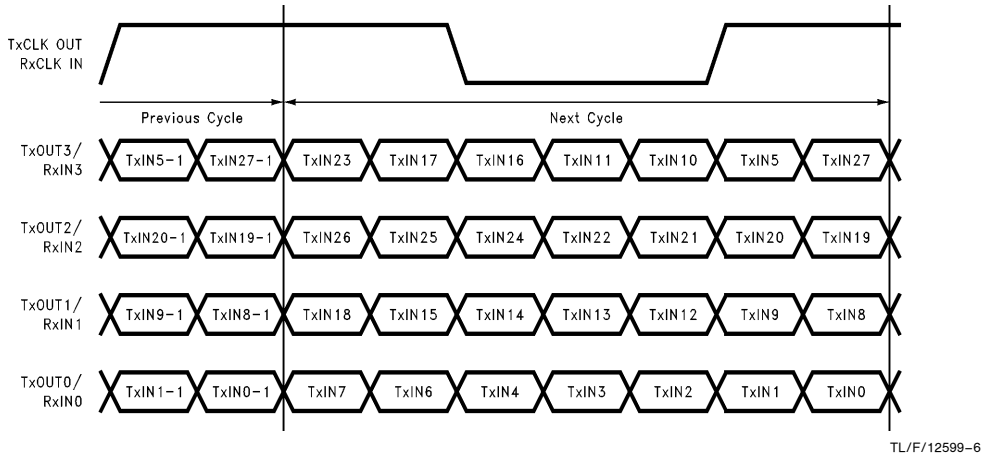

FIGURE 6. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR581)

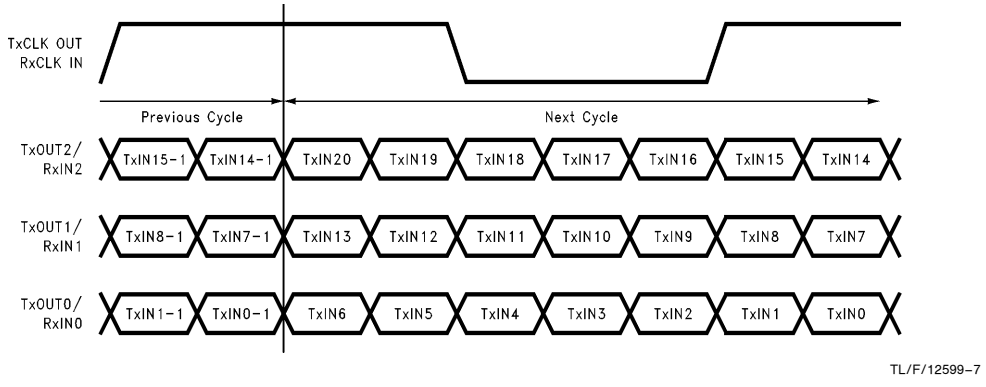

FIGURE 7. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR561)

POWER SEQUENCING

Outputs of the FPD Link chip remain in TRI-STATE® until the power supply reaches 3V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 4.5V and the Powerdown pin is above 2V.

When powering down the device, the Powerdown pin may be asserted. This will TRI-STATE the outputs to prevent excess current flow (10 μA maximum). This input is typically driven by power supply control logic.

The FPD Link chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through a diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device. (Note: latchup immunity is $>$ 300 mA) In addition, an external circuit can be used such that when the receiver board powers down, the transmit Powerdown pin is pulled low to TRI-STATE the transmitter outputs so short circuit current does not flow.

CLOCK INVERSION

The FPD Link chipset is available with rising or falling edge data strobe. A rising or falling edge strobe device should be selected based on the characteristics of the timing controller being used. If the strobe of the FPD Link device does not match that of the timing controller, a simple inverting buffer may be used at the transmitter input and receiver output to invert the signal.

CLOCK JITTER CONSIDERATIONS

The FPD Link devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. These high speed signals require an accurate, low noise clock signal. The width of the LVDS data bits is one seventh the clock period. For example, a 40 MHz clock has a period of 25 ns; the width of a data bit is 3.6 ns. Differential signal skew, interconnect skew, data and clock jitter all reduce the available window for sampling data. It is recommended to keep each component as small as possible to support the maximum operating frequency. The initial clock source should provide a clean signal to the Tx clock input. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

EMI BENEFITS

One of the benefits to using the FPD Link chips with their LVDS signaling is the relatively low EMI. LVDS has demonstrated lower spectral content (EMI) than competing technologies such as RS-422, PECL, and CMOS (often used in display interface applications). Testing was performed using DCM (direct contact method) with a 32 MHz continuous wave. Low EMI translates to less noise on a cable in a box-to-box transmission environment. The cable shielding requirements are less, thus the cost of interconnect is reduced.

CONCLUSION

The FPD Link chipset architecture in conjunction with the LVDS technology provides the high bandwidth interface necessary for leading edge display technology. The conversion from parallel TTL to serial LVDS allows for a narrow interface between graphics controller and panel. A narrower interface means lower cable cost and simplifies the physical connection through a notebook hinge. The high speed of the LVDS technology supports the high data transfer rates required. EMI problems typically associated with such high speed transmissions are addressed by the low signal swing and differential nature of LVDS. LVDS, with its high speed capabilities, will allow future products in the FPD Link chipset to support the industry's ever increasing needs for bandwidth. National's FPD Link provides the solution for the latest in display technology.

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