HiSeC™ Remote Keyless Entry System Utilizing the MM57HS01 Decoder

National Semiconductor
Application Note 1033
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INTRODUCTION

This application note explains how to use the MM57HS01 decoder in an HiSeC remote keyless entry system with the HiSeC rolling code encoder NM95HS01. Such a system consists of 1 to 6 transmitters (key fobs) and one receiver.

1.0 RF BASED SYSTEM

Radio frequency is often used to transmit data from the transmitter to the receiver, because it frequently provides the best convenience for the user.

1.1 Transmitter Design

In the RF transmitter there is a NM95HS01 encoder driven by a low cost RC clock (R4, C7). The values of R4 and C7 result in a CKI frequency of about 53 kHz. A LED with a preresistor (R5) is used to provide a visual feedback for the user. The keys S1 and S2 activate the transmitter. If 3 or 4 keys are needed the 14-pin version of the NM95HS01 has to be used instead of the 8-pin version. The RF transmitter stage has been designed especially for the use with a single lithium battery (3V). It provides high radiated RF power of −12 dBm and spurious emissions of lower than −40 dBm. For technical details on the RF design and a PCB layout see AN-1021 3V RF-Transmitter.

To work together with this hardware and the MM57HS01 receiver the NM95HS01 encoder needs a special configuration programmed into its internal EEPROM. The following configuration selects the correct timing values and bit coding format, the correct frame format and some special features.

NM95HS01 EEPROM Array Configuration

AutoResync:	1	
LEDSEL:	0	RFEN/LED=RFEN
BatteryType:	0	
(Low battery detection		3V)
TIMEOUTEN:	1	
Pause1: (bit3)	1	
Pause0: (bit2)	0	
FactoryDisableBit:	1	algo protect
WriteDisableBit:	0	clear
PreamblePresent:	0	disabled
SyncType:	1	
SyncPresent:	1	NRZ
FixSize:	1	
FixPresent:	1	24 bits
DynSize:	1	36 bits
ParityPresent:	1	enabled
CompareEnable:	1	enabled
IRSel:	0	RF format
PRSel2:	1	\
PRSel1:	0	> PWM 33% / 66% start high
PRSel0:	1	/
TxPol:	0	noninverted
SCLK:	1	PSC 2
Prescaler3: (hex)	02	
Prescaler2: (hex)	02	
Prescaler1: (hex)	01	
Dynamic start code: (hex)	xxxxxx	
KeyIDCode: (hex)	xxxxxx	
SyncFieldCode: (hex)	FE	
Custom algorithm: (hex)	00	
Programming data stream: (hex)		9A7F54208lxxxxxxxxxxx FE00

(x = hexadecimal digit 0..F)

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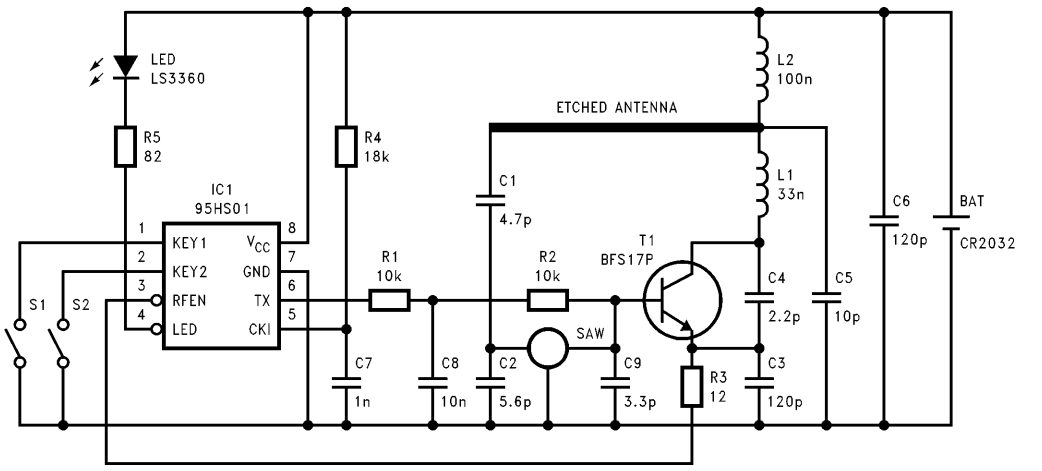


TL/D/12600–1

FIGURE 1. HiSeC 3V RF Transmitter

With the clock frequency of 53 kHz these settings result in the following timing values which may vary in the real application because of the tolerances in the RC oscillator:

Bit length (t_{PWM}):	1.4 ms
Pause between frames:	30 ms
Time-out length:	45s
Autoresync time:	6s

The special features used with this configuration are:

- Low battery detection is enabled. The transmitter detects and indicates a low supply voltage.
- Autoresync is enabled. When both key 1 and key 2 are held down for more than 6 seconds the transmitter will reset. The next time one of the keys is pushed sync frames are sent out. This is used for learning and resynchronization procedures.
- Time-out is enabled. The transmitter will automatically enter halt mode when a key is held down for more than 45 seconds.

If one of these features is not desired to be used in the system the related bits in the NM95HS01 array configuration have to be cleared. E.g. to switch off low battery detection set the CompareEnable bit to 0.

1.2 Decoder Design

On the decoder side there is the MM57HS01 reading the incoming data stream, evaluating the HiSeC frames and verifying the rolling codes. The configuration data and the information about the learned keys is stored in an NM93C46 serial EEPROM. The decoder part is clocked by a simple RC network (R = 3.3 kΩ, C = 56 pF). The circuit at the $\overline{\text{RESET}}$ pin automatically resets the chip on power-up.

The LM2936 voltage regulator provides the decoder circuit with the needed 5V supply voltage.

The RF signals are received by a radio receiver such as the super-regenerative RF receiver shown in AN-985 (Designing and Programming a Complete HiSeC™-based RKE System) or a common RF receiver module.

The load drivers must be designed accordingly to the characteristics of the loads. They need to have high impedance inputs, because on first power-up the decoder reads the status of the four data pins to get the configuration settings. In this example a pull-down resistor is used to provide the $\overline{\text{DATA1}}$ pin with a logic LOW level. This resistor R_{toggle} has to draw down the level against the internal pull-up resistor which is about 100 kΩ. So the decoder selects toggle mode instead of normal mode for the outputs. If it is desired to use the decoder in normal output mode then R_{toggle} has to be removed from the circuit. To ensure that loads are not unintentionally activated during the reset phase (which lasts about 1 second), it may be necessary to qualify the load drives with both $\overline{\text{VALID}}$ and $\overline{\text{RESET}}$ signals. This is not shown in *Figure 2*.

The user gets a visual feedback from the receiver through the Status and Error LEDs. The Learn switch is used to set the receiver into learn mode. If the Resync switch is closed the receiver automatically resynchronizes to incoming valid sync frames. If this switch is open the decoder will not do any resynchronization. The $\overline{\text{RESYNC}}$ pin can also be driven by a special external circuit, e.g. in a car the resynchronization can be coupled with the ignition.

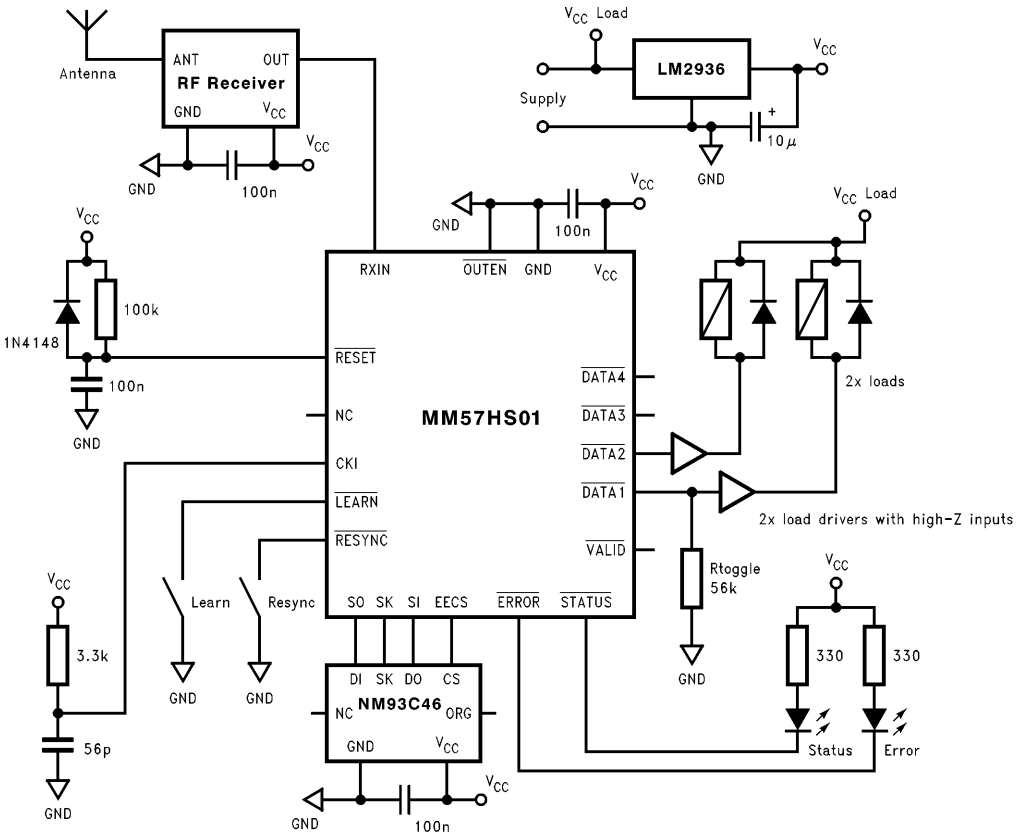


FIGURE 2. HiSeC RF Receiver Utilizing MM57HS01 Decoder

2.0 HOW TO USE THE HiSeC SYSTEM

2.1 Initialization

To get the NM93C46 EEPROM initialized correctly by the decoder part on first power-up make sure that it is blank (all cells contain 00 or FF hex). If an EEPROM is used which has already been initialized by a MM57HS01 decoder, then the configuration will be read out of the EEPROM and the state of the DATA pins will be ignored. So in the application the DATA pins are read only once to initialize the EEPROM and then never again.

When the system is used for the first time you have to learn the transmitters which the decoder should accept.

2.2 Learning Procedure

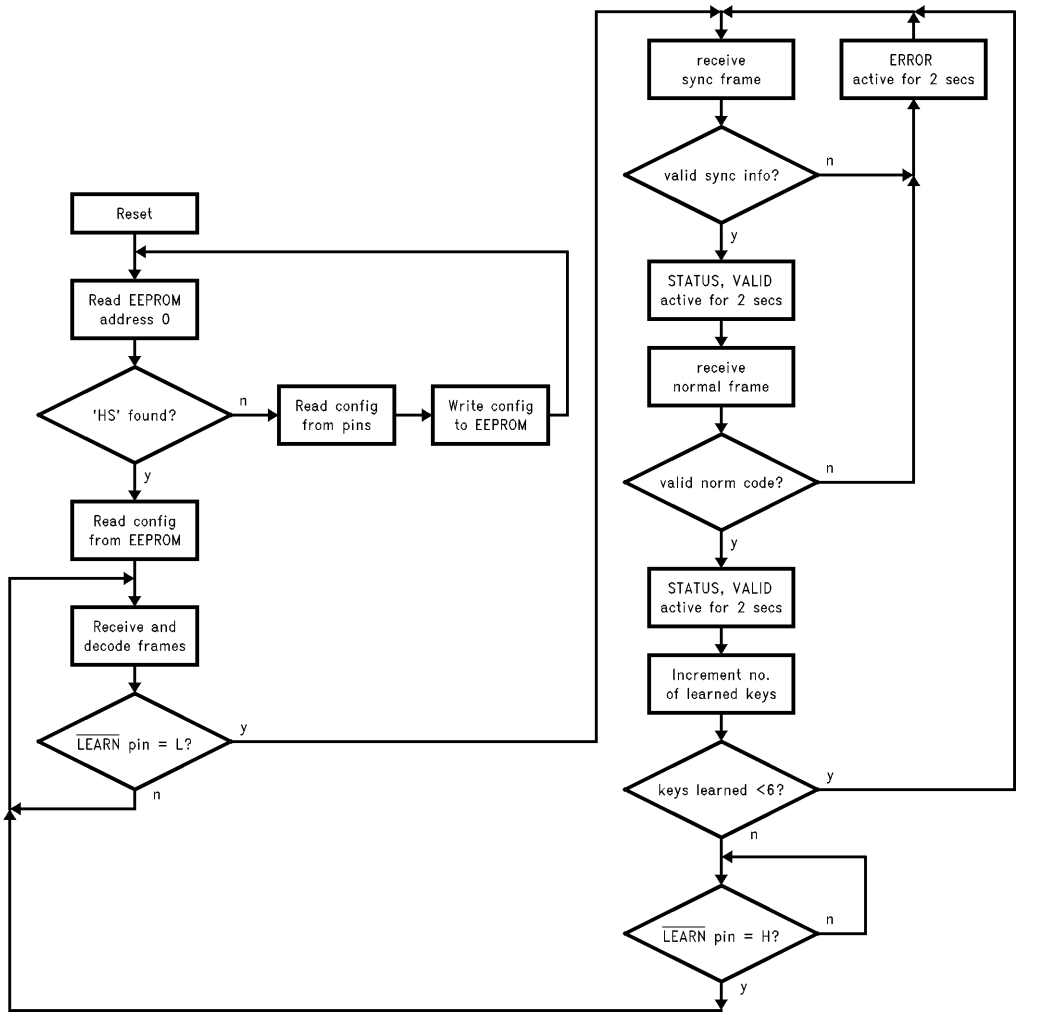
1. Switch on learn mode ($\overline{\text{LEARN}}$ pin to GND).

   The Status LED starts to blink.
2. Reset your transmitter by taking the battery out and putting it in again or holding KEY1 and KEY2 down for at least 6 seconds if this option is enabled.
3. Send the sync information to the receiver. If this was valid sync data the Status LED goes on for about 2 seconds (or as long as the key button is held down). Then the Status LED blinks faster.
4. Push a button on the transmitter again to send a normal frame to the receiver. If it is a valid frame with a correct dynamic code again the Status LEDs goes on for about 2 seconds. Now this key is learned by the receiver and all keys that were learned before are erased.
5. The Status LED blinks slowly again indicating that the receiver expects the next sync frame now. So repeat steps 2 to 4 with your next keys until all keys (max. 6) have been learned.
6. Switch off learn mode ($\overline{\text{LEARN}}$ pin OPEN or to V_{CC}). Now the receiver accepts all the keys that have been learned during this procedure.

Whenever a correct frame is received the Status LED goes on and the $\overline{\text{DATA}}$ output corresponding with the pressed key button toggles its state. If output normal mode has been selected in the configuration the $\overline{\text{DATA}}$ outputs corresponding to the pressed key buttons are activated as long as the key is held down.

Figure 3 illustrates the initialization phase and the learning procedure.

MM57HS0x Flow Chart



TL/D/12600–3

FIGURE 3. Initialization and Learning Procedure of the MM57HS01 Decoder

2.3 Resynchronization Procedure

The transmitter and receiver must be resynchronized if the transmitter battery is replaced, or if the receiver misses more than 256 sequential frames (this would happen if the transmitter is repeatedly activated while out of the receiver's range, for example).

If the receiver and a learned key come out of synchronization because the transmitter has been activated for more than 256 times without the receiver getting those frames or the battery has to be replaced at the transmitter a resynchronization procedure has to be done.

1. Enable resynchronization by turning on the Resync switch ($\overline{\text{RESYNC}}$ pin to GND).
2. Reset the transmitter as described in the learning procedure.
3. Send the sync information to the receiver. If the sync information is correct then the Status LED goes on. Now the key is resynchronized and will be accepted again with the next normal frame.
4. If it is desired to disable automatic resynchronization turn off the Resync switch ($\overline{\text{RESYNC}}$ pin OPEN or connected to V_{CC}).

3.0 HOW TO IMPROVE THE HiSeC SYSTEM

Some fine tuning can be done at the system by using a preprogrammed EEPROM. The following values can be changed: The capture window, the maximum value for the scan protection counter and the low battery detection. This section explains how to prepare an EEPROM for the use with the MM57HS01 or MM57HS02 (Note 1) decoder.

Note 1: For availability please contact the local National Semiconductor Sales Office/Distributor.

Table I shows the contents of the configuration area of the EEPROM. The values in brackets are the defaults set during the first initialization by the decoder. These 4 words (address 0 to 3) have to be prepared to make the HiSeC decoder work correctly. The values in the other cells may be anything.

TABLE I. EEPROM Configuration Contents

Address Word	Contents	
	Highbyte	Lowbyte
0	48 hex, ASCII ''H''	53 hex, ASCII ''S''
1	Max. Value for Scan Protection Counter (30)	Reserved (0)
2	Number of Learned Keys (0)	Capture Window Divided by 16 (16)
3	CONFIG Register (see Table II)	Scan Protection Counter (0)

Customizing the receiver settings using a preprogrammed EEPROM:

- Word 0, HiSeC indicator:
  This cell has to contain ASCII ''H'' and ''S'' to indicate that the EEPROM contains valid HiSeC receiver data.
- Maximum value for scan protection counter:
  If the decoder receives this number of wrong dynamic codes it stops working for about 30 seconds.
  Allowed range: 2–255.
- Number of learned keys:
  Must be set to 0.
- Capture window divided by 16:
  This value times 16 is the maximum number of dynamic codes the decoder calculates forward to find the received dynamic code if the previous frames have not been received. The bigger the capture window size the higher the comfort for the user but the lower the security of the system and the longer the time to calculate the dynamic codes. The decoder can calculate about 250 codes per second.
  E.g. if this value is set to 32 then the capture window is 512 codes and it takes about 2 seconds (worst case) to find the right code or to decide ''wrong code''.
  Allowed range: 1–255.
- CONFIG register:
  This register selects the decoding modes of the receiver. In the above application *(Figure 2)* the following modes are selected by the DATA pins: RF PWM, long frame, rolling code mode and output toggle mode.
  The low battery detect function of the receiver which is always enabled if the EEPROM is initialized by the decoder can be switched off by resetting bit 5 of the CONFIG register. In this case ensure that the CompareEnable bit in the transmitter is also reset because otherwise there will be malfunctions on the receiver if the transmitter sends a low battery signal. All reserved bits must be set to 0.
- Scan protection counter:
  It counts the wrong dynamic codes and is reset when a correct code is received.
  Must be set to 0.

TABLE II. CONFIG Register Contents

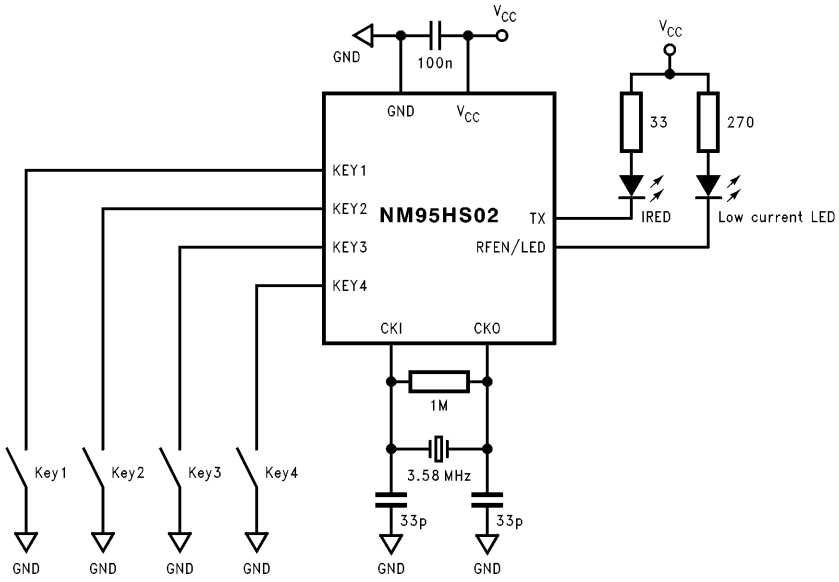
Location	Meaning if Logic ''1''	Meaning if Logic ''0''	Setting in Example Application *(Figure 2)*
0	IR	RF PWM	0
1	Long Frame	Short Frame	1
2	Fixed Code	Rolling Code	0
3	Reserved	Reserved	0
4	Reserved	Reserved	0
5	Low Battery Detect Enabled	Low Battery Detect Disabled	1
6	Output Toggle Mode	Output Normal Mode	1
7	Reserved	Reserved	0

4.0 IR BASED SYSTEM

The HiSeC encoder can also be used in an infrared based system which is normally cheaper than an RF solution and provides even higher security. The IR circuits are similar to the RF circuits. The differences to the RF system are described in the following sections.

4.1 IR Transmitter Design

For infrared transmitters it is recommended to use a resonator clock circuit (see *Figure 4*). So the modulation frequency of the IR signal is very accurate and stable over temperature. This ensures that the IR receiver which usually has a very narrow band width can receive the signal at the maximum sensitivity.



TL/D/12600–4

FIGURE 4. HiSeC IR Transmitter

NM95HS02 EEPROM Array Configuration

```
Bit Settings:
AutoResync:                    1
LEDSEL:                        1        RFEN/LED=LED
BatteryType:                   0
(Low battery detection                  3V      )
TIMEOUTEN:                     1
Pausel: (bit3)                 1
Pause0: (bit2)                 1
FactoryDisableBit:             1        algo protect
WriteDisableBit:               0        clear
PreamblePresent:               0        disabled
SyncType:                      0
SyncPresent:                   1        bitcoded
FixSize:                       1
FixPresent:                    1        24 bits
DynSize:                       1        36 bits
ParityPresent:                 1        enabled
CompareEnable:                 1        enabled
IRSel:                         1
PRSel2:                        0        \
PRSell:                        0         > IR 2, 8 pulses, 33% duty cycle
PRSel0:                        1        /
TxPol:                         1        inverted
SCLK:                          0        PSC 1
Prescaler3: (hex)              0A
Prescaler2: (hex)              0A
Prescalerl: (hex)              09
Dynamic start code: (hex)      xxxxxx
KeyIDCode: (hex)               xxxxxx
SyncFieldCode: (hex)           05
Custom algorithm: (hex)        00

Programming data stream (bytes 0-12 in hex): DE3F98A289xxxxxxxxxxxx0500

( x = hexadecimal digit 0..F )
```

With the CKI frequency of 3.580 MHz these settings result in the following timing values:

Bit length: (mean)	0.670 ms
IR modulation frequency:	30 kHz
IR pulse length (t_{IR}):	269 μs
PauseLength:	54 ms
Time-out length:	44s
Autoresync time:	6s

If the IR receiver has a different center frequency than 30 kHz the timer values have to be changed. If more IR power is needed a driver stage, e.g. a FET, has to be added to provide the IRED with more current. Depending on the driver circuit the bit TxPol has to be set to 0. The polarity is correct when the transmitter stage is inactive between the frames.

4.2 IR Decoder Design

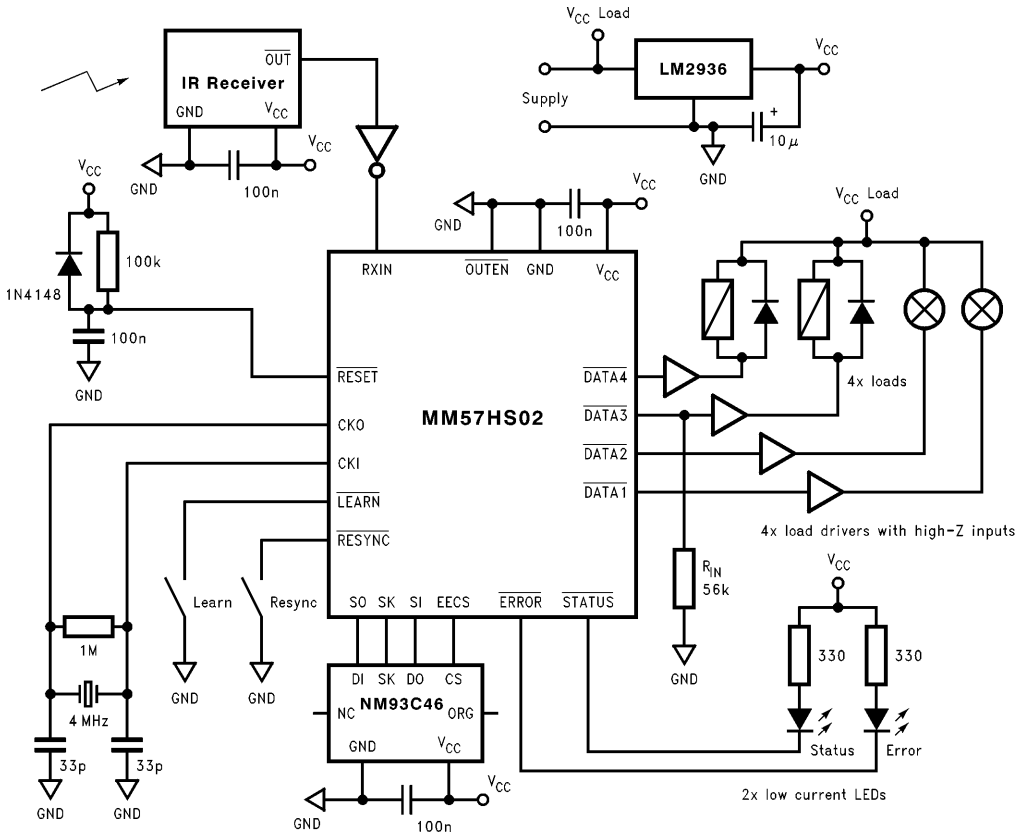
On the decoder side it is recommended to use a MM57HS02 (Note 2) decoder with a 4 MHz crystal clock because this clock frequency ensures that the decoder reads the short IR bits correctly. See *Figure 5* for an example circuit.

Note 2: For availability please contact the local National Semiconductor Sales Office/Distributor.

The R_{IR} is needed to select infrared bit decoding mode when the EEPROM is being initialized on the first power up.

The IR receiver front end shown in the schematic *(Figure 5)* can be an integrated IR receiver module which provides the needed values for the parameter's bandpass center frequency and pulse length.

The load drivers may need additional qualification so that the outputs with pull-down resistors are not activated during reset.



Note 3: For availability please contact the local National Semiconductor Sales Office/Distributor.

FIGURE 5. HiSeC IR Receiver Utilizing MM57HS02 (Note 3) Decoder

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