RS data

DPM I.C's RS 7106, 7126, 7107

Stock numbers 307-862,303-652, 307-143

The RS digital panel meter i.c.'s incorporate all the analogue and digital active circuitry to enable 3½ digit panel meters with auto-polarity and auto-zero to be constructed. The devices also include display decoder/drivers, thus allowing direct interface with 7-segment common anode L.E.D. displays (7107) or a 3½ digit liquid crystal display (7106 & 7126).

The i.c.'s utilise the dual ramp principle which is a technique where the unknown input voltage is used to charge a capacitor for a fixed time. Then, with the unknown disconnected, a reference voltage is used to discharge the capacitor. The time taken to discharge the capacitor is a measure of the unknown voltage. To ensure that the charge and discharge are linear an integrator is used.

Figure 1 **Simplified schematic**

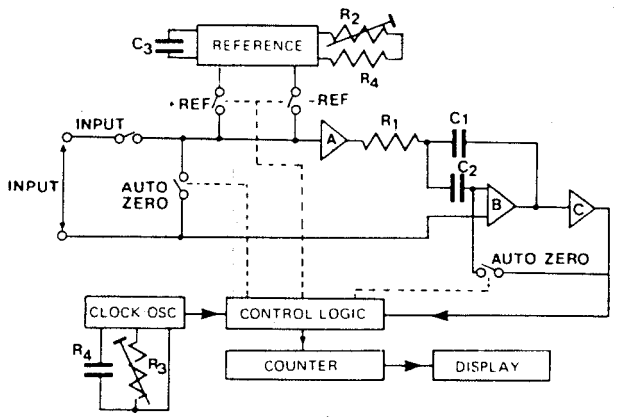


Figure 2 **Pin connections**

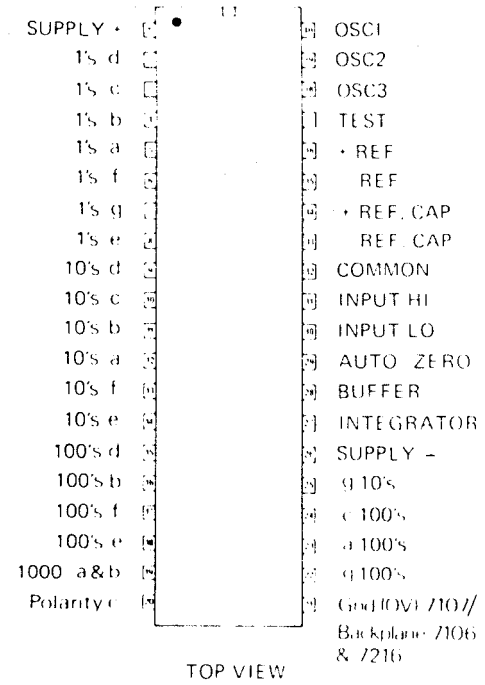


Table 1 – Electronic switch positions

Switch \ State	1	2	3
INPUT	Closed	Open	Open
+ REF	Open	*	Open
- REF	Open	*	Open
AUTO-ZERO	Open	Open	Closed

*+ REF closed for – ve inputs – REF closed for + ve inputs

Initially the control logic sets the electronic switches as shown in table 1, in this mode the unknown input is applied to the integrator, comprising amplifier (B), R1 and C1, via buffer amplifier (A). The integrator output therefore ramps positively or negatively, depending on the input polarity, for a period set by the internal clock oscillator. At the end of this period, state 2 in table 1 is selected, here the input is disconnected and the positive or negative reference connected to the integrator which subsequently begins to ramp towards zero. The comparator (C) determines, during the initial ramp, which reference is selected and also detects that state of zero integrator output. During state 2 the counter accumulates clock pulses until the integrator reaches zero, i.e. comparator (C) changes state. At this point state 3 is selected, here the accumulated count and polarity are displayed giving the unknown input value and the auto-zero mode is selected, this mode short circuits the input and connects capacitor C2 between the buffer amplifier (A) output and short circuited integrator and comparator. Auto-zero capacitor C2 thus charges to a value determined by the offsets appearing at the amplifier outputs and the period of the auto-zero mode; this timing is once again determined by the clock oscillator. Upon completion of auto-zero, state 1 is re-selected thus the whole cycle is repeated. However, the charge on the auto-zero capacitor C2 is subtracted or added to the input voltage thereby correcting any drift in circuit performance. In the event of an input not being applied the auto-zero mode maintains a zero reading by continuous compensation of amplifier drift.

The frequency of the clock oscillator is independent of overall circuit accuracy, however, by selecting a clock frequency such that the initial ramp period is equivalent to or a multiple of the mains period maximum rejection of series mode interference is obtained (see "System Timing" section under Operating Modes).

Absolute maximum ratings

7106 and 7126

Supply voltage (V + to V −) ____ 15V
Analogue input voltage (either input) (Note 1) ____ V + to V −
Reference input voltage (either input) ____ V + to V −
Clock input ____ Test to V +
Power dissipation (Note 2) ____ 800mW
Operating temperature ____ 0°C to + 70°C
Storage temperature ____ −65°C to + 160°C
Lead temperature (Soldering, 60 sec) ____ 300°C

7107

Supply voltage V + ____ + 6V
V − ____ − 9V
Analogue input voltage (either input) (Note 1) ____ V + to V −
Reference input voltage (either input) ____ V + to V −
Clock input ____ Gnd to V +
Power dissipation (Note 2) ____ 800mW
Operating temperature ____ 0°C to + 70°C
Storage temperature ____ − 65°C to + 160°C
Lead temperature (Soldering, 60 sec) ____ 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Note 3: Unless otherwise noted specifications apply to both the 7106, 7126 and 7107 at T_A = 25°C, f_{clock} = 48 kHz, 7106 and 7126 are tested in the circuit of figure 10 using the 200mV version. The 7107 is tested using the 200mV version with external precision voltage reference as figure 9 and figure 3.

Note 4: Refer to "Differential Input" section under Operating Modes.

Note 5: Back plane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate.

Note 6: Does not include LED current for 7107.

Electrical characteristics (Note 3)

Characteristics	Conditions	Min	Typ	Max	Units
Zero input reading	V_{in} = 0.0V Full scale = 200.0 mV	−000.0	±000.0	±000.0	Digital Reading
Ratiometric reading	V_{in} = V_{ref} V_{ref} = 100 mV	999	999/1000	1000	Digital Reading
Rollover error (Difference in reading for equal positive and negative reading near full scale)	$-V_{in}$ = $+V_{in}$ = 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common mode rejection ratio (Note 4)	V_{cm} = ±1V, V_{in} = 0V. Full scale = 200.0mV		50		μV/V
Noise (pk-Pk value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		15		μV
Leakage current @ input	V_{in} = 0V		1	10	pA
Zero reading drift	V_{in} = 0 0°<T_A<70°C		0.2	1	μV/°C
Scale factor temperature /Coefficient	V_{in} = 199.0mV 0<T_A<70°C (Ext. Ref. Oppm/°C		1	5	ppm/°C
Supply current 7106 & 7107 7216	V_{in} = 0 (Note 6) V_{in} = 0		0.8 50	1.8 100	mA μA
Analogue common voltage (with respect to pos. supply)	25kΩ between common & pos. supply (7216 250K)	2.4	2.8	3.2	Volts
Temp. coeff. of analogue common (with respect to pos. Supply)	25kΩ between common & pos. supply (7216 250K)		80		ppm/°C
7106 and 7216 Pk-Pk segment drive voltage (Note 5)	V supply = 9V	4	5	6	Volts
7106 and 7216 Pk-Pk backplane drive voltage (Note 5)	V supply = 9V	4	5	6	Volts
7107 ONLY Segment sinking current (Except Pin 19)	+supply = 5.0V Segment voltage = 3V	5	8.0		mA
7107 ONLY Segment sinking current (Pin 19 only)	+ supply = 5.0V Segment voltage = 3V	10	16		mA

Operating modes

Auto-zero

With the inputs shorted, the display should read zero. The negative sign being displayed about 50% of the time.

Differential input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Differential reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worse case condition. (See "Component Value Selection").

Analogue common

This pin is included primarily to set the common mode voltage for battery operation (7106 and 7126) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analogue common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (0.001%/%), low output impedance (≃15Ω), and a temperature coefficient typically less than 80ppm/°C.

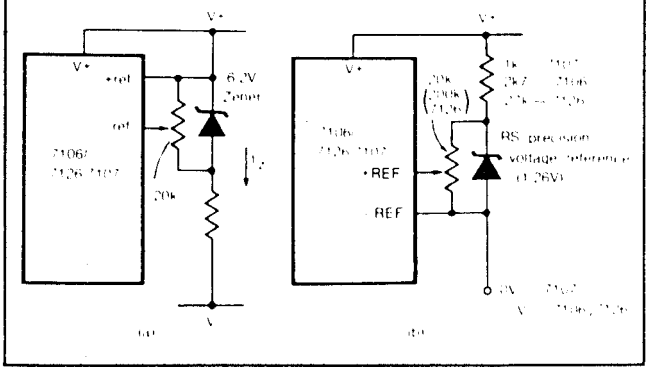
Over-range

Inputs greater than full scale will cause suppression of the three least significant digits, i.e. only 1 or − 1 will be displayed.

Polarity

The absence of a polarity sign indicates a positive input reading. A negative input is indicated by a negative sign.

Figure 3 **Using an external reference.**



The limitations of the on-chip reference should also be recognised, however. With the 7107, the internal heating which results from the L.E.D. drivers can cause some degradation in performance. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106 and 7126 with negligible dissipation, suffer from none of these problems. In all cases, an external reference can easily be added, as shown in figure 3.

(N.B. When an external bandgap reference (1.26V) is used with the 7107, Input − (pin 30) is tied to Analogue common (pin 32) thus establishing the correct common mode voltage. If Analogue common is not shorted to Digital ground (pin 21), the input voltage may float with respect to the power supply if Analogue common is shorted to ground, the input is single ended (referred to supply ground).

Analogue common is also the voltage the input returns to during auto-zero and de-integrate. If signal low is different from analogue common, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications input low will be set at a fixed known voltage (power supply common for instance). In this application, analogue common should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analogue common, it should be since this removes the common mode voltage from the reference system.

(N.B. When using the internal reference analogue common must not be connected to 0_V or ground)

Within the i.c., analogue common is tied to an N channel FET that can sink 30mA (100μA 7126) or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA (1μA 7126) of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The test pin serves two functions. On the 7106 and 7126, it is coupled to the internally generated digital ground through a 500Ω resistor (digital ground is set at approximately 5V below +V). Thus, when operated from a single battery supply, test can be used as the 0v rail for externally generated segment drivers, such as decimal points (or any other presentation the user may want to include on the LCD display), or it may be used as a common mode reference level to ensure compatibility with most op amps. Figure 8 shows such an application.

When the 7106 is operated from a ±5V supply and external digital circuitry is required, the test pin should be connected to 0v. (N.B. the test function can only be implemented in this case by use of a S.P.D.T. switch). The second function is a "lamp test". When test is pulled high (to + supply) all segments will be turned on and the display should read −1888. Caution: on the 7106 and 7126, in the lamp-test mode, the segments have a constant d.c. voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.

System timing

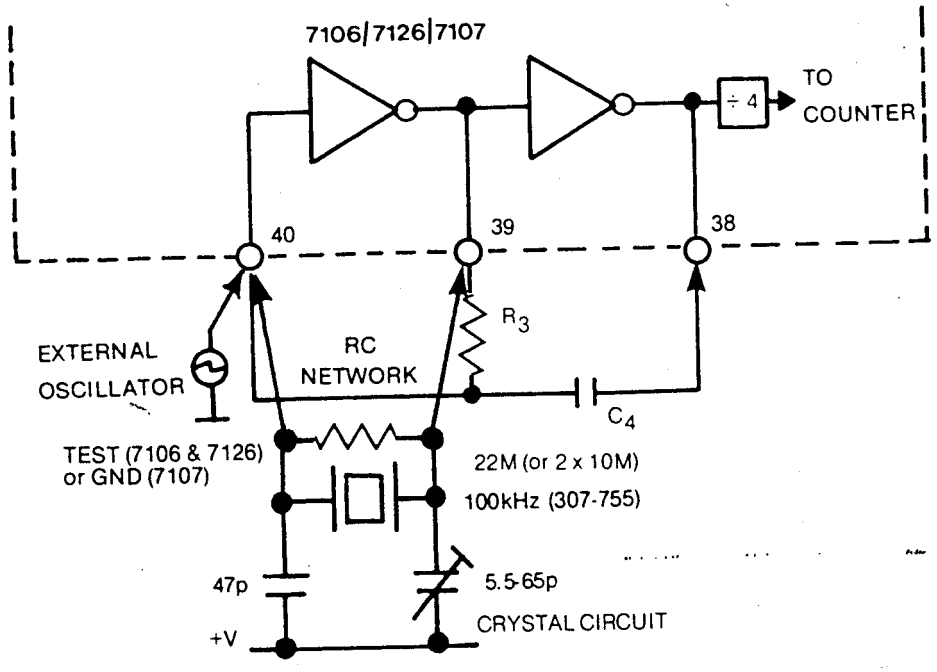
Figure 4 shows the clocking arrangements used in the 7106, 7126 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal circuit between pins 39 and 40.
3. An R.C. oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 50 Hz pickup, the signal integrate cycle should be a multiple of 20 ms. Oscillator frequencies of 200kHz, 100kHz, 66⅔ kHz, 50kHz, 40kHz etc would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

Figure 4 **Clock circuits**



Component value selection

(7126 values shown in brackets).

Integrating resistor (R_1)

Both the buffer amplifier and the integrator have a class A output stage with 100μA (6μA) of quiescent current. They can supply 20μA (1μA) of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470k (IM8) is near optimum and similarly a 47k (180k) for a 200.0 mV scale.

Integrating capacitor (C_2)

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). When the analogue common is used as a reference, nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analogue common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings second (50kHz clock), nominal values for C_1 are 220n 7106, 100n 7107 and 47n 7126. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is to have low dielectric absorption to prevent roll-over errors. Polypropylene and polycarbonate capacitors are suitable for this application.

Auto-zero capacitor (C_2)

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise is very important, a 470n (330n) capacitor is recommended. On the 2 volt scale, a 47n (22n) capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference capacitor (C_3)

A 100n capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analogue common) and a 200 mV scale is used, a larger value is required to prevent roll-over error. Generally 1μ will hold the roll-over error to 0.5 count in this instance.

Oscillator components (R_3 & C_4)

For all ranges of frequency a 100k (200k) resistor is recommended and the capacitor is selected from the equation $f = \frac{0.45}{R_3 C_4}$. For 48kHz clock (3 readings/second), $C_4 \simeq$ 100p (50p).

Reference voltage

The analogue input required to generate full-scale output (2000 counts) is: $V_{in} = 2V_{ref}$. Thus, for the 200.0 mV and 2.000 volt scale, V_{ref} should equal 100.0mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select V_{ref} = 0.341V. Suitable values for integrating resistor and capacitor would be 120k and 220n 7106, 120k and 100n 7107, 330k and 47n 7126. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for Vin ≠ 0. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between input high and common and the variable (or fixed) offset voltage between common and input low.

7107 Power supplies

The 7107 is designed to work from ±5 volt supplies. (N.B. It is recommended to decouple the supplies with two 10μ capacitors).

However, if a negative supply is not available, it can be generated from the clock output as shown in figure 5.

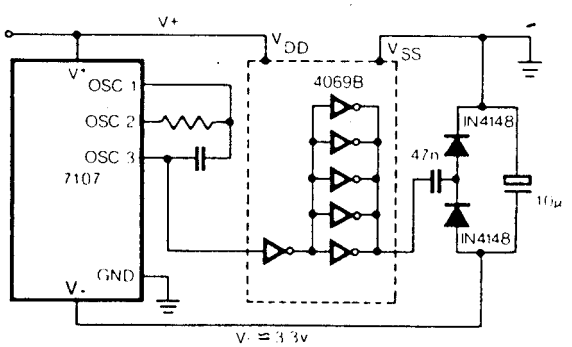
In fact, in selected applications no negative supply is required. The conditions to use a single + 5V supply are:

1. The input signal can be referenced to the centre of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

7106 and 7126 Supplies

The 7106 and 7126 may be operated from either a battery source, or from a mains system derived supply. The latter should be ±5V. The 0v may be connected to the test pin, if external circuitry is required, and also be used as a ground reference for the input. (See Test and Analogue sections).

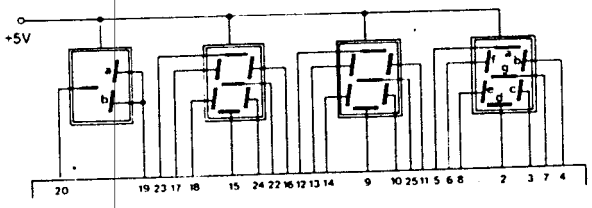
Figure 5 **Generating negative supply from + 5v**



Displays

7107: Common Anode to +5V
7106 and 7126 Backplane to Pin 21

Figure 6 **Display connections 7107**



Note 0.3 in. Common Anode L.E.D. displays are available for direct driving from the 7107 and 3½ digit L.C.D. displays for use with the 7106 and 7126. Please refer to current catalogue. (See figure 8 for method of driving L.C.D. decimal points).

Figure 7 **Display buffering for increased drive current. Requires four RS 7407 hex buffers. Each buffer is capable of 40 mA max.**

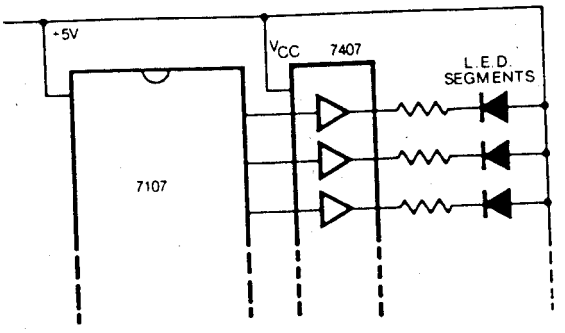
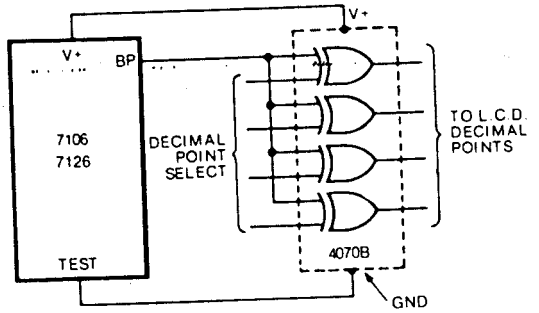


Figure 8 **Exclusive "OR" gate for decimal point drive of liquid crystal display. (See test function)**



External components

Figure 9 **7107 using the internal reference. INPUT — may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See "Analogue Common section under operating modes).**

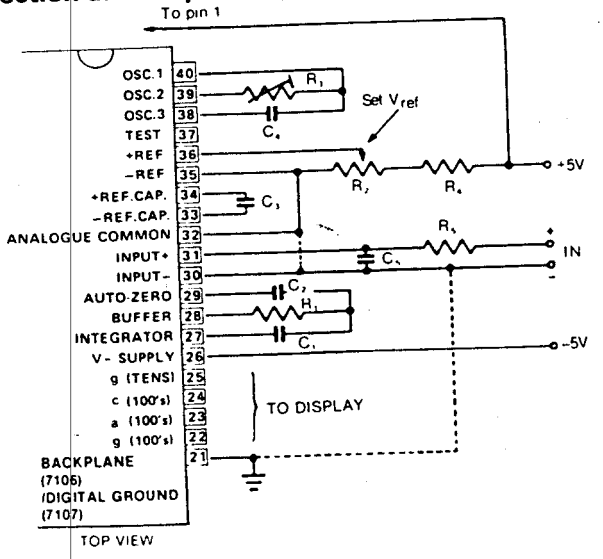
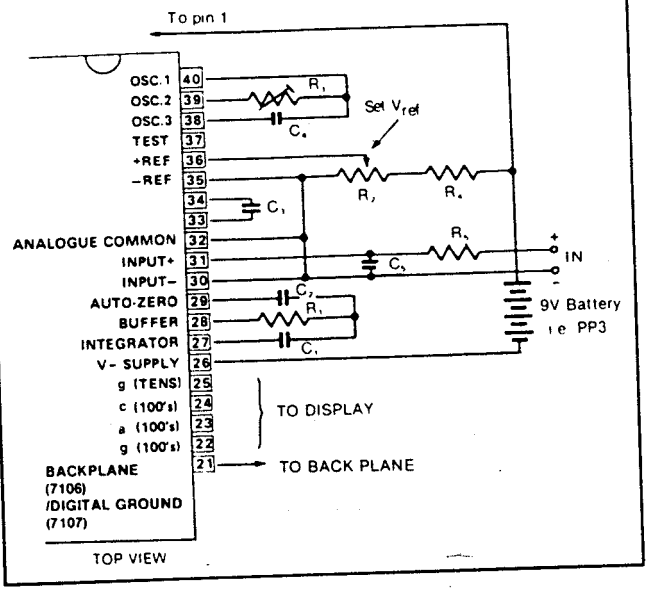


Figure 10 **7106/7126 using the internal reference and a floating supply voltage (9V battery).**



Component values

	7106 and 7107		7126	
	200 mV F.S.R.	2V F.S.R.	200 mV F.S.R.	2V F.S.R.
R_1	47K	470K	180K	IM8
R_2	1K	20K	10K	250K
R_3	100K preset	100K preset	200K	200K
R_4	22K	22K	240K	240K
R_5	1M	1M	1M	1M
C_1	220n 7106, 100n 7107	220n 7106, 100n 7107	47n	47n
C_2	470n	47n	330n	22n
C_3	100n	100n	100n	100n
C_4	100p	100p	50p	50p
C_5	10n	10n	10n	10n

Use 2% 0.5W metal oxide resistors and cermet presets. Capacitors should ideally be 160V polyarbonate except C_4 which should be silvered mica.

Input filters

Due to the extremely low input leakage current, typically 1pA at 25°C, the errors caused by high impedance passive filters on the input are minimal. The simple R.C. filter consisting of R5(IM) and C5(10n) introduces a negligible 1μV error.

Input protection

As stated in note 1 in the maximum ratings section, the input voltage may exceed the supply voltages providing that the input current to the IC is limited to ±100μA. If the D.V.M. IC is used in the single ended input mode, the 1M ohm input filter resistor is sufficient to give protection up to at least ±100V. If the device is to be used in the differential input mode the 1M ohm resistor in the non-inverting input line should be changed to 470K and another 470K added to the inverting input line, this will then give protection to at least ±100V as before. In some cases an input attenuator, if used, may form part of the input protection.

A.C. Voltage measurements

Measuring A.C. voltages requires the voltage to be first rectified before applying to the D.P.M. To achieve this a precision rectifier is used as shown in figure 12. Here the use of an operational amplifier gives a D.C. voltage proportional to the R.M.S. value of the A.C. input. This is only true for sinewaves as any harmonic content will introduce significant errors.
Apply the output to the D.P.M. differential inputs pins 30 and 31.

Figure 11 **Input protection**

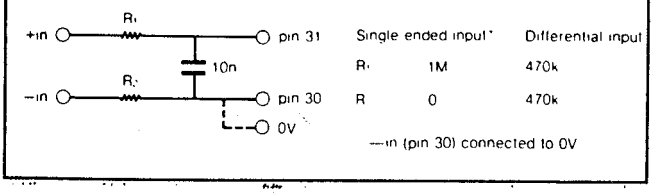
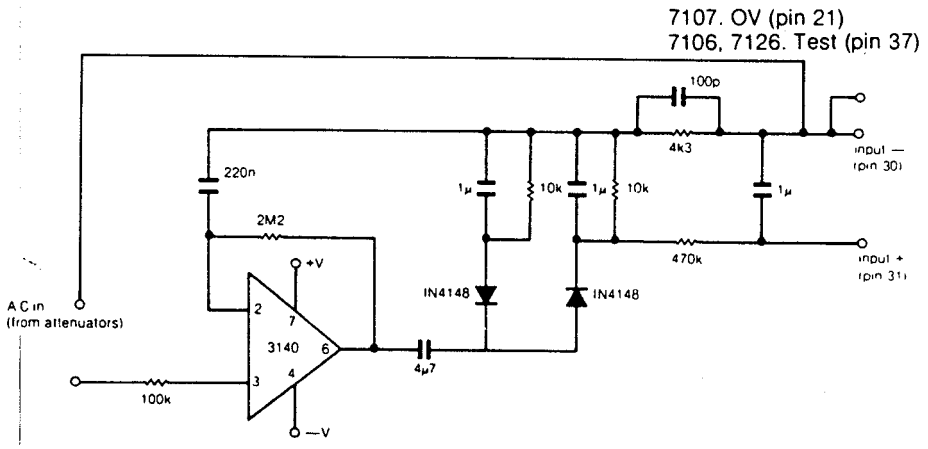


Figure 12 **A.C. Rectifier**



N.B. DPM 200mV range.
Analogue common not connected to input−
Test decoupled to supplies by 10μF capacitors

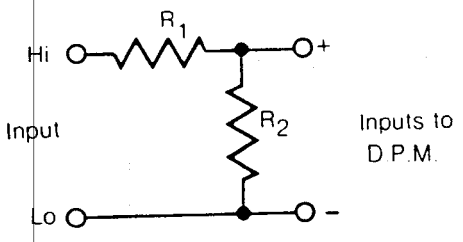
RS data

Input attenuators

When it is required to measure voltages in excess of the maximum, i.e. 2V F.S.D. the input voltage must first be attenuated. In this instance a reduction in input resistance should be expected.

To maintain a reasonably constant attenuation, without serious loss in reading accuracy due to loading effects, the attenuator input resistance is usually selected to lie between 1M and 10M. Figure 13 shows the method of calculating resistor values and figure 14 gives suggested component values.

Figure 13 **Input attenuators**

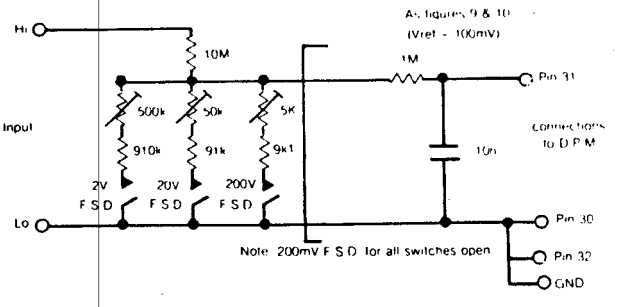


$\frac{R2}{R1 + R2}$ = Attenuation ratio

for 10:1	for 100:1	for 1000:1
$R_2 = \frac{R_1}{9}$	$R_2 = \frac{R_1}{99}$	$R_2 = \frac{R_1}{999}$

Input resistance = $R_1 + R_2$

Figure 14 **Input attenuation – suggested values**



Current measurements

Measurement of A.C. or D.C. current can be achieved by measuring the voltage drop across a known resistor which is placed in series with the circuit under test. Depending on the range selected, i.e. 200mV or 2V the voltage drop across the resistor can be determined by Ohms law:

V drop = I.R. where R = known resistor value
I = current to be measured
V drop = subsequent voltage drop

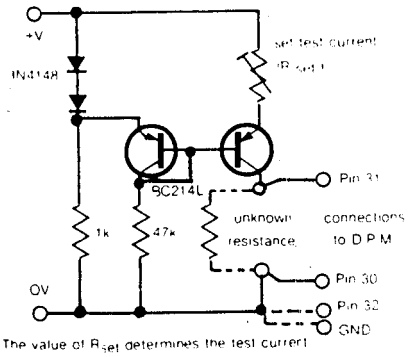
Take care not to exceed the power dissipation of the resistor.

Resistance measurements

To measure the unknown value of a resistor a defined current is passed through the resistor and the resultant potential difference is measured. The current is obtained from a constant current source. A typical circuit to achieve this is shown in figure 15. The approximate values of Rset are shown in the table.

Figure 15 **Resistance converter — set D.P.M. to 2V (F.S.D.) (For use with dual rail supplies)**

I test	R_{set}	Meter F.S.D
10mA	200R	200R
1mA	2k	2k
100µA	20k	20k
10µA	200k	200k



The value of R_{set} determines the test current