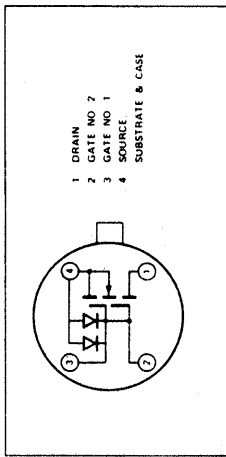


UHF AND GENERAL PURPOSE RF APPLICATIONS

DESCRIPTION

The Signetics D-MOS SD300 and SD301 are dual gate silicon insulated field effect transistors of the N-channel enhancement mode type. They are fabricated by a new principle which gives superior high frequency performance up to 2 GHz. Special diodes are connected between the two gates and the case. These diodes bypass any voltage transients which lie outside the range of -0.3 volts to +25.0 volts. Thus, the gates are protected against damage in all normal handling and operating situations. The device attributes make them ideally suited for a variety of high frequency amplifier and mixer applications. The presence of two gates plus the incorporation of the drift region in the structure, has allowed us to reduce feedback capacity, C_{rss} to 0.02 pF typ. A wide AGC capability plus a significant reduction in cross modulation is now available because of the inherent linearity of the devices. The SD300 and SD301 are hermetically sealed in a modified 4 lead TO-72 package.

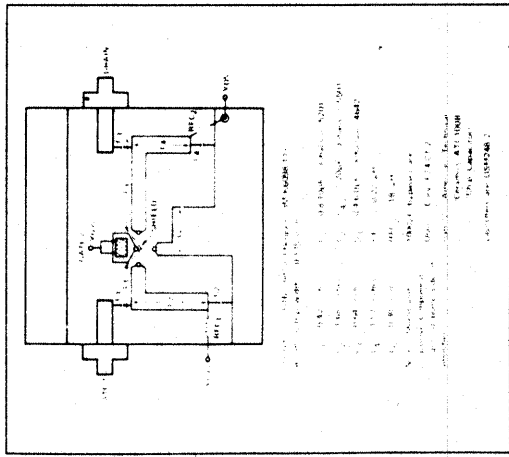
PIN CONFIGURATION (Bottom View)



ABSOLUTE MAXIMUM RATING

($T_A = 25^\circ\text{C}$ unless otherwise specified)
 Drain-to-source voltage (VDS) +25V (max)
 Gate No. 1-to-source voltage (VG1S) -0.3 to +25V dc
 Gate No. 2-to-source voltage (VG2S) -0.3 to +25V dc
 Drain current (I_D) 50 mA (max)
 Ambient temperature range (T_A)
 Storage -65°C to +175°C
 Operating -65°C to +125°C
 Transistor Dissipation (P_T) 300mW
 At 25°C case temperature
 Temperature above 25°C derate at 2.0mW/°C

TEST FIXTURE



FEATURES

- LOWER CROSS-MODULATION AND WIDER DYNAMIC RANGE THAN BIPOLAR OR SINGLE GATE FETs.
- REVERSE AGC CAPABILITY.
- LINEAR MIXING CAPABILITY.
- DIODE PROTECTED GATES.
- HIGH FORWARD TRANSDUCANCE $g_{fs} = 10,000 \mu\text{mhos}$ (typ.).
- HIGH GAIN THROUGH UHF RANGE (13 dB typ. AT 1 GHz).
- LOW NOISE THROUGH UHF RANGE (6 dB typ. FOR SD301 AT 1 GHz).
- LOW INPUT CAPACITANCE (2.0 pF typ.).
- LOW FEEDBACK CAPACITANCE (0.02 pF typ.).
- LOW OUTPUT CAPACITANCE (0.6 pF typ. FOR SD301).
- ION IMPLANTED.
- POSITIVE BIAS ONLY.

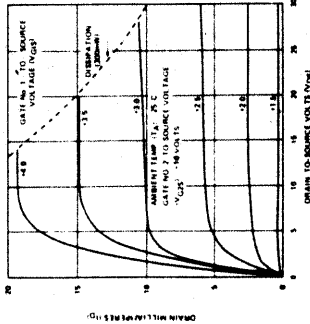
ELECTRICAL CHARACTERISTICS SD300, SD301 at 25°C

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain to Source Breakdown	BVDS	$V_{G1S} = V_{G2S} = 0V, I_D = 5\mu A$	+25	+30		volts
Gate 1 Leakage Current	IG1SS	$V_{G1S} = +5V, V_{G2S} = V_D = 0V$	0.001		0.1	μA
Gate 2 Leakage Current	IG2SS	$V_{G2S} = 10V, V_{G1S} = V_D = 0V$	0.001		0.1	μA
Drain to Source Leakage Current	ID (off)	$V_{DS} = +15V, V_{G1S} = V_{G2S} = 0V$		0.001	1.0	μA
Zero Bias Drain Current	IDSS					
Gate 1 Threshold Voltage	V _{T1}	$V_{DS} = V_{G1S} = V_{T1}$ $V_{G2S} = +10V$ $I_D = 1\mu A$	+0.1	+0.5	+2.0	volts
Gate 2 Threshold Voltage	V _{T2}	$V_{DS} = V_{G2S} = V_{T2}$ $V_{G1S} = +4V$ $I_D = 1\mu A$	+0.1	+0.5	+2.0	volts
Small Signal Short Circuit Capacitances						
Gate 2 A.C. Grounded Input	C _{iss}	$V_{DS} = +15V, V_{G1S} = +4V,$ $V_{G2S} = +10V, I_D = 18mA$ $f = 1 \text{ MHz}$		2.0	2.5	
Output	C _{oss}	$V_{DS} = +15V$ SD300 $V_{G2S} = +10V$ SD301 $f = 1 \text{ MHz}$		1.0	1.2	pF
Reverse Transfer	C _{rss}	$V_{DS} = +15V, V_{G2S} = +10V$ $f = 1 \text{ MHz}$		0.6	0.8	
Forward Transconductance	g _{fs}	$V_{DS} = +15V, V_{G1S} = +4V$ $V_{G2S} = +10V, I_D = 18mA$	8.0	10.0		mmhos
Power Gain*	G _{ps}	$V_{DS} = +15V,$ SD300 $V_{G1S} = +4V,$ SD300 $V_{G2S} = +10V$ SD301 $I_D = 18mA$	9.0	13.0		dB
Noise Figure*	NF	$f = 1 \text{ GHz}$ SD300 SD301	8.0	9.0	7.0	
Power Gain	G _{ps}	$V_{DS} = +15V,$ SD300 $V_{G1S} = +4V,$ SD300 $V_{G2S} = +10V,$ SD301 $I_D = 18mA$	22	24		dB
Noise Figure	NF	$f = 200 \text{ MHz}$ SD300 SD301	2.0	3.0	3.0	dB
Interfering Signal Level at Gate for 1% Cross Modulation Distortion, Peak Voltage	E _{int}	$V_{DS} = V_{G2S} = +15V$ $I_D = 18mA$ Wanted Signal $f = 500 \text{ MHz}$ Interfering Signal $f = 501 \text{ MHz}$		200		mV
Range of Automatic Gain Control	AGC (VG2S)	$V_{DS} = +15V, V_{G1S} = +4V$ $f = 500 \text{ MHz}$		40		dB
Drain to Source on Resistance	r _{DS (on)}	$V_{G1S} = +5V, V_{G2S} = +10V,$ $I_D = 0.1mA$		90	130	Ω rms

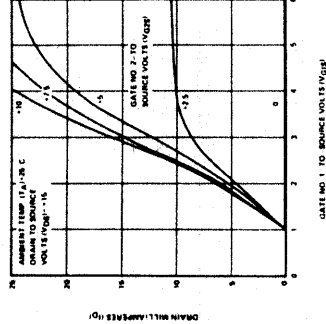
CHARACTERISTIC CURVES

PERFORMANCE CURVES

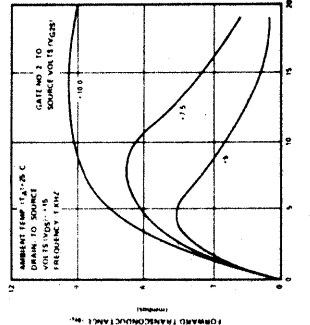
DRAIN CURRENT VERSUS DRAIN-TO-SOURCE VOLTAGE



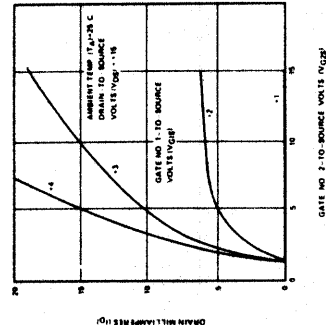
DRAIN CURRENT VERSUS GATE NO. 1-TO-SOURCE VOLTAGE



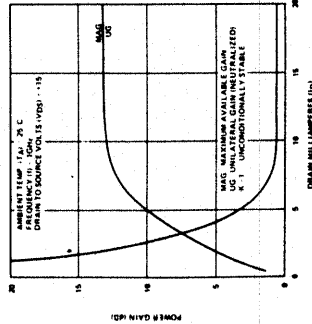
1 KHZ FORWARD TRANSCONDUCTANCE VERSUS DRAIN CURRENT



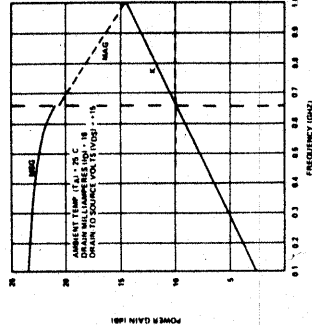
DRAIN CURRENT VERSUS GATE NO. 2-TO-SOURCE VOLTAGE



POWER GAIN VERSUS DRAIN CURRENT

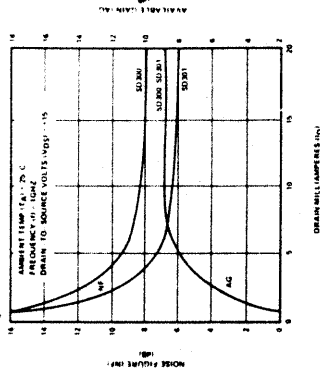


POWER GAIN VERSUS FREQUENCY

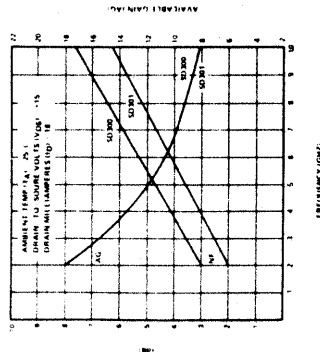


CHARACTERISTIC CURVES (Cont'd)

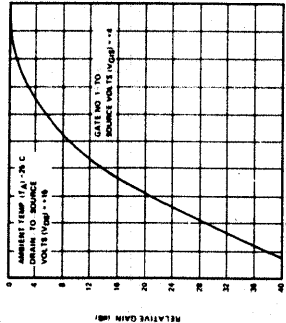
NOISE FIGURE AND AVAILABLE GAIN VERSUS DRAIN CURRENT



NOISE FIGURE AND AVAILABLE GAIN VERSUS FREQUENCY

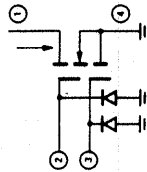


AUTOMATIC GAIN CONTROL RANGE AT 500 MHZ



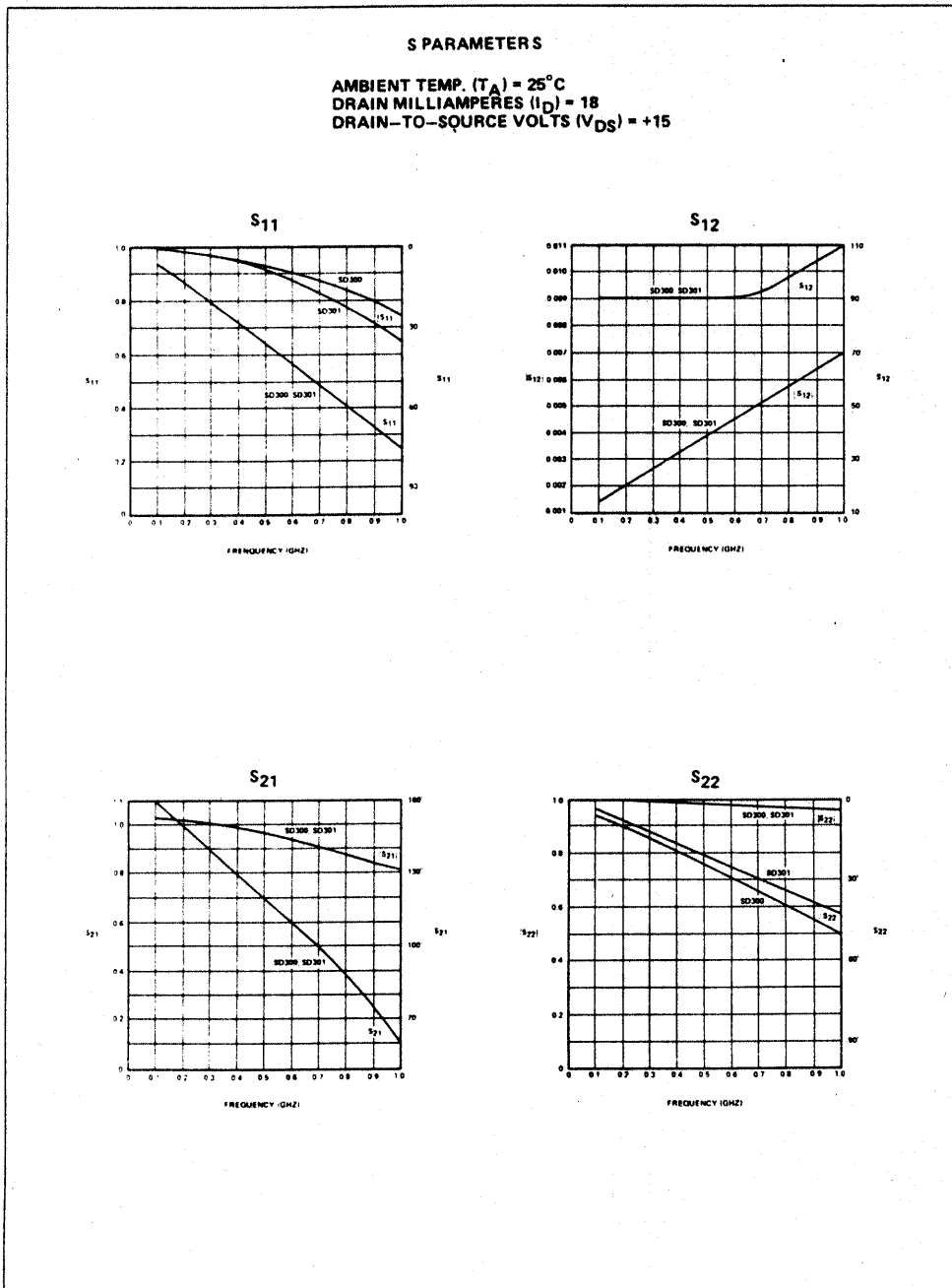
DUAL GATE CASCODE BIAS SCHEME

SD 300/301



- *VGS = 0 - +28 VOLTS
- *VGS = 0 - +4 VOLTS
- *VGS = 0 - +10 VOLTS
- *IGS = 0 - +20mA

CHARACTERISTIC CURVES



DESCRIPTION

The Signetics D-MOS SD300 insulated field effect transistor is an enhancement mode type. It is a common source principle which gives superior performance up to 1 GHz. Specified for operation between the two gates and the drain and source, it is capable of handling any voltage transients which limit the drain to +25.0 volts. Thus, it is suitable for use in all normal situations. The device attributes are: wide AGC capability plus a significant modulation is now available. The device is sealed in a modified 4 lead TO-18 package.

FEATURES

- LOWER CROSS-MODULATION THAN OTHER DUAL GATE FETs.
- REVERSE AGC CAPABILITY.
- LINEAR MIXING CAPABILITY.
- DIODE PROTECTED GATES.
- HIGH FORWARD TRANSCONDUCTANCE (10,000 μ mhos (typ.)).
- HIGH GAIN THROUGH VHF BANDS (500 MHz).
- LOW NOISE THROUGH VHF BANDS (500 MHz).
- LOW INPUT CAPACITANCE.
- LOW FEEDBACK CAPACITANCE.
- LOW OUTPUT CAPACITANCE.
- ION IMPLANTED.
- POSITIVE BIAS ONLY.

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise specified)
 Drain-to-Source Voltage (V_{DS})
 Gate No. 1-to-Source Voltage (V_{G1})
 Gate No. 2-to-Source Voltage (V_{G2})
 Drain Current (I_D)