National Semiconductor



# TBA950-2 Television Signal Processing Circuit

## General Description

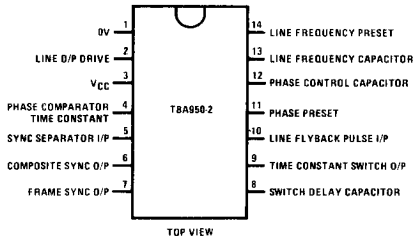
The TBA950-2 is a monolithic integrated circuit for pulse separation and line synchronization in TV receivers with transistor output stages.

The TBA950 comprises the sync separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity, the line oscillator with frequency range limiter, a phase control circuit and the output stage.

It delivers prepared frame sync pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration, few external components are needed.

## Connection and Block Diagrams

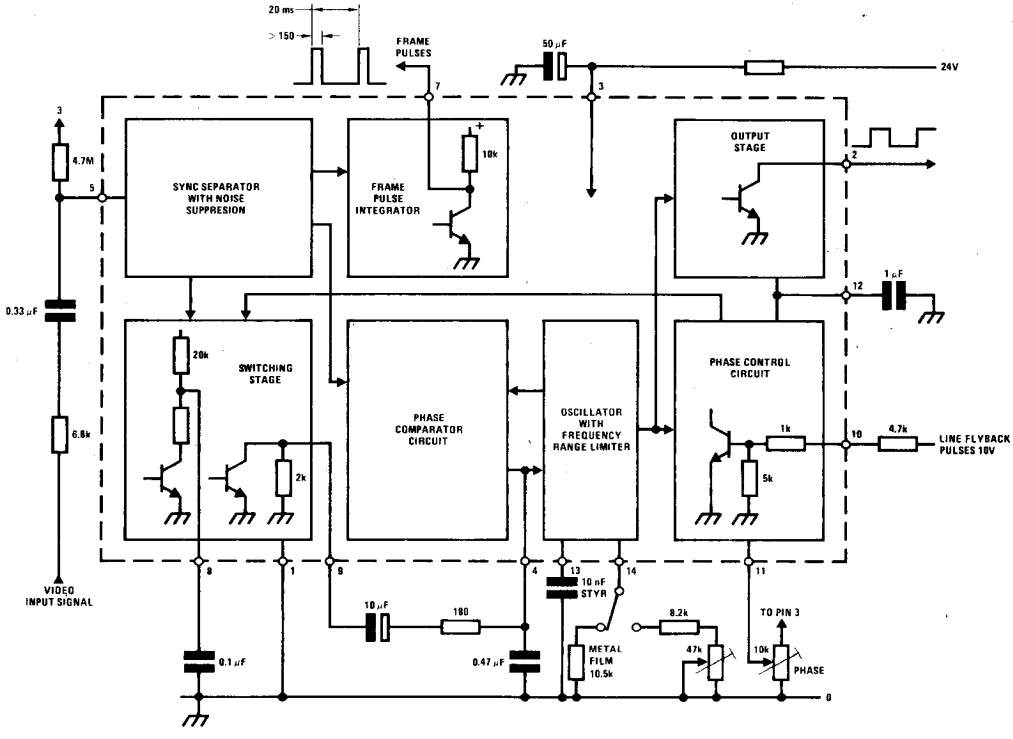
**Dual-In-Line Package**




TOP VIEW

**Dual-In-Line Package, Order Number TBA950-2**
**See NS Package N14A**

**Quad-In-Line Package, Order Number TBA950-2Q**
**See NS Package N14C**



## Absolute Maximum Ratings

**All voltages are referred to pin 1**

| | |
|---|---|
| $I_3$, Supply Current *(Figure 6)* | 45 mA |
| $I_5$, Input Current | 2 mA |
| V5, Input Voltage | −6V |
| $I_2$, Output Current | 22 mA |
| V2, Output Voltage | 12V |
| $I_8$, Switch-Over Current for Video Recording | 5 mA |
| $I_{10}$, Flyback Peak Pulse Current | 5 mA |
| V11, Phase Correction Voltage | 0 to V3 |
| $T_A$, Ambient Temperature | 60°C |

## Recommended Operating Conditions

**(For operating circuits *Figures 4 and 5*)**

| | |
|---|---|
| $I_5$, Input Current During Sync Pulse | >5 μA |
| $V_{IN}$ p-p, Composite Video Input Signal | 3 (1 to 6)V |
| $I_{10}$, Input Current During Line Flyback Pulse | 0.2 to 2 mA |
| $I_8$, Switch-Over Current | >2 mA |
| $t_d$, Time Difference Between the Output Pulse at Pin 2 and the Line Flyback Pulse at 10 | <20 μs |
| $I_3$, Current Consumption *(Figure 6)* | ≤45 mA |
| $T_A$, Ambient Operating Temperature Range | 0°C to +60°C |

## Electrical Characteristics

$T_A = 25°C$, $f_o$ = 15,625 Hz in the test circuit *Figure 2* (Note 1)

| SYMBOL | CHARACTERISTIC | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| V7 | Amplitude of the Frame Pulse | | | >8 | | V |
| t7 | Frame Pulse Durations | | | >150 | | μs |
| $R_{OUT\ 7}$ | Output Resistance at Pin 7 (High State) | | 7.5 | 10 | 13 | kΩ |
| t2 | Output Pulse Duration | Typical Ranges | 25 | | 28 | μs |
| V2 Res | Residual Output Voltage | $I_2$ = 20 mA | | <0.55 | | V |
| $f_o$ | Oscillator Frequency | C13/1 = 10 nF, R14/1 = 10.5 kΩ | 14063 | 15625 | 17187 | Hz |
| $\pm\Delta f_F$ | Frequency Pull-In Range | | 400 | | 1000 | Hz |
| $\pm\Delta f_H$ | Frequency Holding Range | Typical Ranges | 400 | | 1000 | Hz |
| $df_o/dt_d$ | Slope of Phase Comparator Control Loop | | | 2 | | kHz/μs |
| $dt_d/dt_p$ | Gain of Phase Control | | | 20 | | |
| $t_p$ | Phase Shift Between Leading Edge of Composite Video Signal and Line Flyback Pulse (Note 2) Adjustable by V11 | Typical Range | 0 | | 3.5 | μs |

**Note 1:** By modification of the frequency-determining network at pins 13 and 14, these ICs can also be used for other line frequencies.
**Note 2:** The limited flyback pulse should overlap the video signal sync pulse on both edges.

## Functional Description

The sync separator separates the synchronizing pulses from the composite video signal. The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The *RC* network, hitherto required between sync separator and frame oscillator is no longer needed. Since the frame sync pulse duration at pin 7 is subject to production spreads, it is recommended to use the leading edge of this pulse for triggering.

The frequency of the line oscillator is determined by a 10 nF polystyrene capacitor at pin 13 which is charged and discharged periodically by 2 internal current sources. The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulses. Simultaneously, an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e.g., due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync pulse on both edges *(Figure 3)*.

## Functional Description (Continued)

The switching stage has an auxiliary function. When the 2 signals supplied by the sync separator and the phase control circuit, respectively, are in synchronism, a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin 9. Thus the time constant of the filter network at pin 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50 Hz. This arrangement ensures disturbance-free operation.

For video recording operation, this automatic switchover can be blocked by a positive current fed into pin 8, e.g., via a resistor connected to pin 3. It may also be useful to connect a resistor of about 680 Ω or 1 kΩ between pin 9 and earth. The capacitor at pin 4 may be lowered, e.g., to 0.1 μF. These alterations do not significantly influence the normal operation of the IC and thus do not need to be switched.

The output stage delivers at pin 2 output pulses of duration and polarity suitable for driving the line driver stage. If the supply voltage goes down (e.g., by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to V3 = 4V and shuts off when V3 falls below 4V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V3 reaches 4.5V. In the range between V3 = 4.5V and full supply the shape and frequency of the output pulses are practically constant.

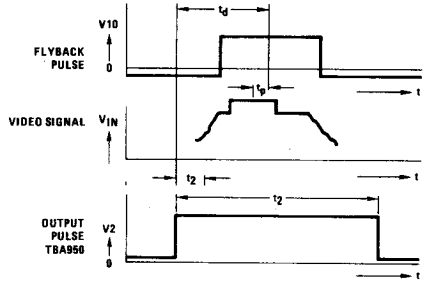
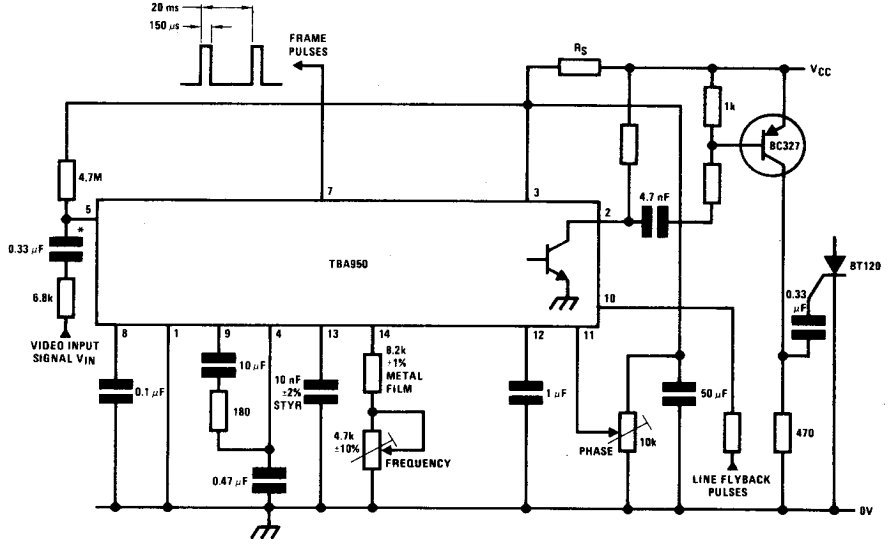


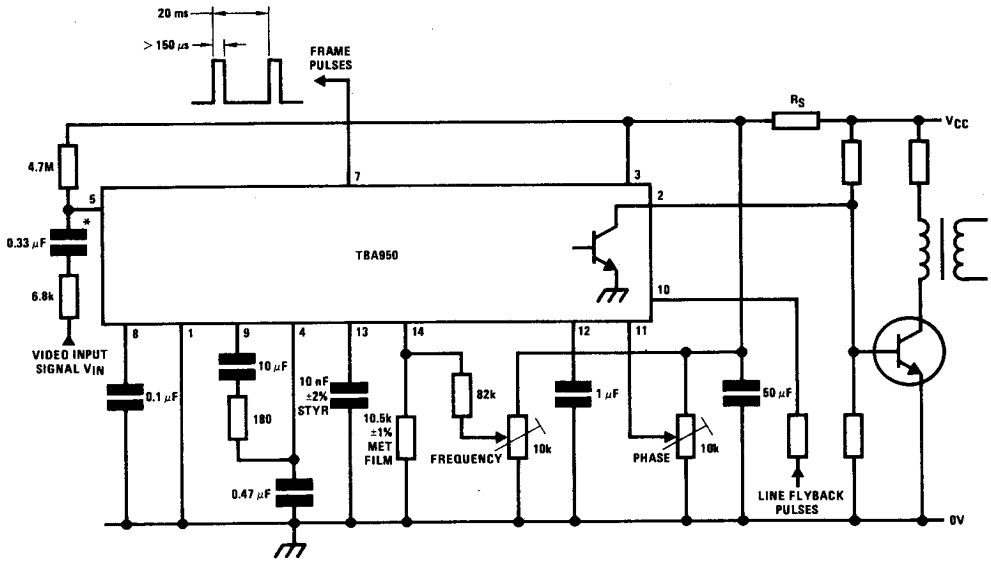

FIGURE 3. Phase Relationships




*Input circuitry must be optimized

FIGURE 4. Operating Circuit (Thyristor Output Stage)

## Functional Description (Continued)




*Input circuitry must be optimized

**FIGURE 5. Another Possibility for Line Frequency Adjustment (Transistor Output Stage)**

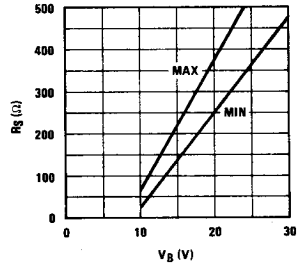



**FIGURE 6. Graph for Determining the Supply Series Resistor, $R_S$**