

**PC68HC16V1**  
**DEVICE INFORMATION**  
**(Issue 2 - 7/28/94)**  
**Rev. 0 Silicon**  
**F33P Mask Set**

The following information and errata pertain to Revision 0 samples of the 68HC16V1 microcontroller. This revision contains the following module versions: CPU16/V8, GRIM/V3, GPT/V2, QSM/V9. The phrase “This is an erratum” identifies characteristics of the current silicon which are expected to be improved. “This is information only” refers to enhancements, clarifications, and changes to the documented descriptions of the microcontroller and the modules within.

**MODULE DETAILS:**

**CPU16:58 Mod Date: 8/5/94 CPU16:** Yield fallout may result from failure of the Sign Latch (SL) bit. When an RMAC or MAC instruction occurs the SL should get affected on an overflow only. In some cases, the SL bit is affected even though an overflow has not occurred. The SL bit is only readable by doing either a PSHMAC or PULMAC instruction following an RMAC or MAC instruction. This is an erratum.

**CPU16:58 WORKAROUND:** Do not rely on correct operation of the SL bit during MAC and RMAC operations.

**CPU16:59 Mod Date: 7/12/94 CPU16:** When entering BDM upon execution of a BGND instruction, FREEZE is asserted prior to the DSI/IPIPE1 signal becoming an input. This means that an external development system could be driving DSI while the MCU is still driving IPIPE1. The problem does not exist when entering BDM via a Breakpoint. This is information only.

**CPU16:59 WORKAROUND:** Delay driving DSI from the development system for approximately 1 clock after the assertion of FREEZE.

**GRIM:050 Mod Date: 8/3/94 GRIM:** While in Non Mux Mode and show cycles are enabled, access to internal address causes a show cycle. If the internal cycle address is inside a memory map specified by a Chip Select as a MUX zone the GRIM does not generate a Non Mux mode SHOW cycle. This is an erratum

**IM:95 Mod Date: 7/20/94 INTEGRATION:** Under certain conditions a masked interrupt may occur with an incorrect level. The conditions are: an external unmasked interrupt must occur coincident with an internal masked periodic interrupt (PIT). Also, previous to the above interrupts, an external interrupt line at the same level as the masked PIT interrupt must have been asserted and remain asserted. Example sequence to cause problem: 1. Set CPU interrupt mask to 5; 2. Set PIT to level 2; 3. Hold IRQ2 line low. 4. Assert valid IRQ interrupts (asserting IRQ 6 or IRQ7) the PIT exception is taken if pending. This is an erratum.

**IM:95 WORKAROUND:** Unknown at present. IM:97 Mod Date: 7/19/94

**INTEGRATION:** Several conditions combined may introduce apparent Periodic Interrupt Timer (PIT) clock errors. The clock error occurs if LPSTOP mode is entered and exited periodically using the PIT, and the system clock is set to minimum (131 KHz) prior to entry of LPSTOP mode and set to maximum at LPSTOP exit (PLL must re-lock). Also, on exiting from LPSTOP, the CPU will be held off of the bus until the PLL is re-locked. Variations in the PIT clock period may appear as the PIT counter missing clocks (the PIT is clocked by the EXTAL reference clock in LPSTOP, if STSIM = 0). During normal operation (not in LPSTOP) the PIT counter clock source (EXTAL) is synchronized by logic to the system clock (CLKOUT). The combination of PLL re-lock time, low frequency (131 KHz) clock source (too near 32 KHz reference), and the synchronization result in this behavior. This is information only. IM:97 WORKAROUND: Use a minimum PLL frequency of 8 times the reference frequency (262 KHz for a 32 KHz reference) or higher if the system clock is toggled from a low frequency prior to LPSTOP entry (if STSIM = 0) and back to maximum on exit of LPSTOP periodically using the PIT as the controlling source. The problem is only seen when switching the PLL clock to a frequency that is too close to the reference (EXTAL) clock frequency.

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