PC68HC916Y1 DEVICE INFORMATION
(Issue 9 - 04/02/96)
Revision E Silicon
6E41C Mask Set

The following information and errata pertain to revision E samples of the 68HC916Y1 microcontroller. Italicized comments follow each item describing the status of the errata or information. Revision E of the 68HC916Y1 contains the following modules: CPU16/V7, SCIM/V6, TPU/V6, GPT/V2.2, MCCI/V3, FLASH48K/V7, ADC/V9, and two TPUSRAM2K/V6.

GENERAL INFORMATION:

1. All modules are functional.

2. This mask set uses the 4.194 Mhz fast reference crystal mask option.

3. The device is specified for operation from -40˚C to 70˚C and 4.75V to 5.25V.

4. At an operating temperature of 70˚C, the estimated data retention of the flash EEPROM is 10 years.

CPU16/V7:

1. When operating in test mode, the instruction following any instruction that asserts the ACUT bit in the SCIM Test Register (SCIMTR) may fail to execute properly. Different instructions may fail in different ways. Test mode is only to be used for TPU microcode development. This is a new erratum.

WORKAROUND: Insert one LBRN * instruction for each memory wait state used in excess of two for the bus access used to fetch the instruction that asserts the ACUT bit. Thus if the instruction that asserts the ACUT bit is stored in two wait state or faster memory, no LBRN * instructions are required. For three wait state memory, one LBRN * instruction will be needed, etc.

SCIM/V6:

1. The loss of clock circuit is intended to detect complete crystal failure (no oscillation). If this condition occurs, the system clock will be provided by an internal RC oscillator. This clock will permit entry into reset or allow continued operation with the RC oscillator which typically runs at 150 kHz. The loss of clock circuit will typically switch to the internal RC oscillator when the EXTAL clock frequency drops below 670 Hz. For normal PLL operation, the EXTAL reference must be maintained within the specified fref frequency range (3.2 Mhz to 4.2 Mhz). Normal PLL operation is not specified outside of this range as system clock irregularities will occur. Non-instantaneous or gradual EXTAL frequency changes, from fref minimum to 670 Hz, typically will cause non-specified or incorrect PLL operation. For the fullest possible protection

against clock related problems, it is recommend that the software watchdog timer be enabled. This is information only.

2. When using the phase locked-loop (PLL), if RSTEN in the synthesizer control register (SYNCR) is set and loss of clock is detected, the reset status register (RSR) will show loss of clock (LOC) as the source of the last reset several milliseconds before RESET is actually asserted. When using an external clock source, the MCU operates as specified. This is a new erratum.

WORKAROUND: None.

3. The crystal oscillator will not run with only VDDSYN powered. VDDSYN and VDDI must both be powered for proper operation. This is a new erratum.

WORKAROUND: None.

ADC/V9:

1. ADC 10-bit accuracy is tested to 2.5 counts with a 1.05 Mhz ADC clock, 2 ADC clock sample period, single-channel conversions, VRH and VDD at 5.0V and VRL and VSS at 0V. This is information only.

2. The ADC sample time may be programmed using the STS[1:0] field in the ADCTL0 register for sample times of 2, 4, 8, or 16 ADC clock periods. The ADC may not meet the 10 bits 2.5 counts at 2.1 Mhz accuracy specification when using the 2, 4, or 8 ADC clock period sample times. This erratum was not fixed on this revision.

WORKAROUND: Use an ADC sample time of 16 ADC clocks to achieve 10 bits 2.5 counts at 2.1 Mhz.

TPUSRAM2K/V6:

1. The transient peak standby current (ISB) may temporarily be up to 3 mA when the VSTBY pin has power applied and VDD is being powered up or down. Once VDD is below 0.5V or above VSTBY - 0.5V, the current returns to specified levels. The slower VDD rises or falls, the longer the period of excessive current consumption. If the VSTBY power source is current limited, this could cause the VSTBY voltage to drop enough to clear the power down status (PDS) flag in the TPU RAM module configuration register (TRAMMCR), indicating a loss of power. This is information only.

FLASH48K/V7:

1. Programming and erasure are specified for operation at room temperature only. Read and verify operations are tested from -40˚C to 70˚C.

2. A filter capacitor should be connected between VFPE and VSS (typically 0.1 F to 1 F) to filter out transients which may cause damage to the VFPE pin. The VFPE pin should be connected to

VDD during normal (read) operation. Connecting VFPE to VSS or allowing it to float may cause permanent damage. In systems where access to the VFPE pin is limited, VFPE may be pulled up to VDD with a low voltage drop diode (0.35V maximum drop). Application of the programming voltage to VFPE will then reverse bias the diode, protecting VDD from excessive reverse current. In this case, leakage on the VFPE pin, from external devices, must be kept low to minimize the voltage drop across the diode. The figure below is a recommended conditioning circuit for the VFPE pin. This is information only.

Revision 0.0, 20 NOV 96

last update: Mar 26 1998