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Motorola Semiconductor Application Note

AN1741

In-Circuit and Emulation Considerations for MC68HC05JJ/JP Series Microcontrollers

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Introduction

The MC68HC05JJ/JP series of microcontrollers (MCUs) present a unique combination of traditional digital peripherals with simple analog components which can be used to construct a variety of special functions. Adding the capability of low-level analog signals to a digital IC (integrated circuit) creates issues not normally considered in applying MCUs.

For instance, for end applications where the analog accuracy requirement is less than eight bits and the sample and hold feature is not used, then the user has more flexibility in circuit board design or emulation. But care should be used in circuit board layout and consideration should be given to the limitations of emulation when requiring higher analog accuracies or when trying to maintain a sample voltage.

This application note discusses those issues which must be considered both in the end application and while the user is developing software with an emulator, such as the MMDS05.

System Interactions

A number of interactions between the digital and analog portions are in the application, and the nature of these effects are discussed here. Suggestions for the specific design of a printed wiring board (PWB) to reduce or eliminate these system interactions are given here, as applicable.

Substrate Current Injection

All pins of the MCU are designed to withstand ESD (electrostatic discharge) input voltages to 2000 volts (human body model). This is accomplished on most pins by a pair of reverse biased parasitic diodes from the pin to both the V_{DD} and V_{SS} pins as shown in **Figure 1**.

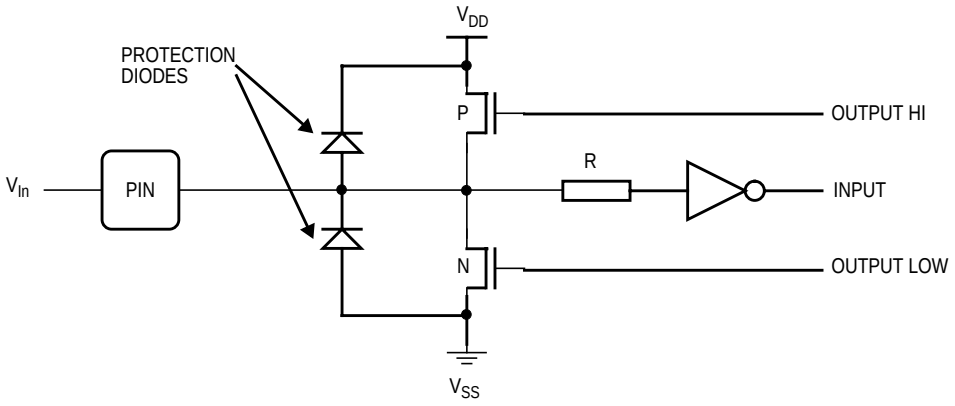

Figure 1. Input Protection (ESD) Diodes

These protection diodes are constructed of the actual drain diffusion of the two output MOS (metal-oxide semiconductor) devices into their respective substrate diffusion. The diode to V_{DD} goes through the drain of the P-channel MOS device to the N-type diffusion well under the MOS device which is then connected to the V_{DD} metal back to the V_{DD} pin. The diode to V_{SS} goes through the drain of the N-channel MOS device to the P-type substrate of the IC, which is then connected to the V_{SS} metal back to the V_{SS} pin. Therefore, when these diodes conduct, the current passes into these well or substrate diffusions before reaching the respective power supply pins. If some of this substrate current disperses

and flows under another MOS device, that device can conduct slightly, causing unwanted leakage currents to nodes connected to the MOS device or the substrate itself.

The most sensitive component to substrate currents is the internal sample capacitor. It typically can hold its charge for several minutes at room temperature, but due to inherent silicon diffusion leakage, this degrades quickly as the temperature is raised. Leakage currents in silicon double every 10 °C such that a one-minute decay time can degrade to less than a second at 85 °C. In practice, a decay rate of 0.2 V/sec should be used for the overall temperature range of –40 °C to +85 °C.

In the presence of substrate currents, the HOLD or DHOLD multiplexers connected to the sample capacitor can cause the charge to leak off in less than a millisecond at room temperature. The effect of the substrate current is further emphasized at higher temperatures. This behavior is also characterized by a dependence on the voltage levels present on the multiplexers when the substrate current is present. The bias on the channel select bus can either charge or discharge the sample capacitor.

The user can control substrate current injection by either limiting the excursions of the input signals or by limiting the maximum current that will flow. Also, the susceptibility to substrate injection will vary from pin to pin depending on their placement with respect to the V_{SS} pin and the location of the sensitive analog devices as shown in **Figure 2**. Pins near V_{SS} or which have current paths not near the sensitive analog functions will have less effect than pins which have the analog circuitry between them and the V_{SS} pin.

The sensitivity of any given design to substrate injection currents can be determined with a “droop” test which compares two A/D (analog-to-digital) conversions:

- One taken immediately after the voltage is sampled
- Another taken after a time delay after the sample is held

If these two samples are taken repetitively in software, then the voltage ramp peaks on the integration capacitor connected to PB0 can be observed to compare the amount of decay (or increase) for the unit of

time delay. The two samples should be taken using new samples of the same fixed voltage and not done as multiple conversions made from the same sample.

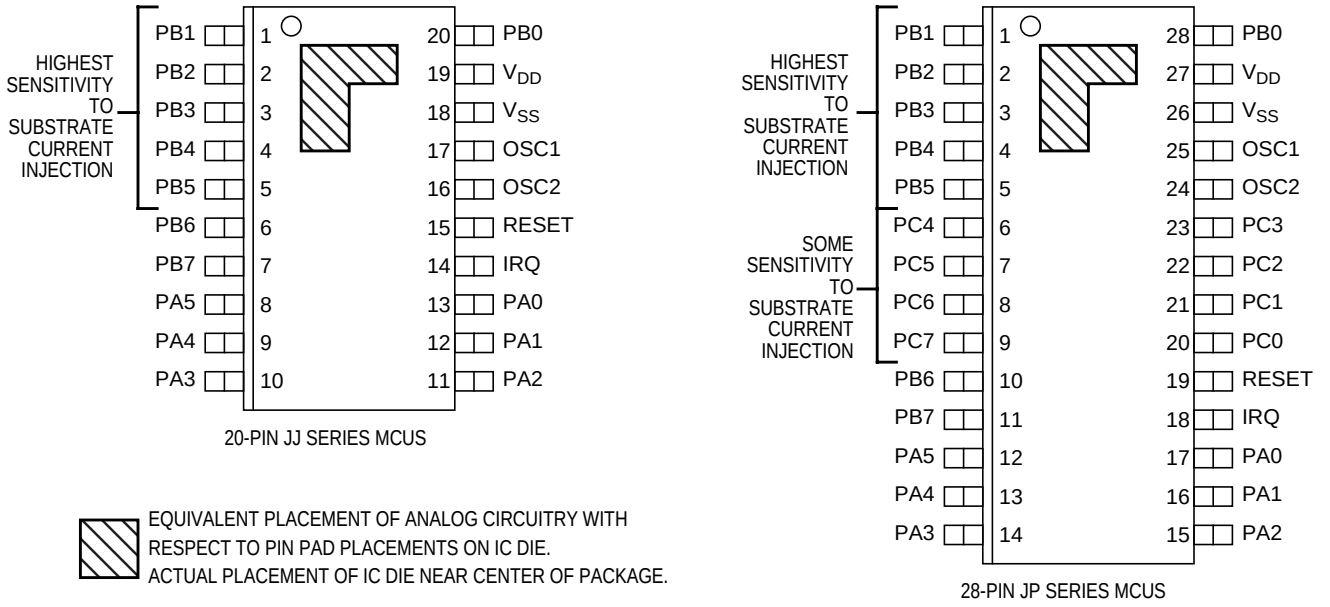

Figure 2. Substrate Current Injection Sensitivity

In practice, the common mode range for the analog inputs can extend below V_{SS} until the input protection diode starts to conduct at about –0.3 volts (at 125 °C). If the input is taken further negative, the diode conduction can become excessive. Similarly, if the input divider is used, the common mode range for the analog inputs can extend above V_{DD} until the input protection diode starts to conduct at about V_{DD} +0.3 volts (at 125 °C). If the input is taken further positive, the diode conduction can become excessive.

Excessive current (greater than 25 mA) can permanently damage the input protection diodes and neighboring input structures. Lesser currents through these diodes can disrupt some of the analog circuits due to substrate current injection. The application circuit should either limit the voltage excursions on *all* pins or limit the currents that they can produce in the protection diodes to less than 600 microamperes. Two limiting methods are shown in **Figure 3**.

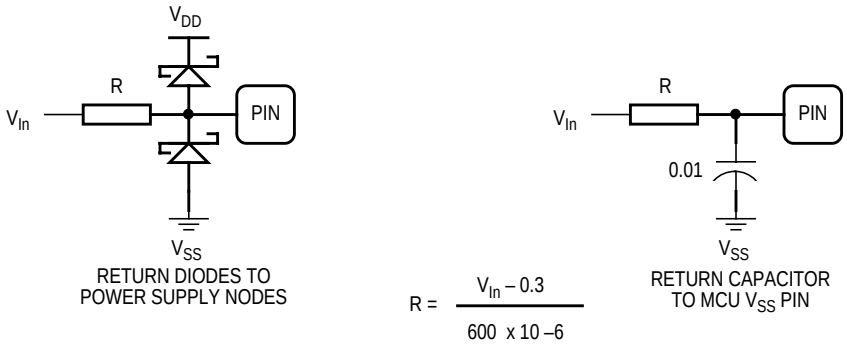

Figure 3. Input Protection Methods

Pins set up as inputs are more likely to be affected by substrate current injection than pins which are configured as drivers. When configured as a driver, the impedance to the V_{DD} or V_{SS} pin is reduced so that it is a more effective shunt of transient currents. It is, therefore, recommended that unused pins should be left unconnected and configured as outputs which are driven by the software to the V_{SS} supply.

NOTE: *Avoid leaving unused or unconnected pins configured as inputs. This makes them more susceptible to transients which can produce substrate current injection.*

V_{SS} Offsets

The MC68HC05JJ/JP series of MCUs has only a single V_{SS} pin through which flows both the analog and digital currents. Also, any external load which sinks current into the device will pass this current through the V_{SS} pin. The internal analog and digital V_{SS} lines are connected to the V_{SS} pin through separate bonding wires. But the current of both must flow through the leadframe and out of the V_{SS} pin to the user's circuit as shown in **Figure 4**.

The resistance of the bond wires, R_{BW}, and the leadframe, R_{LF}, are about 0.10 and 0.07 ohm, respectively. The resistance of the substrate, R_{SUB}, can be ignored since it is several orders of magnitude greater than the bond wire impedance. The level on the AV_{SS} pad of the IC will be at least 0.1 mV higher than the voltage on the internal leadframe, XV_{SS}, due to about 1 mA of current for I_{SSA}. The typical running current for the digital section, I_{SSD}, will be 3 mA for f_{OSC} of 4.1 MHz. The combined

analog and digital current will raise the internal leadframe voltage, XV_{SS}, about 0.7 mV above the voltage at the external end of the package pin. Altogether, the AV_{SS} pad then will be 0.8 mV above the external voltage on the V_{SS} pin. External loads connected from V_{DD} to the I/O pins will sink their current into the digital side of the IC and out through the DV_{SS} pad. For each 6 mA of load current, the AV_{SS} pad will rise another 1 mV.

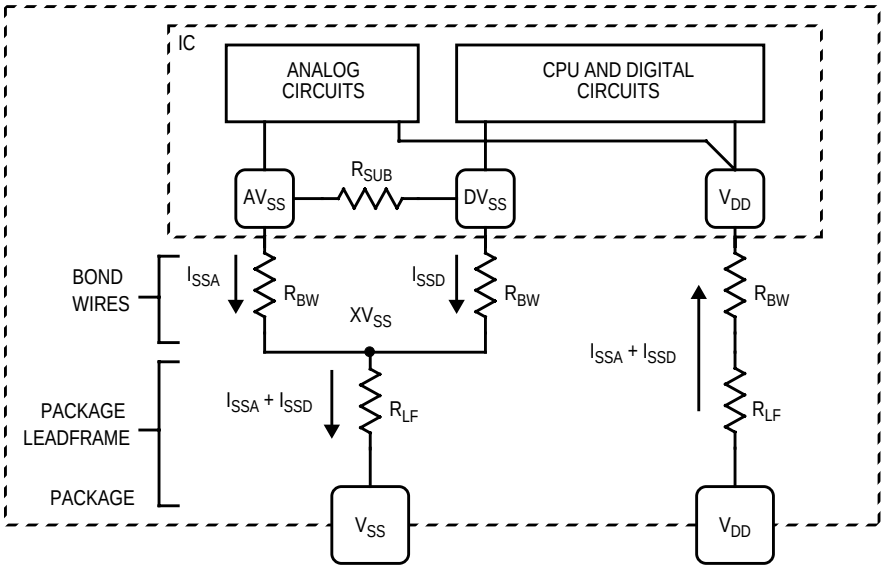

Figure 4. V_{SS} Pin Offsets

Any external impedance sharing the total I_{SS} current will cause substantially more voltage shift in the internal AV_{SS} reference pad as shown in **Figure 5**. In this example, the I_{SS} current must share a short 2.0 cm by 0.5 mm length of 38-micron thick copper (1 oz.) on a PWB before reaching the power supply tie point used for a signal source. That copper trace impedance, R_{PWB}, will add an additional 18-milli-ohm resistance which will cause the internal AV_{SS} pad to move up another 0.2 mV when the LED (light-emitting diode) connected to PA0 turns on and sinks 10 mA.

Shared V_{SS} return impedances must be kept to a minimum if the analog accuracy is to be better than eight bits which has 14 mV per bit for a maximum 3.5-volt signal. The total of 1 mV given in these examples would represent an offset to the AV_{SS} reference pad which equals one bit in a 12-bit analog measurement of 3.5 volts. It is, therefore, important

to consider the impedance paths and signal reference points used when the application requires better than 8-bit accuracy.

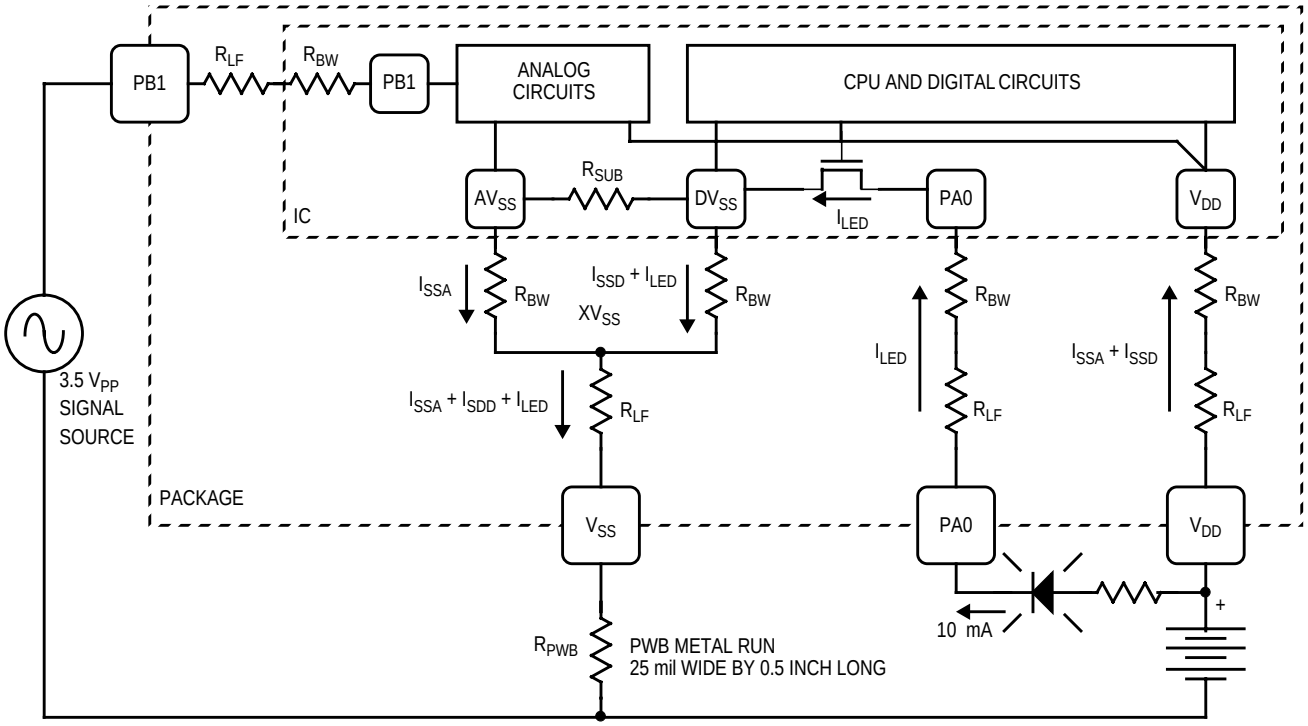

Figure 5. External V_{SS} Pin Offset Example

Current Spikes

Similar to the voltage offset just described, current spikes from high speed digital switching circuits will generate a small voltage drop across the package pin shared with the analog subsystem due to the inductances shown in **Figure 6**. The inductance of the bond wires, L_{BW}, and the leadframe, L_{LF}, are about 2 to 5 nH each. This inductance is particularly a problem with fast switching currents. The voltage change for a fast transient through an inductor can be calculated using the equation given in **Table 1**.

A digital CMOS device has fast switching transients which occur while one of the P-channel and N-channel MOS devices is turning on and the other is turning off. During a short interval of 3 to 5 nanoseconds, these may both be on and present a 100- to 600-ohm load across the power

supply pins. The net result can be a 5-nanosecond rise time which generates a 30-mA current peak.

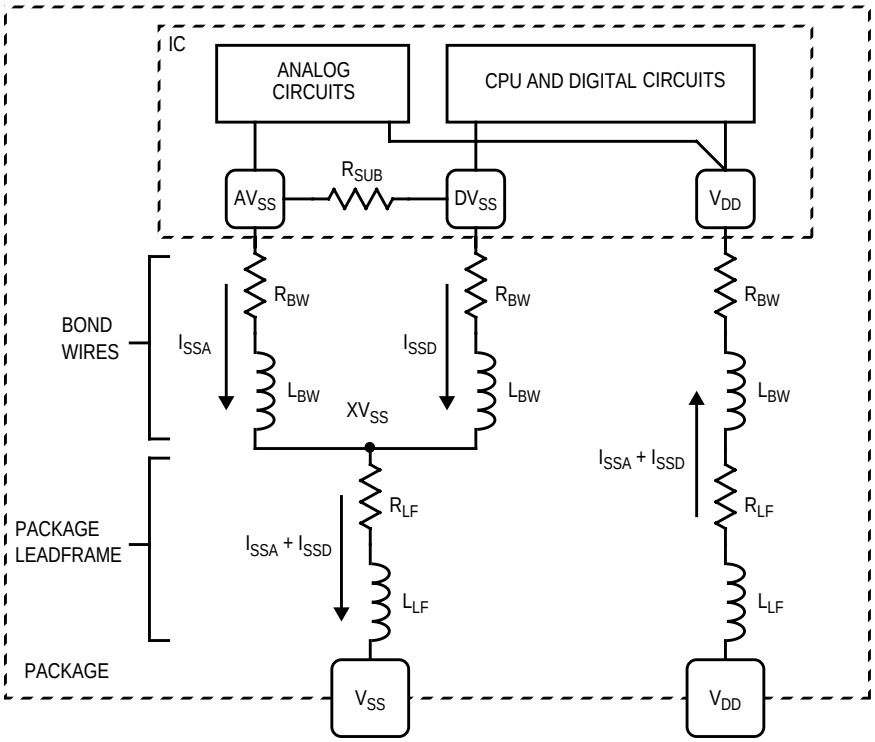

Figure 6. V_{SS} Pin Inductance

Applying this transient to the example in **Figure 6** with a nominal 5-nH inductance will generate a voltage of 30 mV. Circuit interconnect can add about eight nH/cm for typical PWB traces or a No. 30 AWG (American Wire Gage) wire. Under these conditions, a current transient applied to the example in **Figure 5** would contribute an additional 16 nH of inductance for additional voltage of 96 mV. Further, when the LED turns on, it will cause an additional 10-mA current spike resulting in an additional voltage of 42 mV. These can total to a 180-mV voltage spike on the internal AV_{SS} reference node, or about 13 bits in an 8-bit analog measurement. Current spikes are far more significant sources of V_{SS} reference noise than DC offsets.

One particularly troublesome high current spike case occurs when using the discharge device on PB0 to discharge an external capacitor at the

end of a single slope A/D conversion. This discharge can easily reach current peaks of 25 mA or a typical voltage of 25 mV for the V_{SS} pin itself.

NOTE: *Discharging large capacitors or low impedance loads into the PB0 pin can cause high current spikes which may disrupt the internal analog V_{SS} with respect to the V_{SS} pin and cause unwanted analog noise. Repeated high currents also can damage the discharge device and/or the device's interconnect metal. Using capacitors that are less than 2 F and discharge current peaks less than 25 mA is recommended.*

Current transients can cause the analog subsystem V_{SS} reference to rise or drop several hundred millivolts during switching transients.

NOTE: *It is recommended that switching any port pins which carry more than a few milliamperes of current should not be done during A/D conversions or when trying to maintain a charge on the sample capacitor. Further, sampling of the comparator outputs should not be done when these switching transients may be present.*

Also, always clear any CPF1 or CPF2 flags which might get set during such switching transients.

Ground Bounce Noise

One observed source of analog signal corruption comes from V_{SS} ground bounce noise which acts like a combination of current spikes and substrate current injection. The ground bounce signal is a resonant voltage swing as the result of the inductance and stray capacitance of the pins and the power supply leads. These signals can cause voltage transients that swing several hundred millivolts above or below ground. If these swings are large enough, the input protection diodes may begin to conduct and, therefore, generate substrate current ejection problems.

In many cases, the user is in control of the significant sources of ground bounce noise. These occur when the MCU's I/O pins suddenly turn on and sink high currents through the V_{SS} pin. It is recommended that switching of any loads does not occur during the time the sample capacitor must hold its charge. Other sources can be poor layouts on printed wiring boards (PWB) layouts that allow high current loads to share the V_{SS} metal return to the power supply.

System Noise

System noise is inherent to a mixed signal design such as the MC68HC05JJ/JP series of MCUs. This may manifest itself as signal pickup in high impedance signal lines not related to the effects mentioned earlier. There will always be some level of noise which cannot be filtered out, bypassed, or avoided by careful PWB layout.

Also, the general level of system noise, or "noise floor," will be dependent on the operating frequency of the MCU. Lowering the f_{OSC} frequency will reduce the frequency harmonics and the number of times per second that the system is subjected to digital current spikes. This latter effect is important when considering that the single-slope A/D technique is integrating a current over a long timeframe looking for a comparison in voltages to the millivolt level.

The single slope A/D method provides some level of averaging of the input signals; but additional digital averaging may be necessary to further reduce the effects of unwanted noise in the readings. The penalty of the added filtering will be a reduction in response time to the input signal.

NOTE: *Experience has shown that the least sensitivity to substrate current injection, current spikes, and ground bounce noise is created when the channel select bus is connected to the internal V_{DD} after the HOLD of DHOLD multiplexer has been turned off. This also means that the input channel multiplexers are off. Leaving the channel bus connected to V_{SS} or a low voltage input creates the most sensitivity to these noise sources.*

NOTE: *In cases where severe system noise affects input signal measurements, it is recommended that the sample and hold method not be used. Instead, always leave the signal connected to the comparator through the HOLD or DHOLD and channel multiplexers.*

Stray Pin Capacitance

Stray capacitance in the range 0.05 to 0.6 pF is present between pins on the MCU. The pins near the center of the IC have higher stray capacitance due to the design of the leadframe. The effects of stray capacitance can be minimized by connecting the digital and analog grounds together only at the package, which reduces the series impedance to the digital. Otherwise, any high digital current spikes through the increased series impedance can generate a small signal

which can then be transferred through the stray capacitance to any high impedance signals on the analog pins as shown in **Figure 7**. The effects of stray capacitance can be minimized by using these suggestions:

1. Use lower impedance signal sources.
2. Avoid switched currents in pins adjacent to signal pins.
3. Reduce interconnect lead lengths.
4. Use local bypassing to provide lower impedance paths to V_{SS}.
5. Avoid passing switched load lines over or parallel to signal conductors.

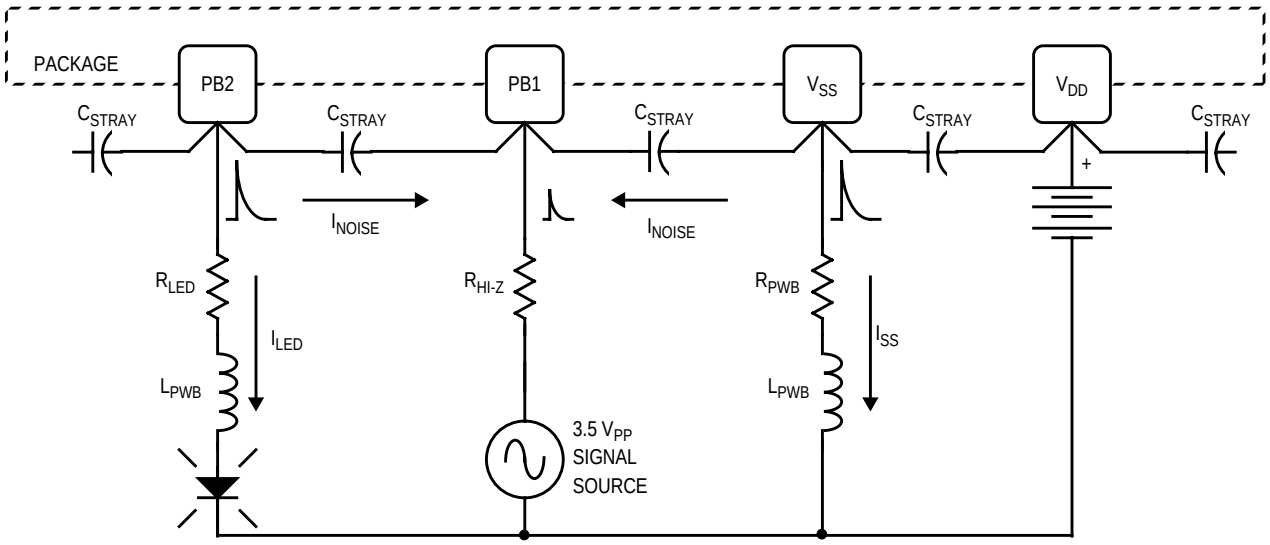

Figure 7. Effects of Stray Capacitance

Bypass Capacitors

Bypassing of the V_{DD} and V_{SS} supply pins and some inputs will reduce noise effects. Bypass is best done with a monolithic ceramic capacitor for the high frequencies and a small tantalum cap for low frequencies. The ceramic should be mounted as close as possible to the device with its leads less than 0.1 inch in length. A ceramic capacitor should be mounted at each device, but one tantalum can be shared by several devices. Paper and film caps are not good choices for bypassing. Bypass capacitors should be in the range of 0.01 to 0.1 F for the ceramic

capacitor and 1 to 10 F for the tantalum capacitor. Ceramic capacitors alone can be used as bypass capacitors to reduce noise pickup on the PB1:PB4 inputs, if the application permits.

PWB Parasitics

The PWB itself also can be a source of desirable stray capacitance between the supply lines (V_{DD} and V_{SS}). But it also can have unwanted stray capacitance which may cause unwanted signal interference between signals. The stray capacitance of a PWB can be calculated using the equation in **Table 1**. For typical PWB made of glass-fiber epoxy, this is about 3 pF/cm^2 for conductors located over each other on the opposite sides. Multiple layer PWBs may have a higher capacitance due to a smaller distance between layers.

EMC Antennae

Interconnect lines can act like small antennae which can pick up radiated signals from other sources external to the application or from electrostatic or electromagnetic signal sources within some other area of the application itself. Some of these interconnect lines can also act as antennae which radiate electrostatic or electromagnetic signals to other devices external to the application. Either case results in unwanted electro-magnetic compatibility (EMC) issues.

Keeping interconnect lines as short as possible will reduce both pickup and radiation.

NOTE: *Be particularly careful not to form small loop antennae which have high frequency currents flowing in them. If such loops must be present ,their loop area should be minimized. A typical source of such a loop antenna is the bypass capacitor between the V_{DD} and V_{SS} power pins.*

Examples of the loop for the bypass capacitor are shown in **Figure 8**.

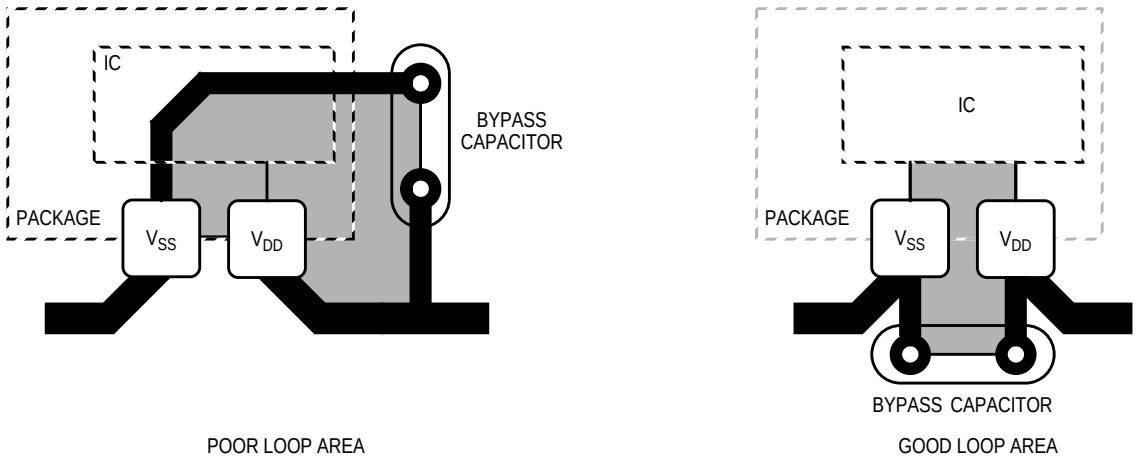

Figure 8. Loop Antennae

Ground Loops

Ground loops are both a source of EMC problems and unwanted V_{SS} offsets. When loads and signal returns are connected together in long loops, the currents that flow back to the low impedance power source can generate small voltage drops which alter the critical reference of the signal source with respect to the V_{SS} pin on the MCU. Signal sources with low currents should have their own return conductors back to the V_{SS} pin on the MCU. Loads should have their own return conductor back to the lowest impedance power source node. This node is usually the point where the power supply is connected to the PWB or module. Finally, the V_{SS} and power pins on the MCU should be taken directly to the low impedance power source node without sharing the ground returns for either the signal sources or loads. This is the “star” connection scheme rather than a “loop” of ground connections. Examples of ground loop and star connections are shown in **Figure 9**.

In the ground loop case, the I_{SS} and I_{Load} currents share a metal run which will increase the level on the V_{SS} pin. Similarly, the I_{SS} and I_{Load} currents share a short metal run with the I_{SIG} current which will increase the voltage at the reference end of the signal source. In the star connection case, the MCU and the load do not share a metal run so there will be no unwanted shifts in the reference pins for the MCU or the signal source. The signal source and the MCU share a metal run back to the low impedance power source, but any changes in the V_{SS} pin

potential will be nulled out since they are also equally applied to the signal reference as well.

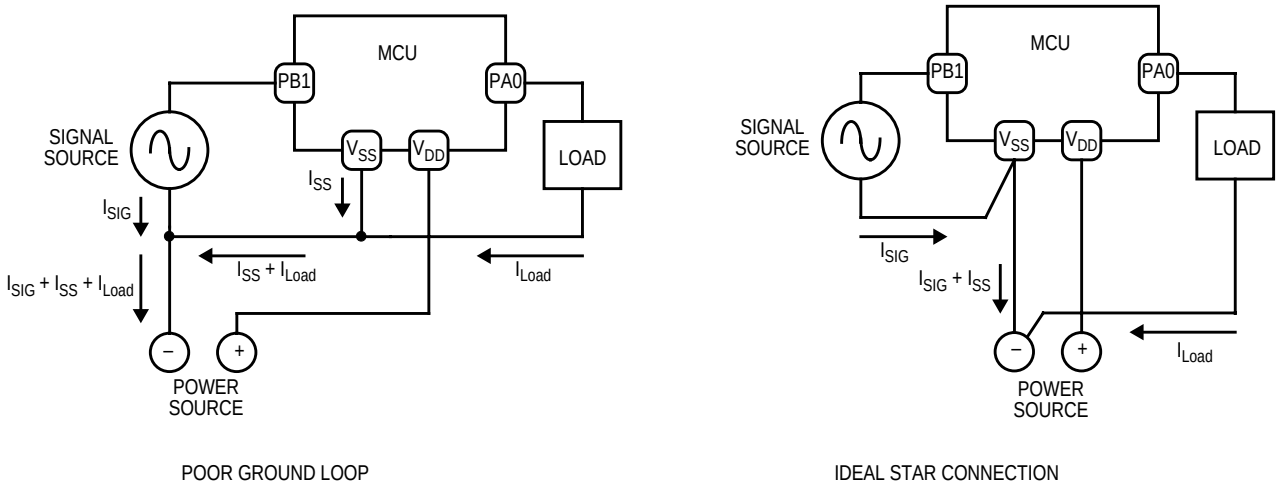

Figure 9. Ground Return Methods

Light Effects

The window on erasable EPROM devices can allow light to enter and affect bias currents, trip points, and leakage in the analog subsystem. The window on these devices must be covered with an opaque material such as black electrical tape. Common white paper labels are not opaque enough to prevent light from affecting the analog subsystem. The one-time programmable (OTP) devices use an opaque plastic package and will not be affected by light.

NOTE: *The window on erasable EPROM devices must be covered with an opaque material such as black electrical tape.*

PWB Techniques

The mixing of low-level analog signals with high speed digital switching transients always presents a challenge to the PWB designer. Attention to board layout applies equally when using the MC68HC05JJ/JP-series of MCUs with A/D conversions. Several suggestions on proper PWB layout have been given for specific system interactions. Signal layout considerations tend not to be a problem if the desired analog accuracy is less than eight bits or the clock frequency of the MCU is less than 1 MHz.

These general rules summarize those suggestions and provide additional considerations that will help minimize the effects of system noise and interactions.

1. Bypass the V_{DD} to V_{SS} pin with a 0.1- F capacitor as close to these two pins as possible.
2. Connect the external ramp capacitor to the PB0 and V_{SS} pins as close as possible to these two pins.
3. Return all analog signal sources back to the V_{SS} pin without sharing any current path with a digital signal or load.
4. Route all high current or digital signal returns back to the power supply input to the PWB; and then connect the V_{SS} pin of the MCU directly to that common tie point.
5. Do not pass digital or high current signals parallel to any low-level or high impedance analog signal.
6. Avoid 90 bends in traces. Use 45 bends or curved traces.
7. If the signal source can tolerate capacitive loading, add 0.1- F bypass capacitors to the input pins (PB1–PB4) as close as possible to the package and connected directly to the V_{SS} pin.
8. If cost considerations allow the use of a 2-sided PWB, try to make one side as much ground plane as possible.
9. Avoid using sockets, as they can increase stray capacitance and series inductance.

10. Ground planes tied to the V_{SS} pin and not carrying any digital load currents will provide shielding and increase the more desired stray capacitance between the supply pins.
11. If a multi-layer PWB is used, place the ground and power planes near or at the top level.
12. Minimize the number of via holes through a ground plane.
13. Avoid notches in the ground plane.
14. Place continuous ground plane near high speed signal traces.
15. Minimize length, bends, and number of via holes for clock or periodic high speed signal traces.
16. Reduce all return path impedances.

Table 1 gives the equations for calculating PWB parasitics and typical values to be expected.

Table 1. PWB and Wire Parasitics

Parasitic	Equation	Typical values
Resistance	$R = \frac{\rho x_R}{a_R}$	No. 22 AWG wire = 0.5 milli-ohm/cm No. 30 AWG wire = 3.4 milli-ohm/cm 1 oz. PWB copper trace: 0.5 mm wide = 9 milli-ohm/cm 1.0 mm wide = 4.5 milli-ohm/cm
Capacitance	$C = \frac{0.00885 E_R a_C}{d_C}$	1.5 mm thick glass-fiber epoxy PWB: 2.8 pf/cm^2
Inductance (wire)	$L = 0.0002 x_L \left[\ln\left(\frac{2x_L}{r_L}\right) - 0.5 \right]$	1 cm of No. 22 AWG wire = 7 nH 100 cm of No. 22 AWG wire = 114 nH 1 cm of No. 30 AWG wire = 9 nH 100 cm of No. 30 AWG wire = 132 nH
Inductance (strip)	$L = 0.0002 x_L \left[\ln\left(\frac{2x_L}{y_L + z_L}\right) + 0.2235\left(\frac{y_L + z_L}{x_L}\right) + 0.5 \right]$	1 oz PWB copper trace: 1 cm of 0.5 mm wide = 8 nH 100 cm of 0.5 mm wide = 128 nH 1 cm of 1.0 mm wide = 7 nH 100 cm of1.0 mm wide = 115 nH
Inductance V	$\Delta V = L\frac{\Delta I}{\Delta t}$	Current spike through a package lead typically yields a V of 1 mV/ mA of current through that lead.

where:

R = Resistance (ohms)

ρ = Resistivity (ohm-cm)

x_R = Length of resistance material (cm)

a_R = Cross-sectional area of resistive material (cm^2)

C = Capacitance (pF)

E_R = Dielectric constant relative to air (4.7 for most PWBs)

a_C = Area of capacitor plate (mm^2)

d_C = Capacitor plate separation (mm)

L = Inductance (H)

r_L = Radius of inductor material (mm)

x_L = Length of inductor material (mm)

y_L = Width of inductor material (mm)

z_L = Thickness of inductor material (mm)

V = Change in voltage across inductor (volts)

I = Change in current through inductor (amps)

t = Time over which I changes in inductor (seconds)

Emulator Limitations

Emulators for the MC68HC05JJ/JP series of MCUs must operate the device in one of its expanded test modes to gain control of the device and interact with its I/O and memory resources. Such a configuration immediately presents multiple devices, external interconnect lines, and high-speed signals into the user’s target system. The prior discussion suggests that it can easily be expected that the background level of all the system interactions will be higher. Indeed, this is usually the case, with some degradation in analog system performance during use of an emulator.

The preferred emulation tool is the M68EM05JP7 emulation module with the Motorola modular development system for HC05 MCUs, MMDS05. The M68EM05JP7 also can be used with the Motorola evaluation system for HC05 MCUs, M68HC05PFB. Their behavior with regard to the system interactions are similar, but emulators from other manufacturers may have different responses.

MMDS05 Considerations

The Motorola MMDS05 development system with a M68EM05JP7 emulation module operates a 28-pin JP series device (either EPROM or ROM version) in its expanded emulation mode.

In this mode, all of the port B functions are unaltered and can be connected directly to the user's target system.

Ports A and C, however, are converted into expanded data, address, and control bus signals for control by the mother board or use by the bus state analyzer within the MMDS05. The actual port A and C connected to the user's target system have been reconstructed using external components to the JP MCU. The MCU bus is now exposed external to the device and can operate at frequencies to 2.1 MHz. These high frequency buses and complex personality board layout present a source of system noise, ground bounce, and current spikes which do not occur in the user's end application where the MCU runs in the single-chip mode.

These considerations, as well as some other possible problems the user might encounter when developing their software, are discussed in this application note. When developing code using the M68EM05JP7 emulation module, several considerations should be kept in mind.

Noise Reduction

The emulator will have much more noise than the actual device mounted in a PWB. Several fixes or operating techniques will reduce the noise effects of the emulator. These are:

1. Try mounting 0.1- F bypass caps on the emulator module between PB1, PB2, PB3, and PB4 and V_{SS} at either the XU22 or XU23

sockets to suppress emulator-induced noise. See **Figure 10** for details.

2. Try mounting a 0.1-F bypass cap on the emulator module closely between V_{DD} and V_{SS} at either the XU22 or XU23 sockets to suppress emulator-induced noise. See **Figure 10** for details.

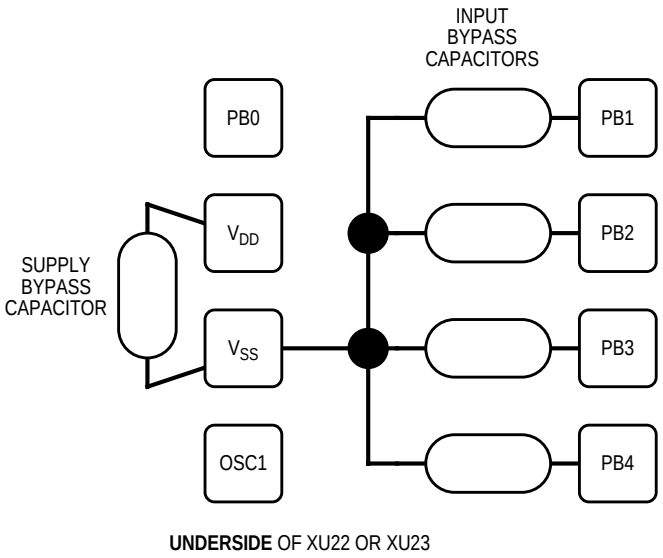

Figure 10. Local Bypassing on M68EM05JP7

3. Unused I/O port pins should be configured as outputs which are driven to V_{SS}. Do not leave unused pins as floating inputs as this increases the sensitivity to noise-induced substrate injection currents.
4. Using a slower clock frequency will reduce the noise in the emulator and, therefore, reduce the analog sensitivity to it.
5. If the sample and hold function is to be used, always connect the channel bus to the internal VREF node on a separate write cycle to the AMUX register after the HOLD or DHOLD multiplexer has been turned off.
6. Do not use Schottky diode clamps tied directly to the pins on XU22 or XU23 on the M68EM05JP7 emulation module as a means to reduce substrate current injection. There is no suitable supply tie

points for them and a series resistor cannot be used on those MCU pins which have been changed into the expanded emulation mode bus signals.

Operational Notes

When using the MMDS05, there are several operational suggestions that should be noted when emulating the MC68HC05JJ/JP series of MCUs. These are:

1. Avoid powering up the MMDS05 with the power supply for the emulation module set below 4.0 volts because the emulator may not start in this case. The emulator module can run with the emulation device operating down to 2.7 volts. However, if your software crashes during low-voltage operation, be sure to increase V_{DD} before restarting the emulator.
2. Use the RAPID software for your debug environment, as it allows quick switching among emulator, editor, and assembler (CASM).
3. Writing to the pulldown inhibit registers (PDRA and PDRB) on the emulator will result in a message:

   "WRITE did not verify"

   This message merely reflects the fact that these registers are write-only registers which cannot reflect back their contents after a write. (The actual data read back will be the LSB of the address for the PDRs.)
4. When using A/D mode 2 or mode 3 on the emulator, avoid setting the memory display (MD) to show the contents of the 16-bit timer registers (any address less than $0020). When the emulator stops on a breakpoint, it will read these registers to refresh the display on screen. If the ICF, OCF, or TOF flags have been set before the breakpoint, the emulator may read the TCR and then clear out these flags as it reads the associated LSB registers.
   Also avoid using the real-time variable display RTVAR function which may cause additional accesses to the wrong registers, as well. Use the bus analyze function to watch 16-bit timer operations, or insert into your software predictable reads of these registers which are then stored to RAM locations which can be monitored as real-time variables.

5. The order of some reads and writes of the analog subsystem and 16-bit timer registers are critical. When using higher level compilers to generate the MCU's object code, be careful to check that the actual object code is indeed compiled in the proper order.
6. Be sure to reset the device (RESET command) after changing the oscillator speed (using the OSC command). The emulator's MCU can have its data and/or program counter corrupted during these changes in speed. Failure to reset may cause erratic operation even when executing a known starting address (for instance, using a GO command).

Unexpected Effects

The MMDS05 emulation environment can present some unusual effects when trying to measure low level analog signals. These effects are not normally seen with emulation of totally digital MCUs. If unexpected results are observed, check for one of these cases:

1. Be careful to recognize the parasitic capacitance that is present. If the PB0 pin is left unconnected at the device, it looks like a 20-pF capacitor which requires about 800 ns to charge from V_{SS} to 4 volts. However, if the target cable is left unconnected, the pin sees about 100 pF, which extends the charge time for an open PB0 pin to about 4 seconds.
2. Be careful when using long target cable length near the host PC used with the MMDS05. Some PCs can induce as much as 10 to 20 millivolts of noise into the PB0:PB4 pins, especially if they are being operated from high impedance sources (> 10 k). The PC monitor also can induce noise onto the signals as small "steps" with a period of about 32 microseconds.
3. Be careful that any oscilloscope probes used for development monitoring do not pass near or under the host PC's monitor. The monitor may have strong electromagnetic fields which will induce into the oscilloscope display false signals which appear as small "steps" with a period of about 32 microseconds.

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