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Migrating from the MC68HC811E2 to the MC68HC711E9

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Introduction

This engineering bulletin explains how existing users of the MC68HC811E2 could migrate to the MC68HC711E9. The last date that the MC68HC811E2 can be ordered from Motorola is June 30, 2001. However, beyond that date, parts may be available from Motorola distributors.

The MC68HC811E2 is a versatile part used in many different types of applications. This document addresses applications that use the part only in single-chip mode.

Migrating to the MC68HC711E9

For current MC68HC811E2 users that use the part only in single-chip mode and don't need more than 512 bytes of EEPROM for data storage, the MC68HC711E9 is a possible replacement part (see **Table 1**). The MC68HC711E9 has 12 Kbytes of one-time programmable (OTP) EPROM that can be used for program storage.

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For complete information on the MC68HC811E2 and MC68HC711E9, see the Motorola World Wide Web site at http://www.motorola.com/semiconductors/ and *M68HC11 E Family Technical Data,* Motorola document order number M68HC11E/D.

For those that use the secure device (MC68S711E9), see *Enabling the Security Feature on the MC68HC711E9 Devices with PCbug11 on the M68HC711E9PGMR*, Motorola document order number EB184/D, and at the same Web link.

MC68HC711E9 Advantages

Advantages to using the MC68HC711E9 are:

- Additional RAM

- Faster bus frequency

- E-clock output may be turned off, which reduces RFI (radio frequency interference) emissions

Major Differences

The major differences between these two parts are:

- Package options

- Types and sizes of memory

- EEPROM block protect

- Configuration (CONFIG) register

Table 1. Comparison Chart

Device	MC68HC811E2	MC68HC711E9
RAM (Bytes)	256	512
EPROM/OTP (Bytes)	—	12 K
EE (Bytes)	2048	512
Timer	16-bit, 3 IC, 4 OC, RTI, pulse accumulator	16-bit, 3-4 IC, 4-5 OC, RTI, pulse accumulator
I/O Single Chip	38	38
Input/Output (I/O) Expanded	22	22
Serial	SCI SPI	SCI SPI
Analog-to-Digital (A/D)	8-CH, 8-bit	8-CH, 8-bit
Operating Voltage (V)	5.0	5.0
Maximum Bus Frequency (MHz)	2	2, 3
Temperature	C, V, M	C, V, M
Package Options	52 PLCC (FN); 48 DIP (P)	52 PLCC (FN); 64 QFP (FU)
Comments	Secure device available, MC68SEC811E2; EEPROM block protect	Secure device available, MC68S711E9; EEPROM block protect
Document Order Number	MC68HC11E/D	MC68HC11E/D

Difference:
Package Options

The MC68HC811E2 is available in a 52-pin PLCC (plastic leaded chip carrier) and a 48-pin DIP (dual in-line package) packages. The MC68HC711E9 is available in 52-pin PLCC and 64-pin QFP (quad flat pack) packages.
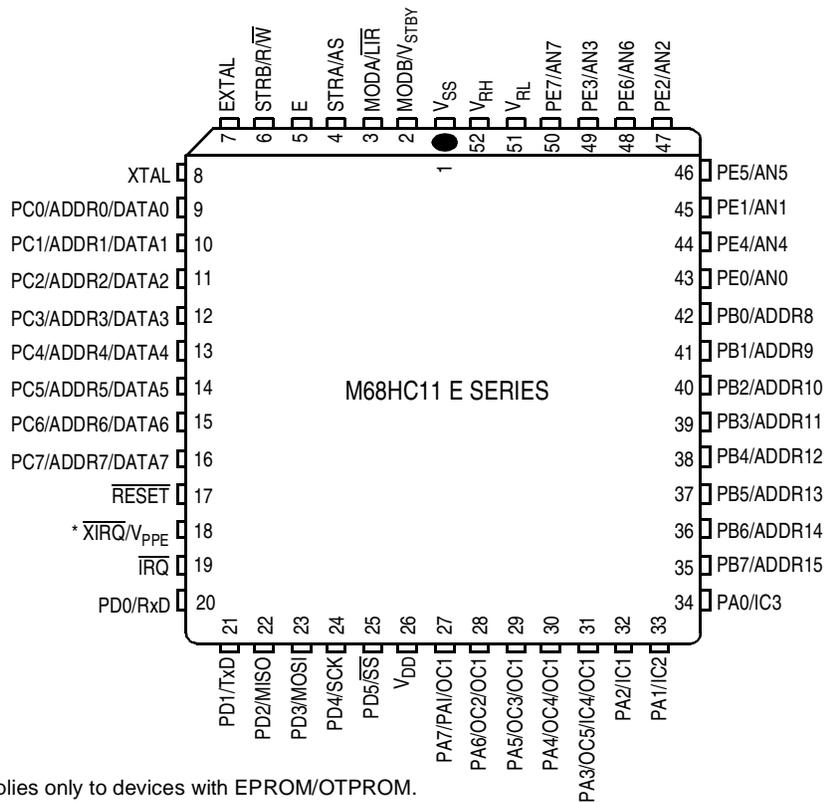
Case 1

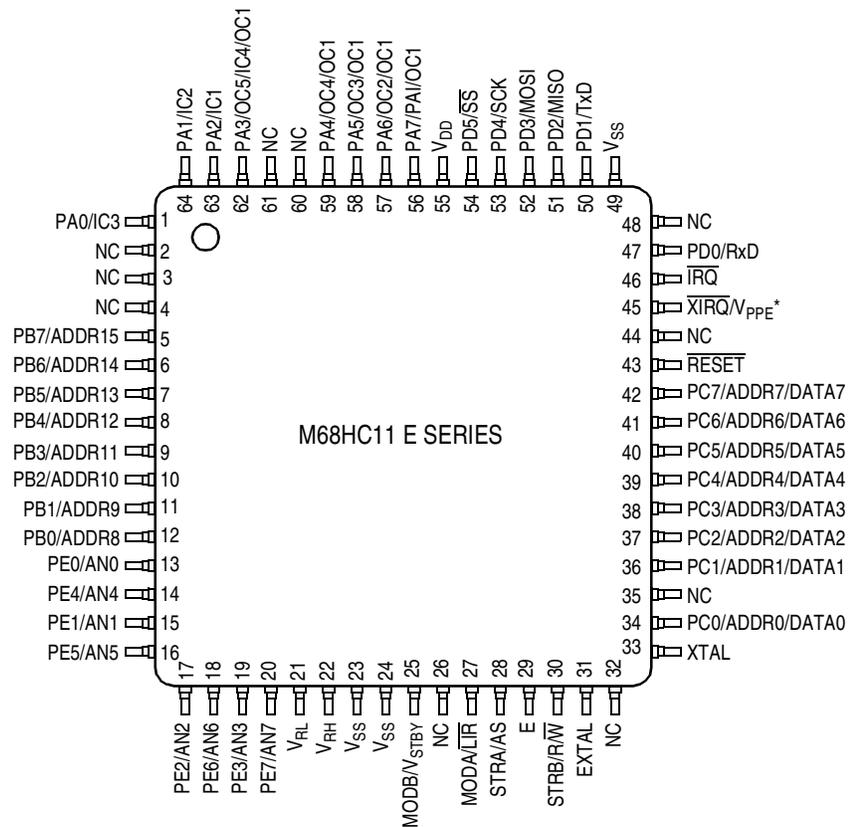|	
Example:	52-pin PLCC
Issue:	None. This is a pin-for-pin compatible part.
Change required:	None

Case 2

Example:	48-pin DIP
Issue:	No 48-pin DIP replacement part available
Change required:	Re-layout application to allow use of 52-pin PLCC or 64-pin QFP. See **Figure 1** and **Figure 2**.

* V_{PPE} applies only to devices with EPROM/OTPROM.

Figure 1. Pin Assignments for 52-Pin PLCC

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Figure 2. Pin Assignments for the 64-Pin QFP

Difference:
Types and Sizes
of Memory

The MC68HC811E2 has the same memory mapped locations for the register block and the normal mode interrupt vectors. These interrupt vectors are located in EPROM/OTP for the MC68HC711E9 instead of EEPROM in the MC68HC811E2. The RAM size and the size and location of the EEPROM for these devices is also different. In addition, the MC68HC711E9 contains EPROM/OTP in its memory map. See **Figure 3** and **Figure 4**.

Case 1

Example:	RAM
Issue:	None
Change required:	None. However, you may want to take advantage of the extra 256 bytes of RAM.

Case 2

Example: EEPROM

Issue: The MC68HC711E9 has less EEPROM (512 bytes vs. 2048 bytes), and it is located at a different starting address ($B600 vs. $F800).
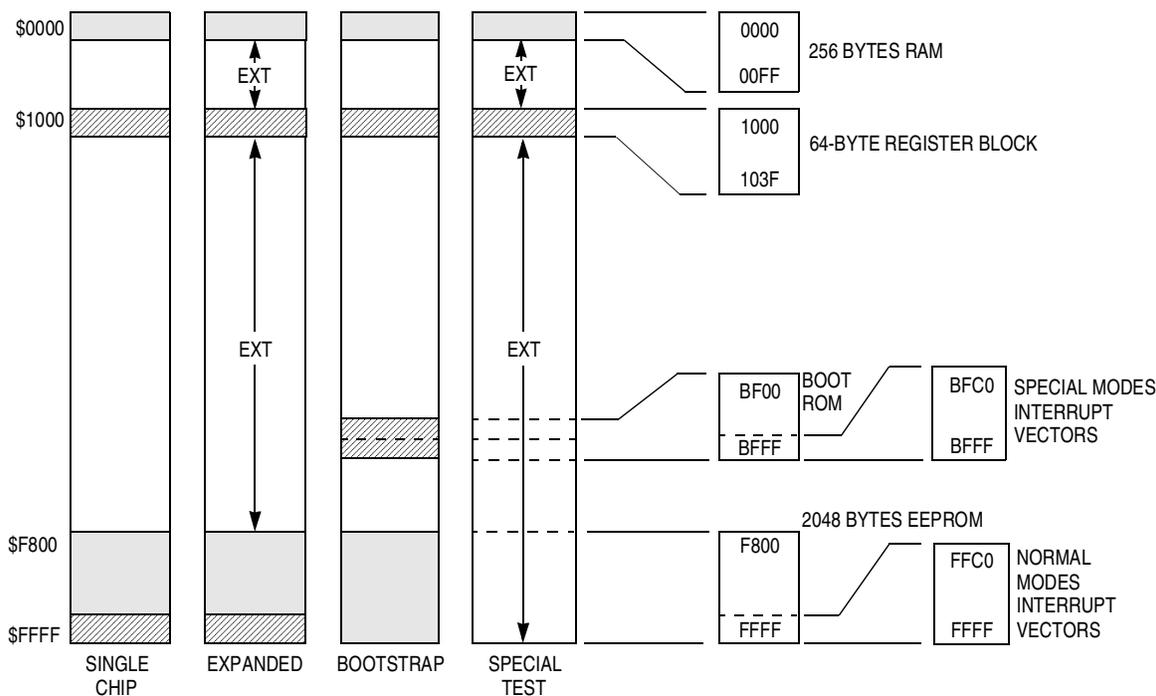
Change required: Change code to use new EEPROM block located at $B600–$B7FF.
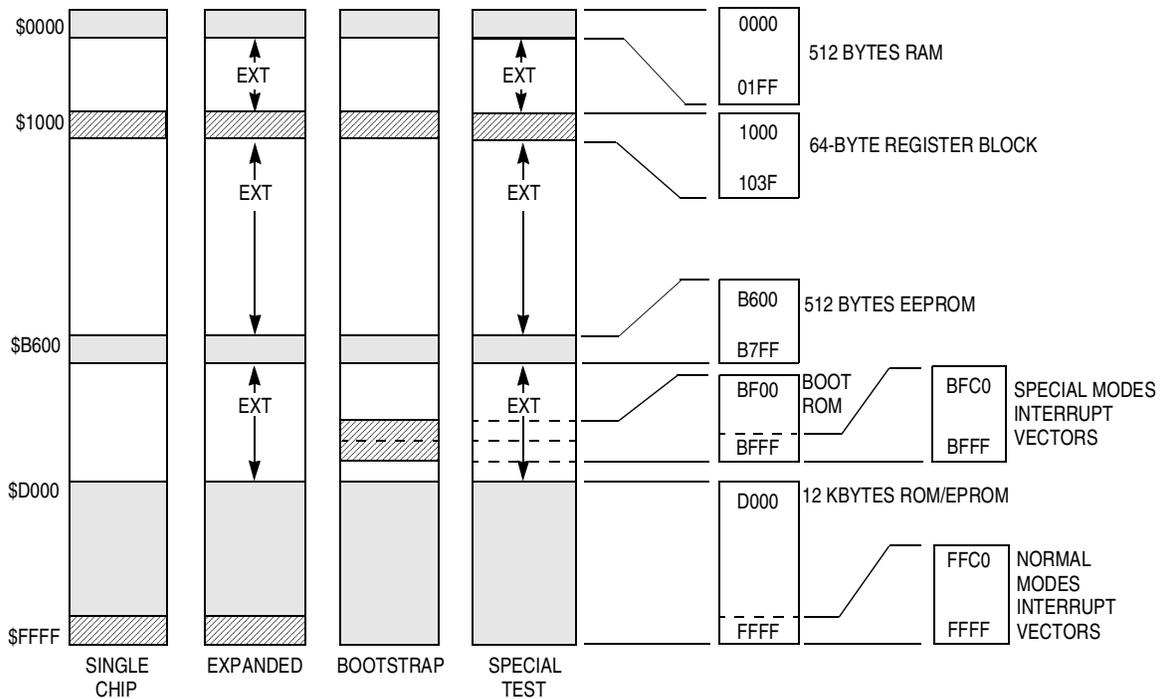
Case 3

Example: EPROM/OTP

Issue: None

Change required: None. However, you may want to take advantage of the 12 Kbytes of EPROM/OTP at location $D000–$FFBF. A user may want to program their code into the EPROM/OTP and use the EEPROM for nonvolatile data storage applications.
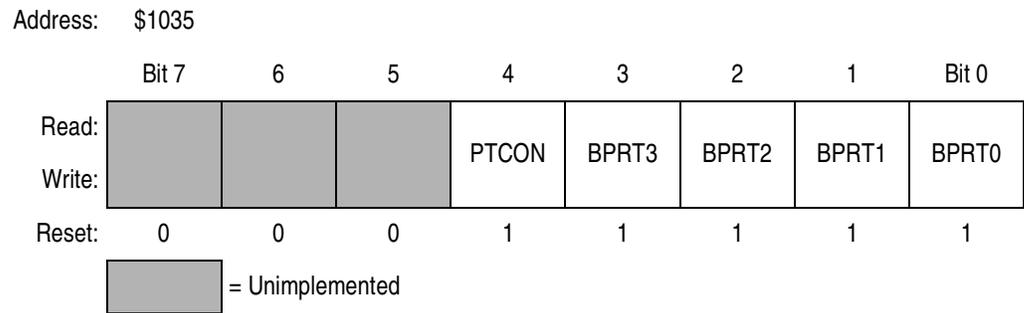
Figure 3. Memory Map for MC68HC811E2

Figure 4. Memory Map for MC68HC(7)11E9

Difference:
EEPROM
Block Protect

Since these two parts differ significantly regarding EEPROM size and location, the address range and block size that can be protected are different. See **Figure 5**, **Table 2**, and **Table 3**.

<u>Case 1</u>

Example: EEPROM block protect

Issue: EEPROM block protect addresses and sizes are different.

Change required: The BPRT bits in the BPROT register ($1035) must be changed to protect the address ranges and block sizes the user desires.

Address: $1035

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:				PTCON	BPRT3	BPRT2	BPRT1	BPRT0
Reset:	0	0	0	1	1	1	1	1

   ☐ = Unimplemented

Figure 5. Block Protect Register (BPROT)

Table 2. EEPROM Block Protect in MC68HC811E2 MCU

Bit Name	Block Protected	Block Size
BPRT0	$x800–$x9FF	512 bytes
BPRT1	$xA00–$xBFF	512 bytes
BPRT2	$xC00–$xDFF	512 bytes
BPRT3	$xE00–$xFFF	512 bytes

Note: x is determined by the value of EE[3:0] in CONFIG register.

Table 3. EEPROM Block Protect in MC68HC711E9 MCU

Bit Name	Block Protected	Block Size
BPRT0	$B600–$B61F	32 bytes
BPRT1	$B620–$B65F	64 bytes
BPRT2	$B660–$B6DF	128 bytes
BPRT3	$B6E0–$B7FF	288 bytes

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Difference:
CONFIG Register

The operation of the configuration (CONFIG) register on the MC68HC811E2 differs from the MC68HC711E9. See **Figure 6**, **Figure 7**, and **Table 4**.
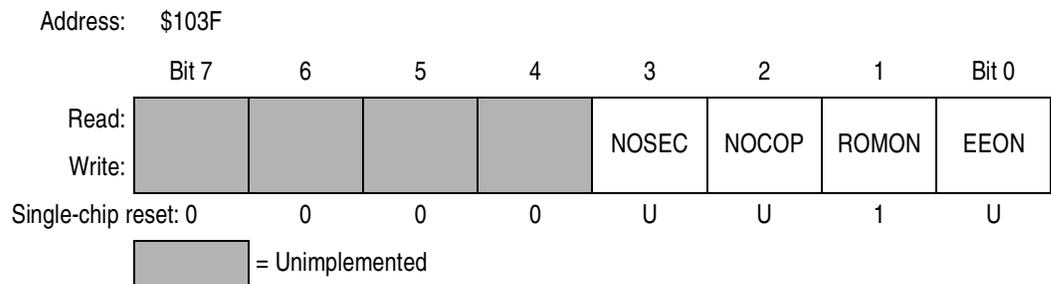
Case 1

Example: CONFIG register

Issue: Some of the bits in the CONFIG register for the MC68HC711E9 are unimplemented.

Change required: Bits 4 –7 in the CONFIG register ($103F) dealt with relocating the EEPROM in the MC68HC811E2. The EEPROM array in the MC68HC711E9 is not re-locatable.
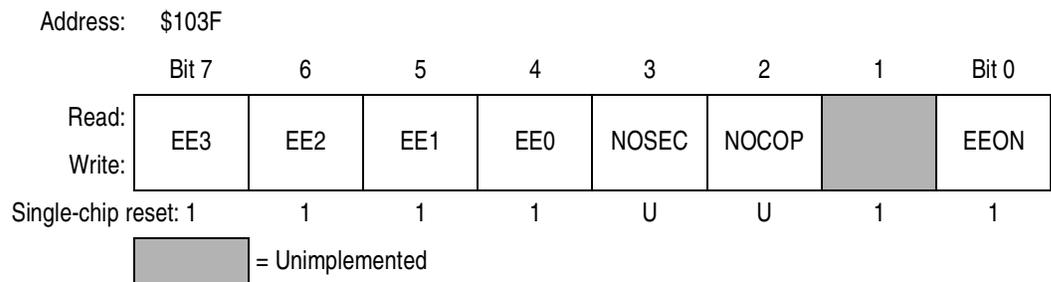
Address: $103F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	EE3	EE2	EE1	EE0	NOSEC	NOCOP		EEON
Single-chip reset:	1	1	1	1	U	U	1	1

= Unimplemented

U indicates a previously programmed bit. U(L) indicates that the bit resets to the logic level held in the latch prior to reset, but the function of COP is controlled by the DISR bit in TEST1 register.

Figure 6. MC68HC811E2 System Configuration Register (CONFIG)

Address: $103F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:					NOSEC	NOCOP	ROMON	EEON
Single-chip reset:	0	0	0	0	U	U	1	U

= Unimplemented

U indicates a previously programmed bit. U(L) indicates that the bit resets to the logic level held in the latch prior to reset, but the function of COP is controlled by the DISR bit in TEST1 register.

Figure 7. MC68HC711E9 System Configuration Register (CONFIG)

Table 4. MC68HC811E2 EEPROM Mapping

EE[3:0]	EEPROM Location
0000	$0800–$0FFF
0001	$1800–$1FFF
0010	$2800–$2FFF
0011	$3800–$3FFF
0100	$4800–$4FFF
0101	$5800–$5FFF
0110	$6800–$6FFF
0111	$7800–$7FFF
1000	$8800–$8FFF
1001	$9800–$9FFF
1010	$A800–$AFFF
1011	$B800–$BFFF
1100	$C800–$CFFF
1101	$D800–$DFFF
1110	$E800–$EFFF
1111	$F800–$FFFF

Summary

For those users using the MC68HC811E2 in the single-chip mode and don't need more than 512 bytes of EEPROM, the MC68HC711E9 is one possible migration path.

For those customers using the 52-pin PLCC package, the MC68HC711E9 is a pin-for-pin compatible part.

Customers also may want to look at migrating to the MC68HC11F1 or the MC68HC812A4 parts if they are re-laying out their application.

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