Mask Set Errata 1

68HC805K3 8-Bit Microcontroller Unit

INTRODUCTION

This errata provides information pertaining to the PA0–PA3 interrupt applicable to the following 68HC805K3 MCU mask set devices:

- 1G40G

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter (e.g., G40G). Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code (e.g., 1G40G).

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code "9115" would indicate the 15th week of the year 1991.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an "SC" or "XC" prefix. An "SC" prefix denotes special/custom device. An "XC" prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the "MC" prefix.

Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

PA0 – PA3 INTERRUPTS

When the 68HC805K3 is configured with port A IRQ enabled (PIRQ = 1 in MOR $12) and the interrupt request option is set to edge-only (LEVIRQ = 0 in MOR $12), the part functions as if the interrupt sensitivity is set to edge-and-level. Therefore, if a constant logic 1 is asserted on PA0–PA3, an interrupt will occur approximately every 1 ms, regardless of f_{OSC}.

NOTE

The $\overline{IRQ}$ pin functions properly.

Additional mask set erratas can be found on the World Wide Web at http://Design-NET.com/csic/TECHSPRT/TechSprt.htm.