

## *Mask Set Errata 1*

# **68HC05M4 8-Bit Microcontroller Unit**

## **INTRODUCTION**

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This errata provides system option register information applicable to the following 68HC05M4 MCU mask set devices:

- 0C10C
- 1C10C

## **MCU DEVICE MASK SET IDENTIFICATION**

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The mask set is identified by a four-character code consisting of a letter, two numerical digits, and a letter (e.g., D85M). Slight variations to the mask set identification code may result in an optional numerical digit preceding the standard four-character code (e.g., 1D85M).

## **MCU DEVICE DATE CODES**

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Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. The date code "9115" would indicate the 15th week of the year 1991.

## **MCU DEVICE PART NUMBER PREFIXES**

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Some MCU samples and devices are marked with an "SC" or "XC" prefix. An "SC" prefix denotes special/custom device. An "XC" prefix denotes device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the "MC" prefix.

*Whenever contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.*

Specifications and information herein are subject to change without notice.



## SYSTEM OPTION REGISTER

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The system option register (location \$2D) contains four one-time programmable write-early bits as shown below.

### System Option Register (\$2D)

|        | Bit 7 | 6    | 5     | 4    | 3   | 2    | 1   | Bit 0 |
|--------|-------|------|-------|------|-----|------|-----|-------|
|        | ADPU  | CSEL | IRQEL | IRQE | CME | COPE | CR1 | CR0   |
| RESET: | 0     | 0    | 1     | 1    | 0   | 1    | 0   | 0     |
| EARLY: |       |      | E     |      |     | E    | E   | E     |

All four one-time programmable write-early bits (bits 0, 1, 2, and 5) must be written during the initial register access and within 68 processor cycles after reset.

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#### NOTE

Simultaneous programming of the four one-time write-early bits must be accomplished within 68 processor cycles after reset.

After the initial register access, subsequent programming of the write-early bits has no effect.

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All remaining bits (bits 3, 4, 6, and 7) can be programmed any time and as often as required.

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