

Mask Set Errata 3

68HC08705C8A 8-Bit Microcontroller Unit

INTRODUCTION

This mask set errata provides information concerning the reading of the security bit on the following MC68HC705C8A MCU mask set devices:

- 0E20T, 1E20T, 2E20T, 3E20T, 4E20T, 5E20T, 6E20T, 7E20T, 8E20T
- 0E79R, 1E79R, 2E79R, 3E79R
- 0K08B
- 1H42K
- 5H72J
- 0J73R

MCU DEVICE MASK SET IDENTIFICATION

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 3J74Y. Slight variations to the mask set identification code may result in an altered version number, for example 4J74Y.

MCU DEVICE DATE CODES

Device markings indicate the week of manufacture and the mask set used. The data is coded as four numerical digits where the first two digits indicate the year and the last two digits indicate the work week. For instance, the date code "9915" indicates the 15th week of the year 1999.

MCU DEVICE PART NUMBER PREFIXES

Some MCU samples and devices are marked with an SC or XC prefix. An SC prefix denotes special/custom device. An XC prefix denotes that the device is tested but is not fully characterized or qualified over the full range of normal manufacturing process variations. After full characterization and qualification, devices will be marked with the MC prefix.

When contacting a Motorola representative for assistance, please have the MCU device mask set and date code information available.

Specifications and information herein are subject to change without notice.




READING THE SECURITY BIT STATUS FROM REGISTER \$1FDF

The reading of bit 3 in the option register (\$1FDF) cannot be considered reliable across the full operating specification. This bit should be considered an unknown by any software reading the option register.

Bit 3 of the option register is a value latched from the EPROM security bit. The EPTOM bit itself is fully functional. It can be written to correctly and is read correctly by security logic. Only when software is reading the option register is the security bit value sometimes misread.

The anomaly is a race condition that most often exhibits itself at cold temperatures and high V_{DD} values.

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