JTAG/IEEE 1149.1 Design Considerations

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SCTA029

TEXAS INSTRUMENTS

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Introduction

The JTAG/IEEE 1149.1 test standard is becoming widely accepted as a way to overcome the problems created by surface-mount packages, double-sided boards, and multichip modules (see Figure 1), all of which result in a loss of physical access to signals on the board. By providing a means to test printed-circuit boards and modules that might otherwise be untestable, the time and cost required to develop a product and bring it to market can be reduced significantly. (see Appendix A for a brief overview of the 1149.1 standard.)

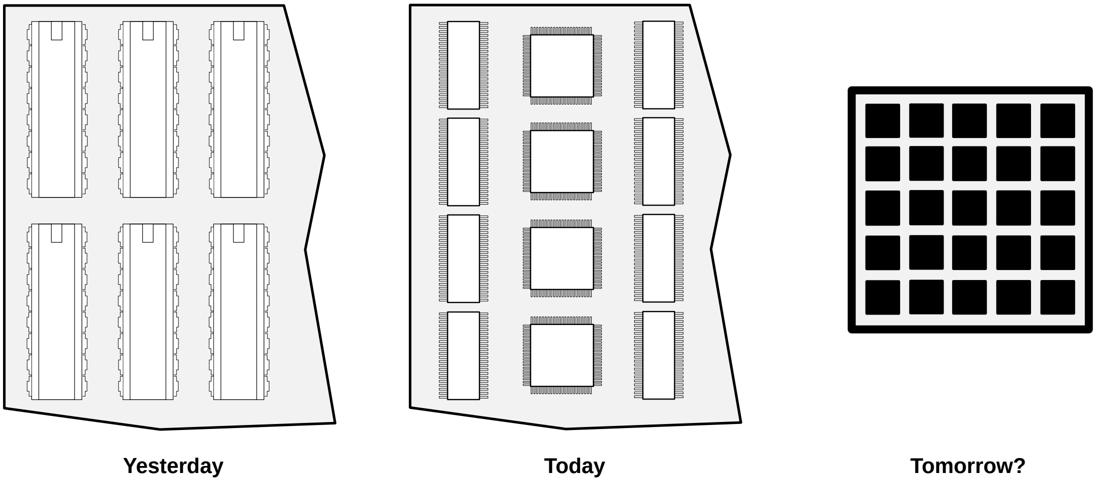


Figure 1. Physical-Access Problem in PCB Designs

The conversion to boundary scan has been readily accepted by many who realize that traditional test methods are not effective in dealing with the issues of decreasing physical access. Their products are such that faults not detected in the factory can be costly to isolate and repair if they surface after they are in the field. These customers see boundary scan as the only solution and have realized cost as well as time-to-market savings, in addition to providing a more reliable product to their customers.

There are others who view boundary scan more skeptically and are uncertain of the ultimate benefits. To help illustrate the potential savings of boundary scan, Table 1 provides a comparative test cost model for an application from the professional product division of Philips Electronics, which involved including boundary scan in their ASICs. Though it doesn't specifically address boundary-scan logic, the benefits to test program generation, testers, fixture costs, etc. apply.

The reader may use this table as a guide to determine the comparative cost savings for his application. In place of the implementation costs for ASICs, you can substitute additional material costs associated with boundary-scan bus interface devices over their nonscan counterparts. In addition to costs savings, there are the benefits of decreased time to market, improved product quality, reduced customer downtime, etc.

Table 1. Comparative Test-Cost Model

	BOUNDARY SCAN	NONBOUNDARY SCAN
Implementation cost (BSR) 200k boards/year, 12 ASICs per PCB, 1% of $25 ASIC	**$600k**	**None**
Test program generation 30 PCB types/year @ $50/hour	50 hours/type = $75k	300 hours/type = $450k
Diagnostics 70% yield of 200k PCBs = 60k PCBs to be repaired @ $25/hour	2 min. per repair = 2k hours = $50k	10 min. per repair = 10k hours = $250k
Number of testers 200k PCBs/year, test time 3 min./PCB = 10k hrs; 3 shifts/tester yields 5k hrs/year/tester	plus diagnostic time and retest = 15k hours = 3 testers	plus diagnostic time and retest = 23k hours = 5 testers
Tester costs Investment = cost of ownership 33%/year	$75k $75k	**$500k** $830k
Fixture costs 30 fixtures	@ $5k = $150k	@ $15k = $450k
Labor cost @ $25/hour	15k hours $375k	23k hours $575k
Yearly total	**$1325k**	**$2555k**

(from: *Boundary-Scan Test, A Practical Approach* by Harry Bleeker, Peter van den Eijnden, and Frans de Jong, 1993)

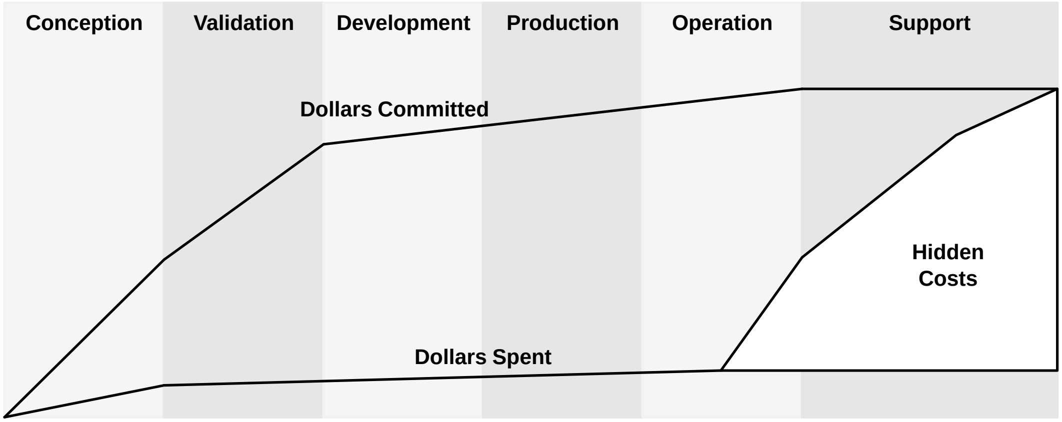
Implementing boundary scan into a design requires a different mindset due to the different hardware, software, and test equipment needs versus traditional test methods, Designers are often uncertain as to exactly how they should begin, what issues must be considered, and what pitfalls await. The purpose of this report is to touch on some of the issues designers should consider when designing with off-the-shelf boundary-scan logic components.

Is JTAG Right for You?

As noted in the introduction, one of the first decisions you will face is whether using boundary scan is of benefit to you. The designer is faced with many issues that must be addressed when implementing boundary scan into a design, versus a design with standard components. A key concern is the fact that boundary-scan devices generally are priced slightly higher than their non-JTAG counterparts. However, as shown in Table 1, there are many situations where the additional material cost of implementing boundary scan is offset by a reduction in life-cycle costs.

Figure 2 provides two views of product life-cycle costs. The lower curve represents actual dollars spent. The upper curve illustrates that development decisions commit funds that other process steps must spend. By the time engineering “releases” a product to manufacturing, 85% of the project’s total costs are committed. These costs are driven by decisions made during the design phase and can only be reduced if they are considered early in the design phase.

Both of the above examples illustrate that the goal of boundary scan is to reduce the product’s life-cycle cost, even though board or system material costs may increase. The life-cycle cost reduction is achieved by enabling faults to be easily identified and isolated, reducing test development and execution time. Further cost reduction is achieved by reducing or eliminating the need for expensive test fixtures and equipment.



(from "Controlling Life-Cycle Costs Through Concurrent Engineering", Addendum to the ATE and Instrumentation Proceedings, Miller Freeman Expositions, 1992)

Figure 2. Life-Cycle Costs of Typical Product

The use of boundary scan can also have a positive impact on time to market, resulting in a maximization of profit potential. These benefits are discussed in greater detail throughout this document.

To make an accurate assessment of the benefits of boundary scan, representatives of all of the disciplines involved in the product's development must discuss their respective problem areas. Only then can a solution be reached that truly addresses the total product life-cycle cost. Several factors can be analyzed to determine the impact of boundary scan on your application:

Boundary Scan Can Reduce PCB Debug Time

By providing access to device I/O without probes, boundary scan allows you to quickly identify and isolate defects to the device and, often, the pin level. Boards that previously may have taken weeks to debug can now be tested in a matter of days or even hours. Additionally, faults that may not have been detected during board test can now be found, preventing faults from surfacing during final test when the costs of finding and repairing the failure are magnified.

Boundary-Scan Components Help Reduce Test Program Development Time

Because tests can be performed independent of device functionality, costly in-circuit test models do not have to be developed. Instead, the user can obtain boundary-scan description language files (BSDL) from the silicon vendor. These files describe how boundary scan has been implemented within the part so tools can understand how to communicate with it. Another key feature of boundary scan is that tests performed at the device level can be rerun at the PCB and system level, reducing or eliminating the need to develop new tests or generate new test vectors. (See Appendix B for examples of how other customers have benefited from the use of boundary scan.)

Boundary Scan Can Reduce the Need for Costly Fixtures

Boundary-scan testing of a PCB only requires the user to access the 4-wire JTAG bus. Thus, a PCB or system can be tested in its normal configuration without the need to develop fixtures for each PCB or subsystem.

Boundary Scan Can Reduce or Eliminate the Need for Test Points

By providing "virtual nails" to each boundary-scannable I/O, the designer no longer needs test points for standard in-circuit testers. Removing these test points reduces board manufacturing cost by reducing the number of board layers required.

Boundary Scan Can Reduce the Number of Pins Needed for In-Circuit Testers

Even if all parts on a PCB do not have boundary scan, all of the benefits discussed here still apply. You may still need to use in-circuit testers to access nonscan nodes. However, by reducing the number of test points needed, you also reduce the number of pins required for the in-circuit tester, which determines the type and cost of the tester needed. The cost of automatic test equipment of this type has risen to as much as $1.5M in the past several years. Reducing the complexity of the tester may mean being able to utilize a tester that is priced significantly less.

Boundary Scan Can Help to Perform Functional Testing

While boundary scan was invented to test for manufacturing defects, users are finding it valuable in doing a variety of functional tests. ASICs and microprocessors can make use of boundary scan to access internal registers and enable testing of the device itself. Clusters of nonscannable logic may be tested by using a boundary-scan device at the cluster input to drive a predetermined pattern. Additional boundary-scan devices at the output can capture the cluster output data and compare it to expected results. In the same manner, other devices such as memories can also be tested.

These are just some of the areas where boundary scan can be of use to you. In some cases you may want to consult with your test or manufacturing engineer to understand the problems they face since, in many cases, designers are unaware of the difficulties their designs pose to others later in the product life cycle.

The degree to which the use of JTAG components impacts your life-cycle development costs will depend on the specifics of your design. While it is not necessary to have a 100% boundary-scan board, the more controllability and observability you can gain by adding boundary-scan devices in key areas, the more benefits you will realize.

Boundary-Scan Training

Whether you are a hardware design engineer, ASIC designer, test engineer, or program manager, there are several options available for learning more about design for test (DFT) and specifically boundary scan. Texas Instruments (TI) has developed several testability training tools to aid you in finding out more about how boundary scan works and how it can benefit you. Some of these are listed below. For more information on available literature and training, please contact your local TI sales representative or authorized distributor.

TI Boundary-Scan Training

Scan Educator (SATB002A)

An educational software program, Scan Educator introduces the fundamentals of the IEEE 1149.1 boundary-scan standard, including architecture, protocol, and required instruction sets.

Self-paced and menu-driven, it contains both information and animated boundary-scan test simulations. Hands-on, practice exercises guide you through boundary-scan test of our SCOPE™ octals at the TAP and at the register level. You are also shown how to use IEEE 1149.1 with single or multiple devices for in-circuit observability and controllability and for interconnect testing.

Testability Primer (SSYA002C)

This pocket-sized book provides an introduction and indispensable reference to JTAG/IEEE 1149.1 testability. It includes discussion of cost benefits/trade-offs associated with design for test, a technical overview of IEEE Std 1149.1 and supporting data formats (BSDL, HSDL, SVF), and a set of application briefs. Summary information on TI silicon testability solutions and support and learning products is also included.

Testability Videotape

This two-part videotape provides a background of the growing need for testability and its economic impact. It also describes the work of JTAG and the provisions of the IEEE 1149.1 standard. Part two of the videotape examines the standard in detail. It explains the function of each component of the standard and shows how they work together to provide an accurate, dependable test procedure.

Testability CD-ROM

TI has assembled the key components of testability on a searchable CD-ROM that includes the IEEE Std 1149.1-1990 and IEEE Std 1149.1a-1993 merged into a single updated document, the TI Test Bus Evaluation Report, application notes on IEEE 1149.1, and device data sheets.

In addition to educational opportunities from TI, other vendors supplying boundary-scan products are usually able to provide training.

For more personal training, TI is also able to hold on-site meetings and seminars tailored to address the needs of your application. Please contact your local TI sales representative or authorized distributor.

Determining Where to Place Boundary-Scan Devices

Once you have become familiar with boundary scan, you will want to integrate it in your design. TI has a broad spectrum of boundary-scan devices available today:

- ASICs
- Fixed and floating-point digital signal processors
- Bus-interface ICs
- Scan-Support ICs

To identify which devices are needed and where they should be placed, there are several questions you should ask:

What Signals Do You Need to Control and Observe?

The boundary-scan standard allows you to take control of an I/O to either sample data at the pin or stimulate the pin with known data. By replacing standard components with JTAG-compliant devices, you can gain access to individual pins for a variety of tests.

Would You Like to Use Boundary Scan to Test Nonscan Logic Clusters?

By having the ability to control and observe device I/O, you can use scannable devices to test devices without JTAG capability. One JTAG device can be loaded with a predetermined pattern that can be driven onto the cluster inputs while additional JTAG devices can capture the output information to be compared against the expected result.

Do You Need Embedded Test Capability?

In support of applications requiring a JTAG controller to be “embedded” within the design, TI has developed devices that can translate parallel commands from a processor into the required JTAG protocol to drive the JTAG bus. For embedded applications, TI has developed a software driver for this bus controller that can be compiled with user code to execute pass/fail tests stored in memory.

Will You Be Implementing Built-in-Self-Test Capability in Your Design?

If you would like to have your board/system execute some form of self test, TI has devices that can help. Within each TI bus interface device lies the ability to execute instructions that command the device to automatically generate output patterns. This capability can reduce or eliminate the need to develop test patterns, as well as significantly reduce the time involved to execute some tests.

What Performance Requirements (Speed, Power, Drive) Are Needed?

The constraints of your design will determine the technology you require in a bus-interface device. TI’s JTAG family contains over 20 devices and crosses a variety of technologies, giving you the ability to pick the device that best suits your needs. Table 2 below provides an example of the performance differences between TI’s BCT and ABT technologies versus competing technology.

Table 2. Performance Comparison, JTAG Transceiver Functions

SPECIFICATION	BCT (TI)	ABT 18-BIT (TI)	FACTQ (NSC)
tp A/B to B/A	10 ns	5.4 ns	8.8 ns
Maximum TCK rate	20 MHz	50 MHz	25 MHz
Number of bits	8	18	18

Based on comparison of TI BCT8245 and ABT18245 vs. NSC SCAN18245.

Will You Require Devices That Operate From 3-V Power?

With more systems moving toward 3-V power, TI has developed 3-V versions of our more popular JTAG Widebus™ devices. These devices are designated as LVTH18xxx. Universal bus transceiver (UBT™) functions are also available now.

Will You Need to Drive JTAG Signals Across a Backplane?

As boundary scan gains acceptance at the board level, the need to perform system-level tests with boundary scan is creating an interesting problem for test engineers. While several approaches have been proposed to date, none addresses the problem better than TI's ABT8996 addressable scan port. This device provides a simple approach to solving a very complex problem without the overhead associated with competing solutions.

What Function Type, Bit Width, or Packaging Limitations Do You Have?

There are many more boundary-scan functions available on the market today than there were even one year ago. Designers are able to select a device based on the functionality, performance, and board area limitations of their design. Boundary-scan buffers, drivers, transceivers, latches, and flip-flops are available in a variety of technologies. TI is the leading supplier of JTAG logic, with over 30 device types available now.

What Type of Test Equipment Do You Expect to Use?

To make the conversion to a test philosophy based on boundary scan, you should define your design, manufacturing, test, and field support flow before beginning hardware design. The details of this test plan will determine the types of tests to be performed, the devices to be used and their placement, and, therefore, the equipment that will be required. There are several vendors supplying CAE and ATE tools to the market today in support of boundary scan.

Will You Need to Use Bare Die for Use in Multichip Modules?

Multichip modules epitomize the problem of no physical access. Boundary scan can be very beneficial by providing you access to internal signals of the MCM. TI supports this effort by supplying bare die for all of its standard components. Additionally, special devices such as the ACT8994 digital bus monitor can give you logic-analyzer capability within the MCM via the JTAG bus.

What Type of Field-Service Requirements Will You Need?

With boundary scan, you now have the ability to access your circuitry via the 4-wire JTAG port without having to totally disassemble the unit. This provides many options to support field maintenance. Will you want the system to execute system self-test and simply notify the end user as to the source of the fault? Or will the system execute self test and then remotely dial back to the factory with the fault? Will a technician go out to the customer site and connect to the JTAG port with boundary-scan diagnostics on a PC to identify the fault? Each of these options and others are available to you because of boundary scan. The option you choose will depend on the ramifications of system downtime to you and your customer and should assist you in determining your use of boundary-scan devices.

The answers to these questions will determine which products you will need, where they should be placed, and what tools and equipment you will require. Additionally, as you begin to understand the types of boundary-scan components that are needed, you will make decisions as to which vendor is best able to support your testability needs. The TI SCOPE family of testability products is the most comprehensive in the industry and is backed by many years of working with customers and other vendors to solve complex testability problems.

Available Literature on TI's JTAG Boundary-Scan Logic Products

The items below contain information on TI's bus-interface and scan-support products that are compatible with the JTAG standard. To obtain a copy of any of these items, please contact your local TI sales representative or authorized distributor.

- Boundary-Scan Logic IEEE Std 1149.1 (JTAG) Data Book 1996 (SCTD002A)
- Testability Primer (SSYA002C)
- Testability CD-ROM
- World Wide Web – URL = http://www.ti.com/sc/docs/jtag/jtaghome.htm

Appendix A – Basics of Boundary Scan

Boundary scan involves placing test points (boundary-scan cells) within each digital I/O of a device. The boundary-scan cell enables the I/O to observe normal data flow through the pin, or the cell can be used to control the state of a pin by providing source data via the serial input (SI). Figure 3 provides a view of the typical boundary-scan cell.

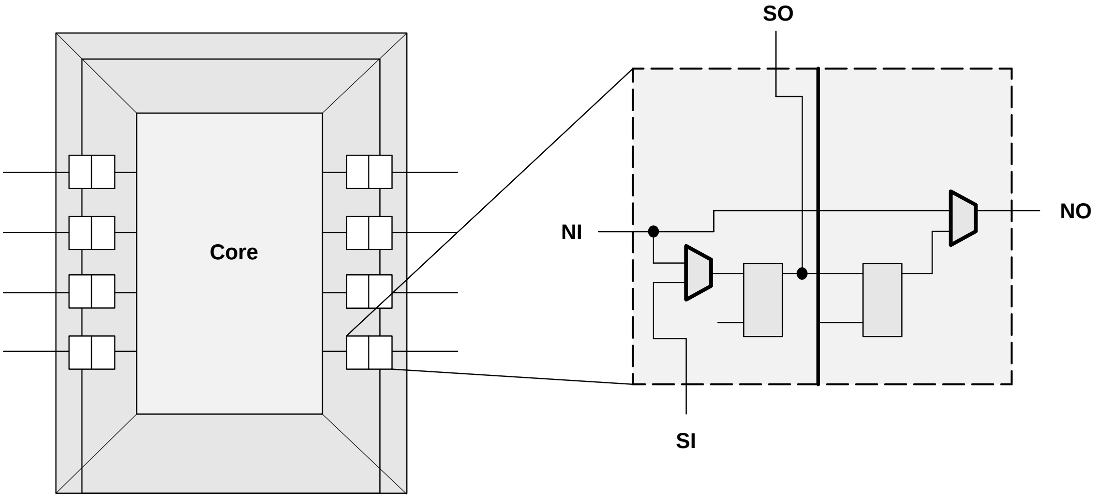


Figure 3. Boundary-Scan Cell

Each boundary-scannable device will contain a minimum of four additional pins:

TDI – test data input
TDO – test data output
TMS – test mode select
TCK – test clock

The TDI and TDO pins serve as the path by which serial data enters and exits the device. The TMS and TCK pins control the state of the device, placing it in either test mode or normal mode. In some cases, an optional fifth pin, test reset (TRST) may be included to reset the test logic and return the device to normal mode. Figure 4 shows these four pins as implemented in one of TI’s SCOPE octals.

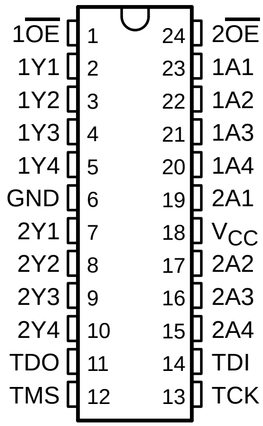
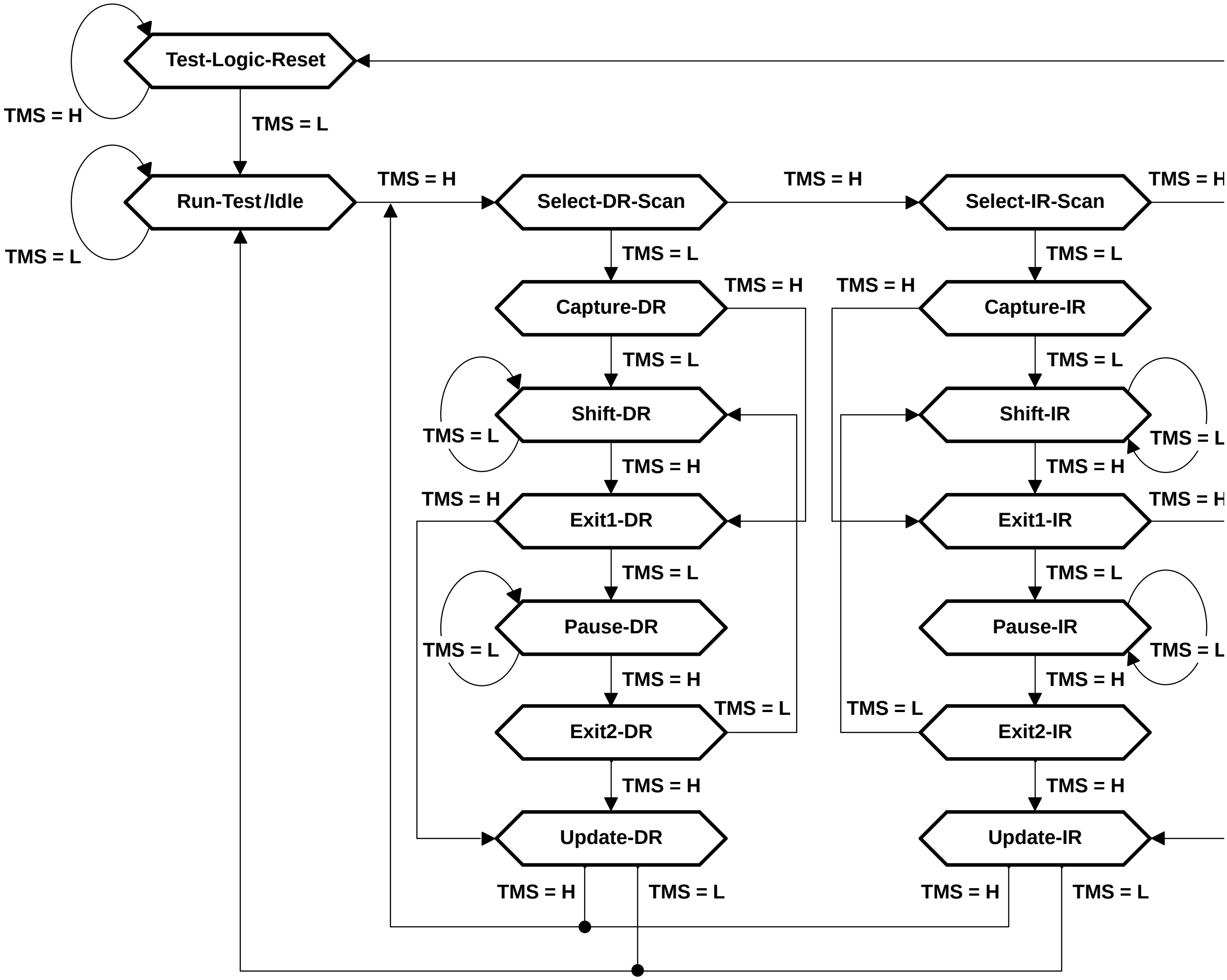


Figure 4. Pinout of TI’s SN74BCT8244

The TMS and TCK signals serve as inputs to control the transition of the device between normal and test modes. These inputs drive a state machine known as the test access port (TAP). The TAP controls serial scanning of instruction or data information through the device and is common to all JTAG/IEEE–1149.1-compliant devices. The TAP state is sequenced based on the state of TMS on the rising edge of TCK, as shown in Figure 5.



TMS input value for state transitions
16-State TAP provides four major operations: RESET, RUN-TEST, SCAN-DR, and SCAN-IR.
Scans consist of three primary steps: CAPTURE, SHIFT, and UPDATE.

Figure 5. TAP-Controller State Diagram

Boundary-scan devices communicate via the serial path from TDO to TDI. This connection is shown in Figure 6. To test the interconnect between two JTAG devices, the user could (for example) serially shift all ones into device 1 and execute an instruction that would drive the data onto the parallel outputs. Device 2 could then be commanded to capture the incoming data at its parallel inputs, transferring the information to the corresponding boundary-scan cells for each input and then serially shift the data to an off-board tester to be compared to the expected results. Any discrepancies in the data can be traced back to the pins where the data mismatch occurs.

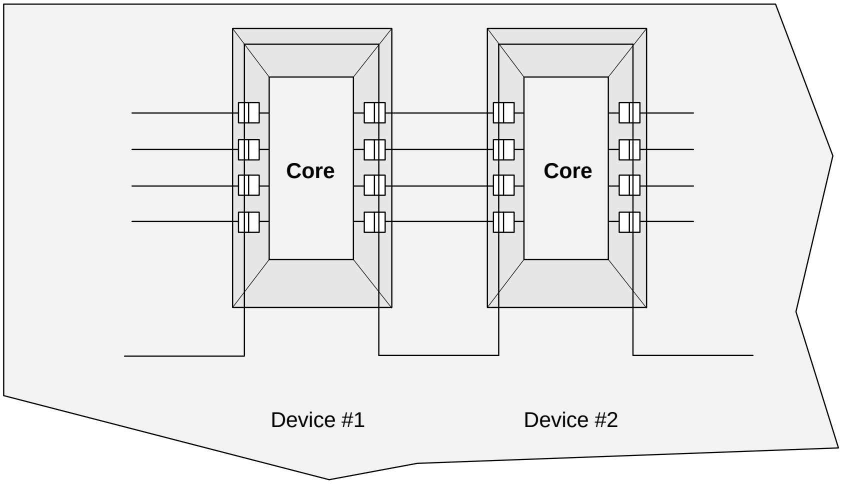


Figure 6. Scan Path Connecting Two Boundary-Scan Devices

For more detailed information on boundary scan, please use the boundary-scan training materials cited in this report.

Appendix B – Boundary-Scan Success Stories

- "We've (AT&T) reduced the number of test points on some boards from 40 down to four and shortened test – debug time on some products from six weeks to two days."[1]

- Hewlett Packard printers reduced the time from the drawing board to production from four and one-half years to two years.[2]

- Test program development time on Intel '386 vs. Intel '486 with JTAG:[3]

Intel '386	Intel '486
7 weeks	10 hours (2 hours if vendor supplied BSDL)

- Controller design company using two programmable logic devices with boundary scan were able to use low-cost tester with ATGP ($25K) instead of standard ATE system ($750K) that would have been used without boundary scan.[4]

[1] Computer Design, January 1994, "Testing Dilemmas and Corporate Alliances Fuel Boundary Scan's Acceptance"

[2] Test and Measurement World, October 1992, "Concurrent Engineering is Common Sense"

[3] Computer Design, November 1992, "Design and Test Engineers Alter Rules to Facilitate Test"

[4] EDN, December 3. 1992. "No 'Accounting' for Boundary Scan Test"