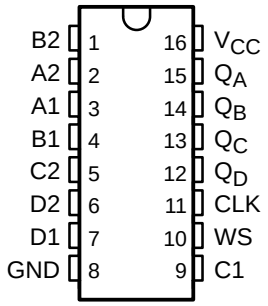
- **Selects One of Two 4-Bit Data Sources and Synchronously Stores Data With System Clock**
- **Applications:**
  - **Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data**
  - **Implements Separate Registers Capable of Parallel Exchange of Contents, Yet Retains External Load Capability**
  - **Has Universal-Type Register for Implementing Various Shift Patterns, Including Compound Left-Right Capability**
- **Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

The SN74AS298A is a quadruple 2-input multiplexer with storage that provides essentially the equivalent functional capabilities of two separate MSI functions (SN74AS157 and ′AS175A) in a 16-pin package.

When the word-select (WS) input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to WS causes the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

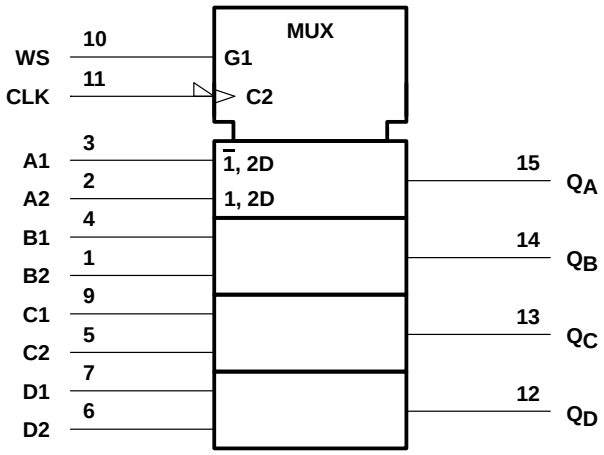
The SN74AS298A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS†			
WS	CLK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

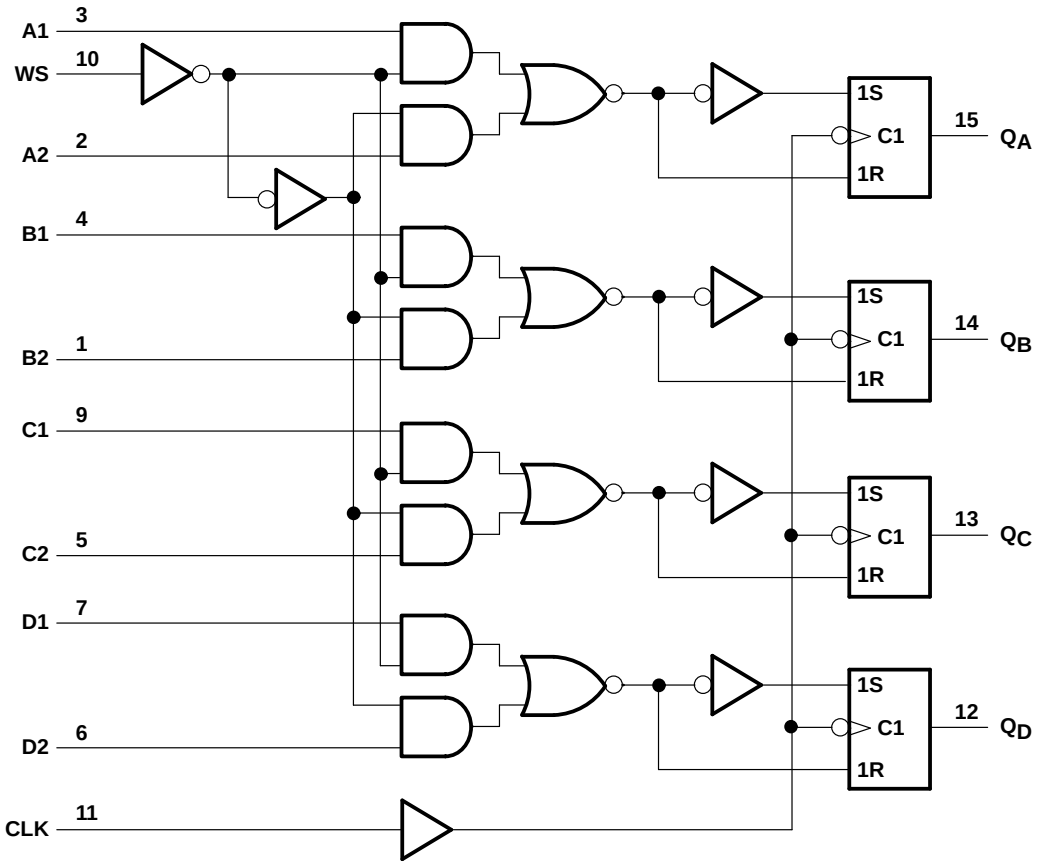
† a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most recent ↓ transition of CLK

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . 65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−2	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	WS	V_{CC} = 5.5 V,	V_I = 2.7 V			40	µA
	All others					20	
I_{IL}	WS	V_{CC} = 5.5 V,	V_I = 0.4 V			−0.75	mA
	All others					−0.5	
I_O§		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			21	33	mA
I_{CCL}		V_{CC} = 5.5 V			22	36	mA

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		0	62	MHz
t_w	Pulse duration, CLK high or low		8		ns
t_{su}	Setup time before CLK↓	Data	4.5		ns
		WS	13		
t_h	Hold time after CLK↓	Data	3.5		ns
		WS	1		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}			62		MHz
t_{PLH}	CLK	Q	2	9	ns
t_{PHL}			1	11	

APPLICATION INFORMATION

This versatile multiplexer can be connected to operate as a shift register that can shift n places in a single clock pulse.

Figure 1 illustrates a BCD shift register that shifts an entire 4-bit BCD digit in one clock pulse.

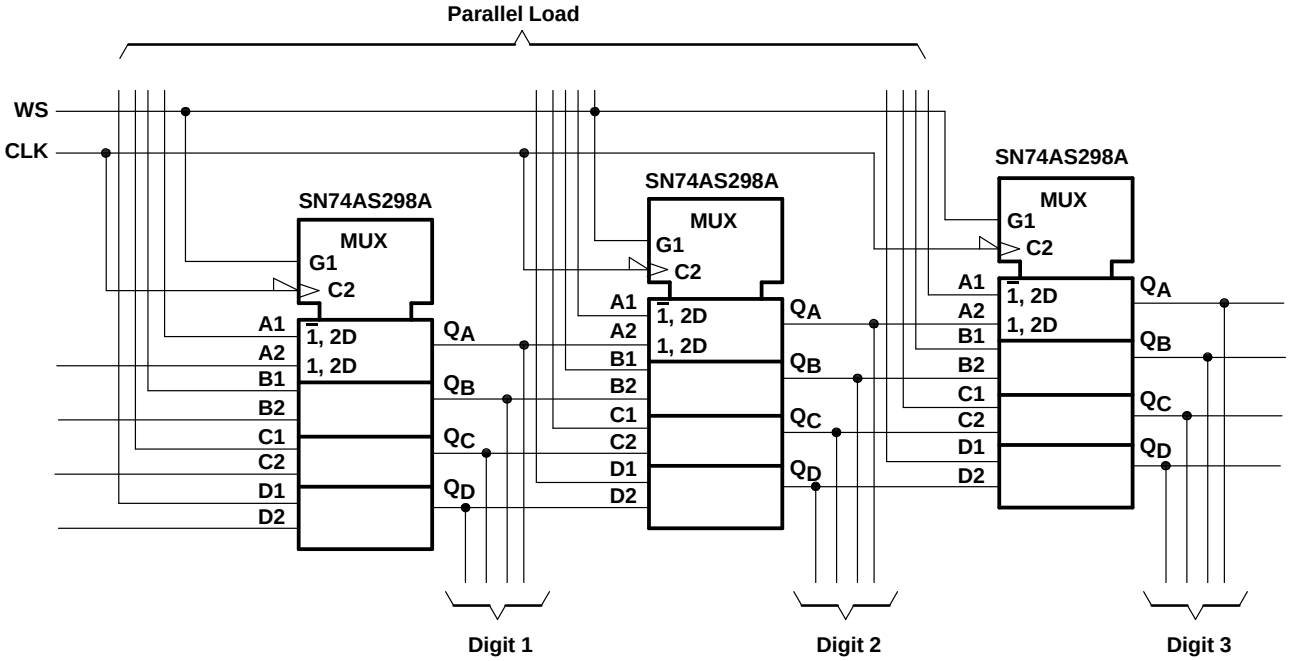


Figure 1. BCD Shift Register

When WS is high and the registers are clocked, the content of register 1 is transferred (shifted) to register 2, etc., effectively shifting the BCD digits one position. This application also retains a parallel-load capability, which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented is a register designed specifically for supporting multiplier or division operations (see Figure 2).

When WS is low and the register is clocked, the outputs of the arithmetic/logic units (ALUs) are shifted one place. When WS is high and the registers are clocked, the data is shifted two places.

APPLICATION INFORMATION

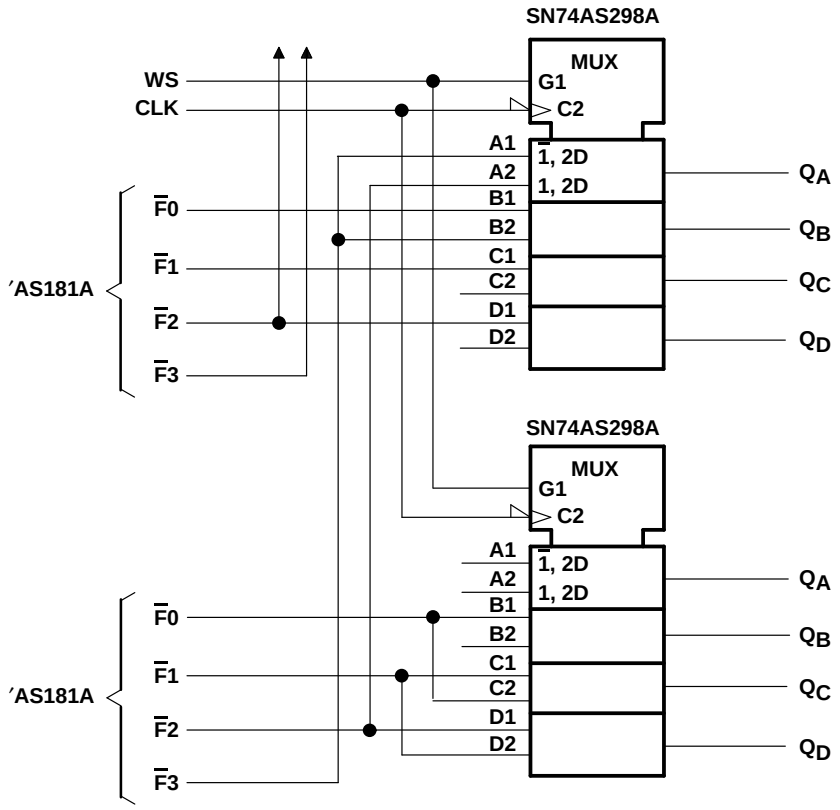
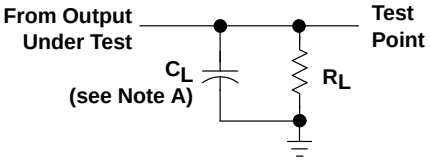
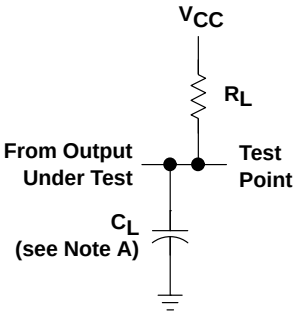


Figure 2. 1-Place/2-Place Shift Register

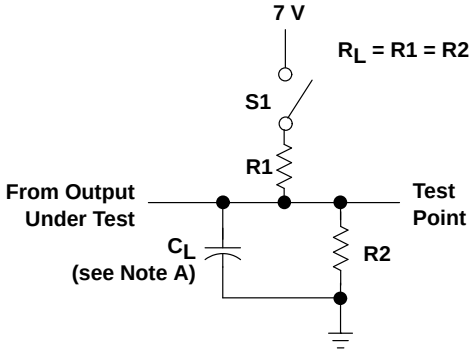
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



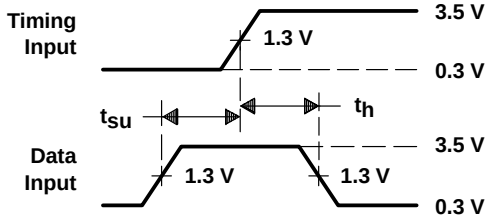
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



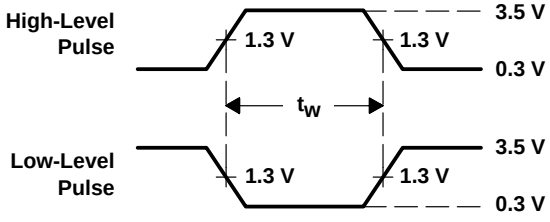
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



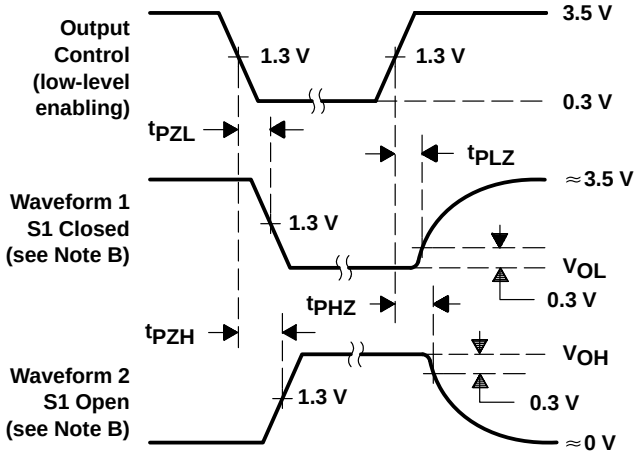
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



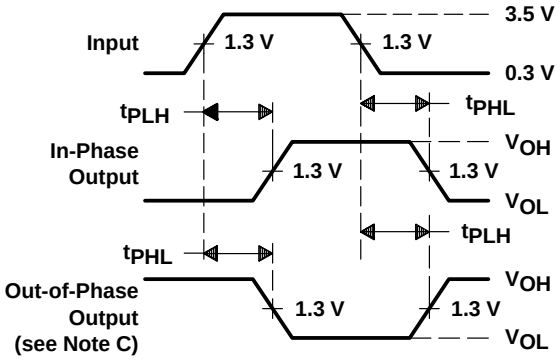
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

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