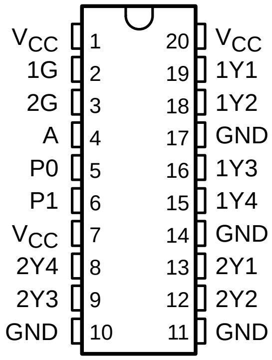
SN54CDC341
1-LINE TO 8-LINE CLOCK DRIVER

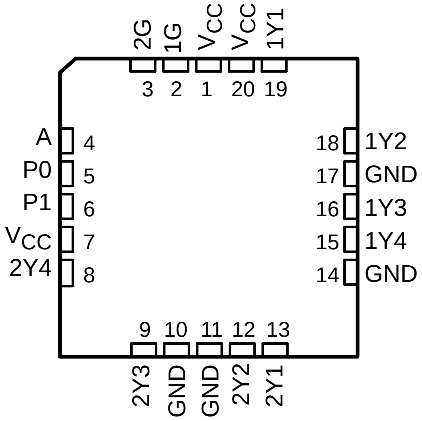
SGAS005 – MARCH 1996

- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Eight Outputs**
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (−48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art *EPIC*-II*B*™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Ceramic Flatpacks (W), Ceramic Chip Carriers (FK), and Ceramic (J) 300-mil DIPS**

J OR W PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



description

The SN54CDC341 is a high-performance clock-driver circuit that distributes one (A) input signal to eight (Y) outputs with minimum skew for clock distribution. Through the use of the control pins (1G and 2G), the outputs can be placed in a low state regardless of the A input.

The propagation delays are adjusted at the factory using the P0 and P1 pins. These pins are not intended for customer use and should be strapped to GND.

The SN54CDC341 is characterized for operation over the full military temperature range of –55°C to 125°C.

FUNCTION TABLE

INPUTS			OUTPUTS	
1G	**2G**	**A**	**1Y1–1Y4**	**2Y1–2Y4**
X	X	L	L	L
L	L	H	L	L
L	H	H	L	H
H	L	H	H	L
H	H	H	H	H

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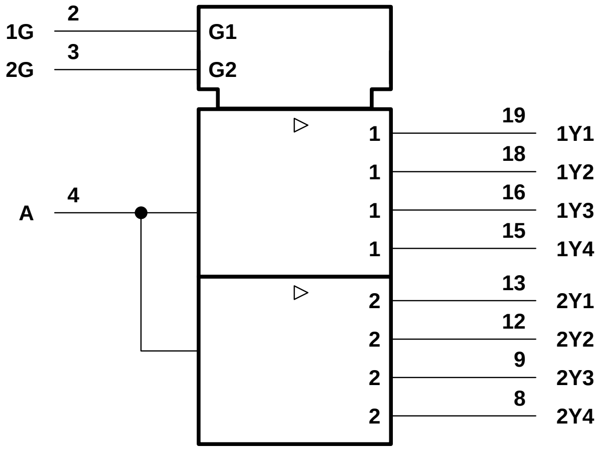
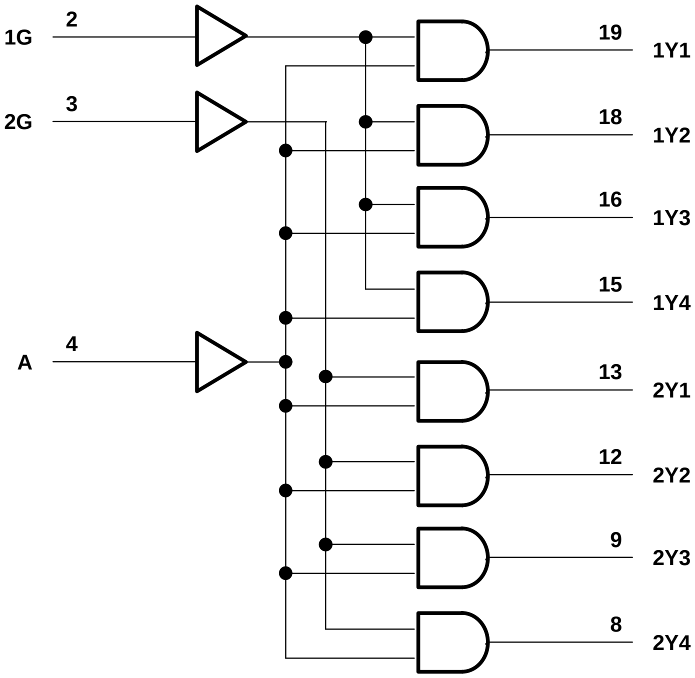
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1)	–0.5 V to V_{CC} + 0.5 V
Current into any output in the low state, I_O	96 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions (see Note 2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_I	Input voltage	0	V_{CC}	V
I_{OH}	High-level output current		–48	mA
I_{OL}	Low-level output current		48	mA
f_{clock}	Input clock frequency		80	MHz
T_A	Operating free-air temperature	–55	125	°C

NOTE 2: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = – 3 mA		2.5		V
	V_{CC} = 5 V,	I_{OH} = – 3 mA		3		
	V_{CC} = 4.5 V,	I_{OH} = – 48 mA		2		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA			0.5	V
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1	µA
I_O[‡]	V_{CC} = 5.5 V,	V_O = 2.5 V		–50	–200	mA
I_{CC}	V_{CC} = 5.5 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		3.5	mA
			Outputs low		33	
C_i	V_I = 2.5 V or 0.5 V					pF

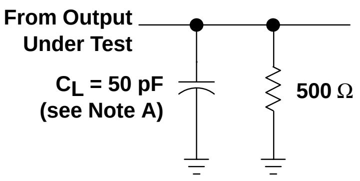
[‡] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

switching characteristics, C_L = 50 pF (see Figures 1 and 2)

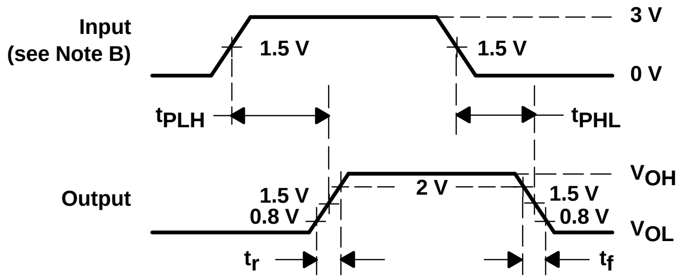
PARAMETER	FROM (INPUT)	TO (OUTPUT)	PACKAGE	V_{CC} = 5 V, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, T_A = –55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	All	2.3		6.7	1.8	7	ns
t_{PHL}				3.6		6.3	3.3	7	
t_{PLH}	G	Y	All	1.6		4.1	1.3	4.7	ns
t_{PHL}				2.3		4.4	1.8	4.9	
$t_{sk(o)}$	A	Y	J			1.8		1.9	ns
			W			0.7		1.9	
			FK			0.6		0.8	
	G	Y	J			0.9		0.9	ns
			W			0.5		1.2	
			FK			0.6		0.7	
$t_{sk(p)}$	A	Y	J			1.7		1.7	ns
			W			1.4		1.7	
			FK			1.7		2.1	
	G	Y	J			1		1	ns
			W			0.6		1.3	
			FK			1.3		1.8	
$t_{sk(pr)}$†	A or G	Y				1.2		1.2	ns

† tsk$_{(pr)}$ is guaranteed across the full voltage and temperature range but is measured only at 25C, V_{CC} = 5 V, using the A inputs.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

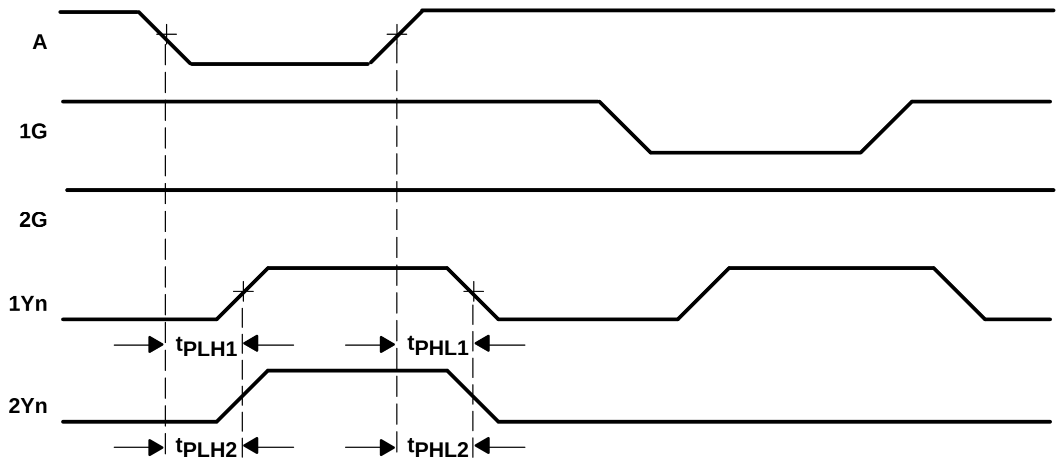


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:

- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2)
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2)

B. Pulse skew, $t_{sk(p)}$, is calculated as the greater of | $t_{PLHn} - t_{PHLn}$ | (n = 1, 2).

C. Process skew, $t_{sk(pr)}$, is calculated as the greater of:

- The difference between the fastest and slowest of t_{PLHn} (n = 1, 2) across multiple devices under identical operating conditions
- The difference between the fastest and slowest of t_{PHLn} (n = 1, 2) across multiple devices under identical operating conditions

Figure 2. Waveforms for Calculation of $t_{sk(o)}$, $t_{sk(p)}$, $t_{sk(pr)}$

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