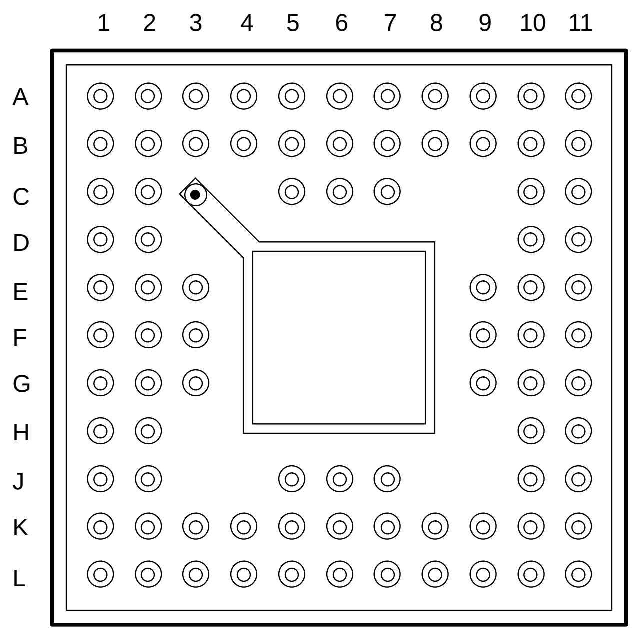
- **Member of the Texas Instruments Widebus™ Family**
- **Independent Asynchronous Inputs and Outputs**
- **Produced in Advanced BiCMOS Technology**
- **Two Separate 512 × 18 FIFOs Buffering Data in Opposite Directions**
- **Programmable Almost-Full/Almost-Empty Flags**
- **Empty, Full, and Half-Full Flags**
- **Fast Access Times of 12 ns With a 50-pF Load and Simultaneous Switching Data Outputs**
- **Available in 84-Pin Ceramic Pin Grid Array (GB)**

GB PACKAGE
(TOP VIEW)



description

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. The SN54ABT7820 is arranged as two 512 × 18-bit FIFOs for high speed and fast access times. It processes data at rates from 0 to 67 MHz with access times of 12 ns in a bit-parallel format.

The SN54ABT7820 consists of bus transceiver circuits, two 512 × 18 FIFOs, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal FIFO memories. Enable inputs GAB and GBA control the transceiver functions. The SAB and SBA control inputs select whether real-time or stored data is transferred. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. Figure 1 illustrates the eight fundamental bus-management functions that can be performed with the SN54ABT7820.

The SN54ABT7820 is characterized for operation from –55°C to 125°C.

Widebus is a trademark of Texas Instruments Incorporated.

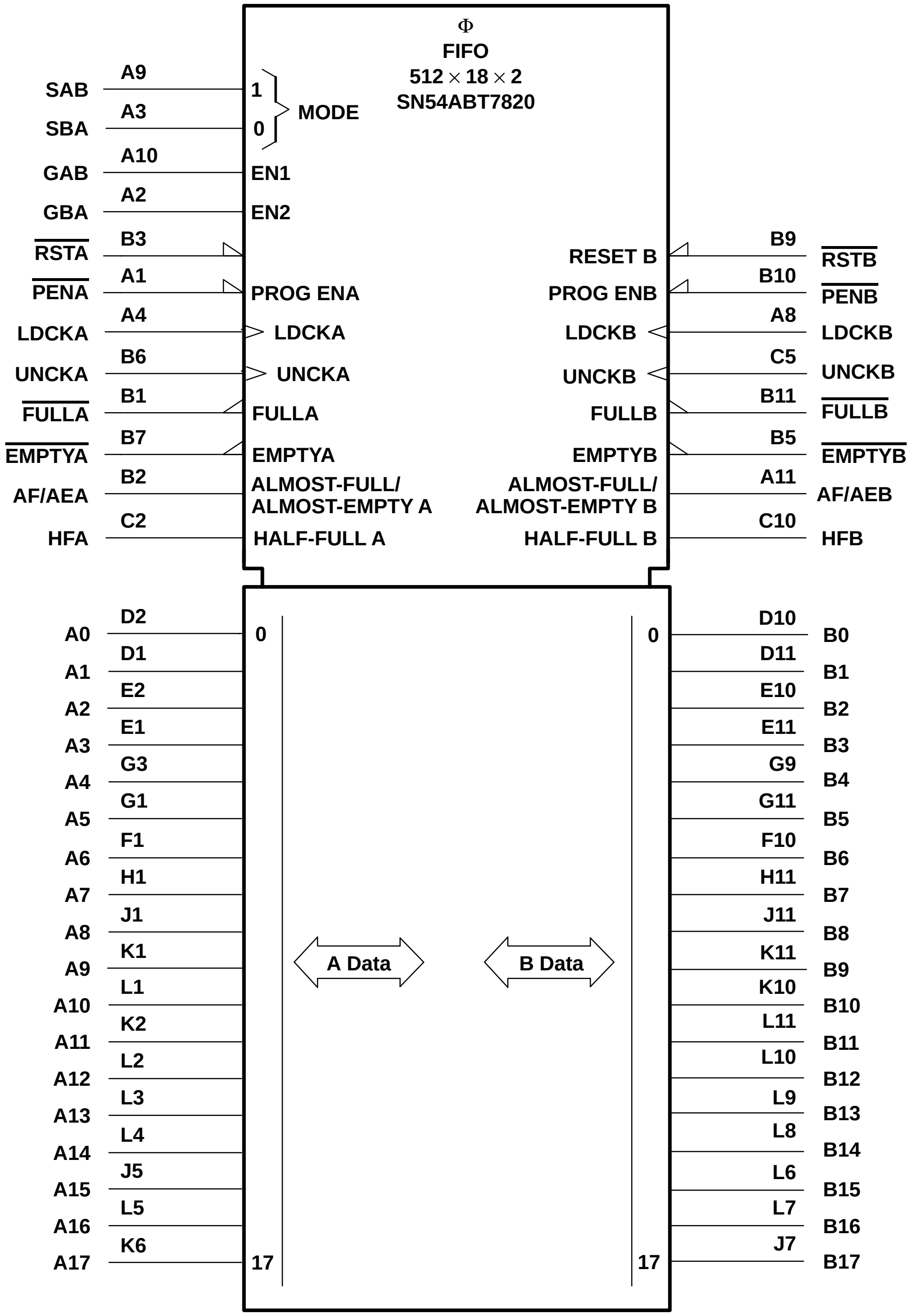
Terminal Assignments

TERMINAL	NAME	TERMINAL	NAME	TERMINAL	NAME	TERMINAL	NAME
A1	$\overline{\text{PENA}}$	B11	$\overline{\text{FULLB}}$	F9	NC	K2	A11
A2	GBA	C1	GND	F10	B6	K3	GND
A3	SBA	C2	HFA	F11	GND	K4	V_{CC}
A4	LDCKA	C5	UNCKB	G1	A5	K5	GND
A5	V_{CC}	C6	NC	G2	GND	K6	A17
A6	V_{CC}	C7	V_{CC}	G3	A4	K7	GND
A7	V_{CC}	C10	HFB	G9	B4	K8	V_{CC}
A8	LDCKB	C11	GND	G10	GND	K9	GND
A9	SAB	D1	A1	G11	B5	K10	B10
A10	GAB	D2	A0	H1	A7	K11	B9
A11	AF/AEB	D10	B0	H2	GND	L1	A10
B1	$\overline{\text{FULLA}}$	D11	B1	H10	GND	L2	A12
B2	AF/AEA	E1	A3	H11	B7	L3	A13
B3	$\overline{\text{RSTA}}$	E2	A2	J1	A8	L4	A14
B4	GND	E3	V_{CC}	J2	V_{CC}	L5	A16
B5	$\overline{\text{EMPTYB}}$	E9	V_{CC}	J5	A15	L6	B15
B6	UNCKA	E10	B2	J6	NC	L7	B16
B7	$\overline{\text{EMPTYA}}$	E11	B3	J7	B17	L8	B14
B8	GND	F1	A6	J10	V_{CC}	L9	B13
B9	$\overline{\text{RSTB}}$	F2	GND	J11	B8	L10	B12
B10	$\overline{\text{PENB}}$	F3	NC	K1	A9	L11	B11

Terminal Functions

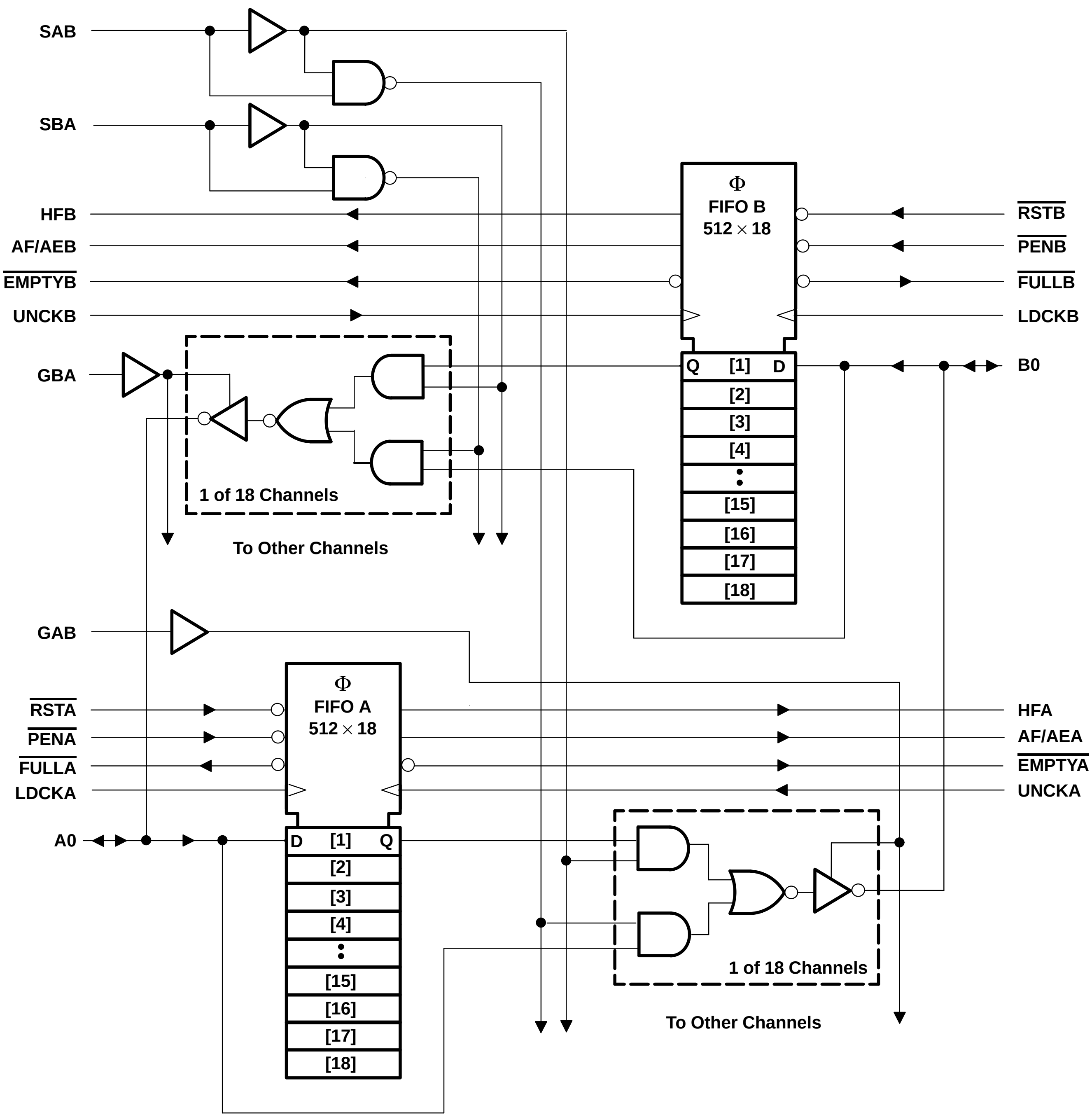
TERMINAL NAME	I/O	DESCRIPTION
A0 – A17	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	O	FIFO A almost-full/almost-empty flag. Depth offset values can be programmed for AF/AEA, or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when FIFO A contains X or less words or (512 – Y) or more words. AF/AEA is set high after FIFO A is reset.
AF/AEB	O	FIFO B almost-full/almost-empty flag. Depth offset values can be programmed for AF/AEB, or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when FIFO B contains X or less words or (512 – Y) or more words. AF/AEB is set high after FIFO B is reset.
B0 – B17	I/O	Port-B data. The 18-bit bidirectional data port for side B.
$\overline{\text{EMPTYA}}$	O	FIFO A empty flag. $\overline{\text{EMPTYA}}$ is low when FIFO A is empty and is high when FIFO A is not empty. $\overline{\text{EMPTYA}}$ is set low after FIFO A is reset.
$\overline{\text{EMPTYB}}$	O	FIFO B empty flag. $\overline{\text{EMPTYB}}$ is low when FIFO B is empty and is high when FIFO B is not empty. $\overline{\text{EMPTYB}}$ is set low after FIFO B is reset.
$\overline{\text{FULLA}}$	O	FIFO A full flag. $\overline{\text{FULLA}}$ is low when FIFO A is full and is high when FIFO A is not full. $\overline{\text{FULLA}}$ is set high after FIFO A is reset.
$\overline{\text{FULLB}}$	O	FIFO B full flag. $\overline{\text{FULLB}}$ is low when FIFO B is full and is high when FIFO B is not full. $\overline{\text{FULLB}}$ is set high after FIFO B is reset.
GAB	I	Port-B output enable. B0 – B17 outputs are active when GAB is high and are in the high-impedance state when GAB is low.
GBA	I	Port-A output enable. A0 – A17 outputs are active when GBA is high and are in the high-impedance state when GBA is low.
HFA	O	FIFO A half-full flag. HFA is high when FIFO A contains 256 or more words and is low when FIFO A contains 255 or fewer words. HFA is set low after FIFO A is reset.
HFB	O	FIFO B half-full flag. HFB is high when FIFO B contains 256 or more words and is low when FIFO B contains 255 or fewer words. HFB is set low after FIFO B is reset.
LDCKA	I	FIFO A load clock. Data is written into FIFO A on a low-to-high transition of LDCKA when $\overline{\text{FULLA}}$ is high. The first word written into an empty FIFO A is sent directly to the FIFO A data outputs.
LDCKB	I	FIFO B load clock. Data is written into FIFO B on a low-to-high transition of LDCKB when $\overline{\text{FULLB}}$ is high. The first word written into an empty FIFO B is sent directly to the FIFO B data outputs.
$\overline{\text{PENA}}$	I	FIFO A program enable. After $\overline{\text{reset}}$ and before a word is written into FIFO A, the binary value on A0 – A7 is latched as an AF/AEA offset value when $\overline{\text{PENA}}$ is low and LDCKA is high.
$\overline{\text{PENB}}$	I	FIFO B program enable. After $\overline{\text{reset}}$ and before a word is written into FIFO B, the binary value on B0 – B7 is latched as an AF/AEB offset value when $\overline{\text{PENB}}$ is low and LDCKB is high.
$\overline{\text{RSTA}}$	I	FIFO A reset. A low level on $\overline{\text{RSTA}}$ resets FIFO A forcing $\overline{\text{EMPTYA}}$ low, HFA low, $\overline{\text{FULLA}}$ high, and AF/AEA high.
$\overline{\text{RSTB}}$	I	FIFO B reset. A low level on $\overline{\text{RSTB}}$ resets FIFO B forcing $\overline{\text{EMPTYB}}$ low, HFB low, $\overline{\text{FULLB}}$ high, and AF/AEB high.
SAB	I	Port-B read select. SAB selects the source of B0 – B17 read data. A low level selects real-time data from A0 – A17. A high level selects the FIFO A output.
SBA	I	Port-A read select. SBA selects the source of A0 – A17 read data. A low level selects real-time data from B0 – B17. A high level selects the FIFO B output.
UNCKA	I	FIFO A unload clock. Data is read from FIFO A on a low-to-high transition of UNCKA when $\overline{\text{EMPTYA}}$ is high.
UNCKB	I	FIFO B unload clock. Data is read from FIFO B on a low-to-high transition of UNCKB when $\overline{\text{EMPTYB}}$ is high.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



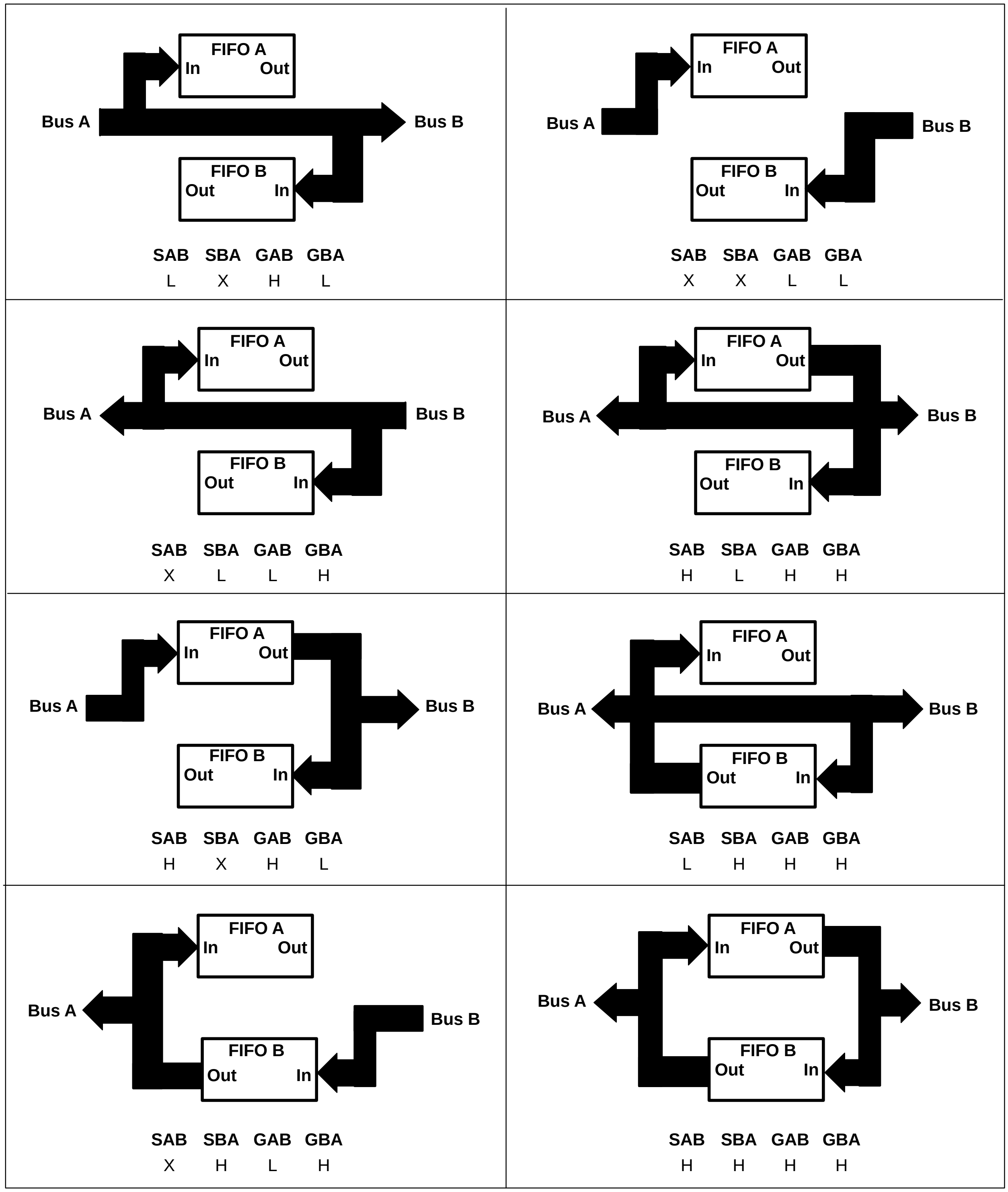


Figure 1. Bus-Management Functions

SELECT-MODE CONTROL TABLE

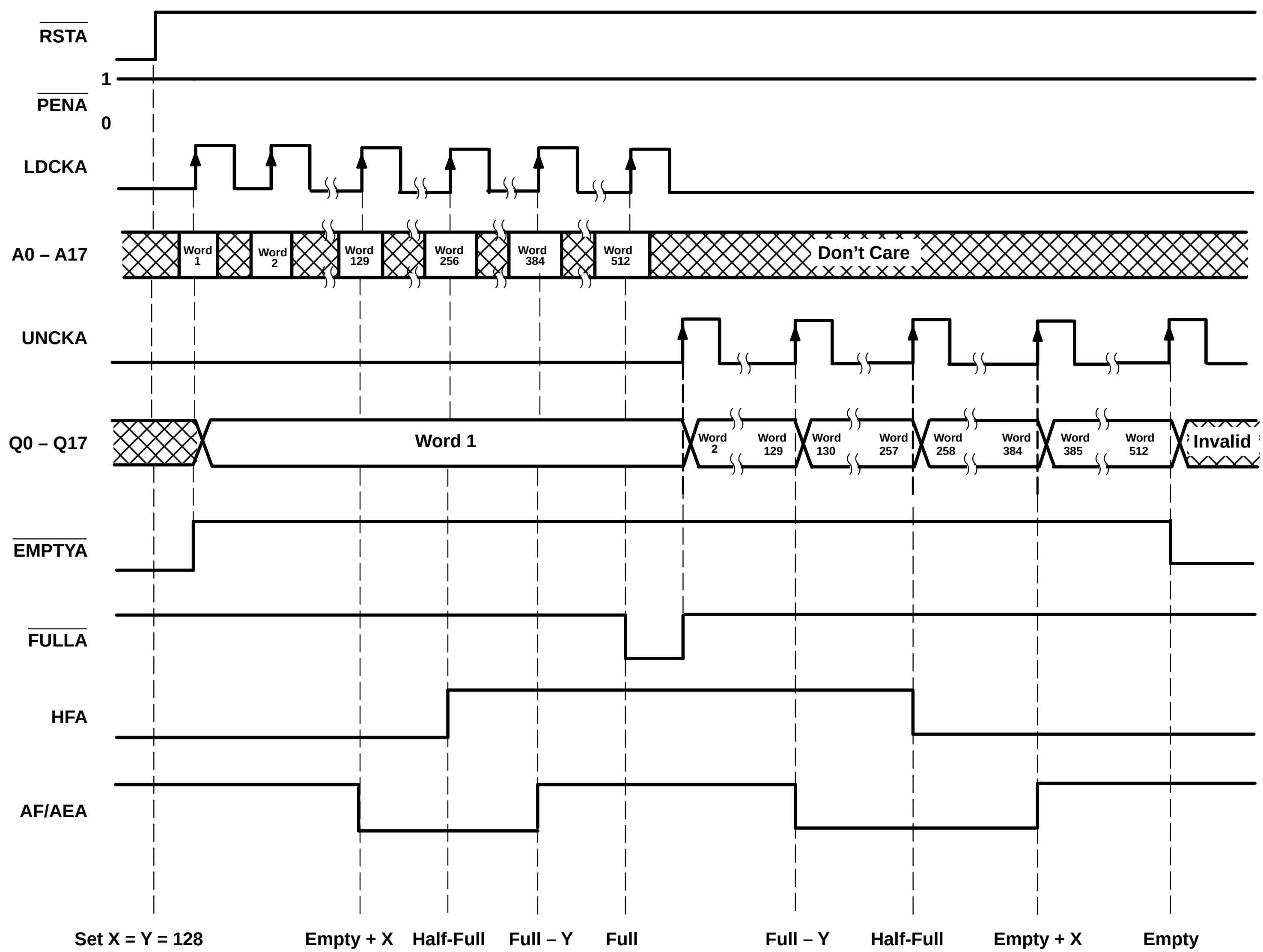
CONTROL		OPERATION	
SBA	SAB	A BUS	B BUS
L	L	Real-time B to A bus	Real-time A to B bus
H	L	FIFO B to A bus	Real-time A to B bus
L	H	Real-time B to A bus	FIFO A to B bus
H	H	FIFO B to A bus	FIFO A to B bus

OUTPUT-ENABLE CONTROL TABLE

CONTROL		OPERATION	
GBA	GAB	A BUS	B BUS
L	L	Isolation/input to A bus	Isolation/input to B bus
H	L	A bus enabled	Isolation/input to B bus
L	H	Isolation/input to A bus	B bus enabled
H	H	A bus enabled	B bus enabled

Figure 1. Bus-Management Functions (Continued)

timing diagram for FIFO A†



† SAB = GAB = H, GBA = L

Operation of FIFO B is identical to that of FIFO A.

offset values for AF/AE

The almost-full/almost-empty (AF/AE) flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). The offsets of a flag can be programmed from the input of its FIFO after it is reset and before any data is written to its memory. An AF/AE flag is high when its FIFO contains X or fewer words or (512 – Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ can be brought low after FIFO A is reset and only when LDCKA is low. On the following low-to-high transition of LDCKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of LDCKA reprograms Y to the binary value on A0–A7 at the time of the second LDCKA low-to-high transition.

$\overline{\text{PENA}}$ can be brought back high only when LDCKA is low during the first two LDCKA cycles. $\overline{\text{PENA}}$ can be brought high at any time after the second LDCKA pulse returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 2). To use the default values of X = Y = 128 for AF/AEA, $\overline{\text{PENA}}$ must be tied high. No data is stored in the FIFO when its AF/AE offsets are programmed.

The AF/AEB flag is programmed in the same manner. $\overline{\text{PENB}}$ enables LDCKB to program the AF/AEB offset values taken from B0–B7.

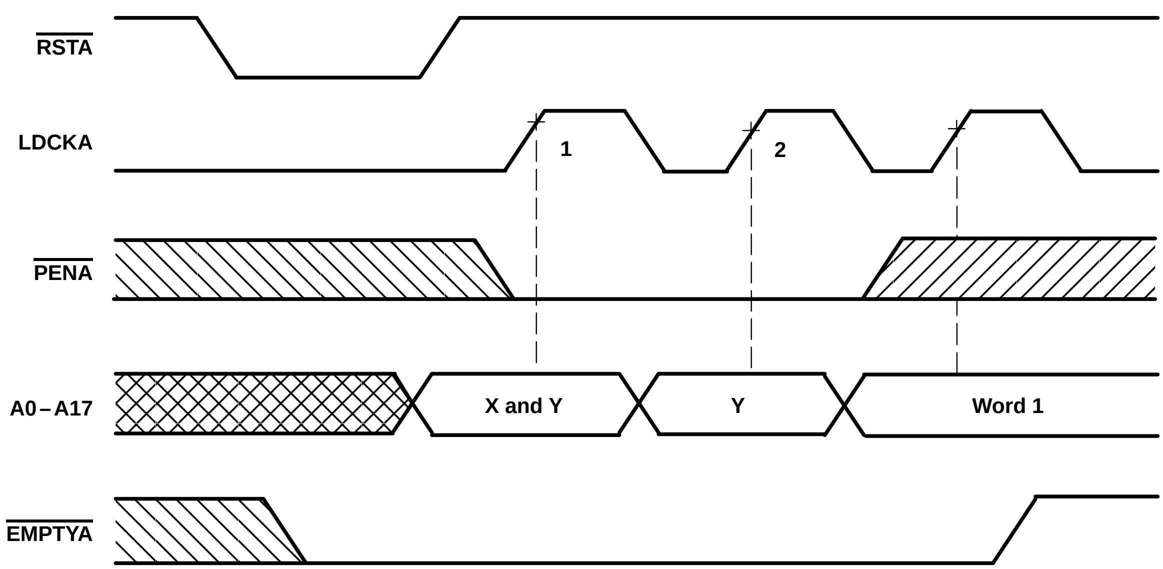


Figure 2. Programming X and Y Separately for AF/AEA

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . –0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . 48 mA
Input clamp current, I_{IK} (V_I < 0) . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . –50 mA
Operating free-air temperature range, T_A . . . . –55°C to 125°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	4.5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature	–55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = – 18 mA					– 1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 3 mA			2.5			V
		V_{CC} = 5 V,	I_{OH} = – 3 mA			3			
		V_{CC} = 4.5 V,	I_{OH} = – 12 mA			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 24 mA					0.55	V
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or GND					±5	µA
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V					50	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V					– 50	µA
I_O¶		V_{CC} = 5.5 V,	V_O = 2.5 V			– 40	– 100	– 180	mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0,	V_I = V_{CC} or GND	Outputs high			15	mA
					Outputs low			95	
					Outputs disabled			15	
C_i	Control inputs	V_I = 2.5 V or 0.5 V					6		pF
C_o	Flags	V_O = 2.5 V or 0.5 V					4		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V					8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency		40		MHz
t_w	Pulse duration	LDCKA, LDCKB high	9		ns
		LDCKA, LDCKB low	9		
		UNCKA, UNCKB high	9		
		UNCKA, UNCKB low	9		
		$\overline{RSTA}$, $\overline{RSTB}$ low	10		
t_{su}	Setup time	A0–A17 before LDCKA↑ and B0–B17 before LDCKB↑	4		ns
		$\overline{PENA}$ before LDCKA↑ and $\overline{PENB}$ before LDCKB↑	6		
		LDCKA inactive before $\overline{RSTA}$ high and LDCKB inactive before $\overline{RSTB}$ high	4		
t_h	Hold time	A0–A17 after LDCKA↑ and B0–B17 after LDCKB↑	0		ns
		$\overline{PENA}$ after LDCKA low and $\overline{PENB}$ after LDCKB low	3		
		LDCKA inactive after $\overline{RSTA}$ high and LDCKB inactive after $\overline{RSTB}$ high	4		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	LDCK, UNCK			40	MHz
t_{pd}	LDCKA↑, LDCKB↑	B/A	3	18	ns
	UNCKA↑, UNCKB↑		3	15	
t_{PLH}	LDCKA↑, LDCKB↑	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	3	17	ns
t_{PHL}	UNCKA↑, UNCKB↑		3	16	
t_{PHL}	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low	$\overline{\text{EMPTYA}}$, $\overline{\text{EMPTYB}}$	5	18	ns
t_{PHL}	LDCKA↑, LDCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	5	16	ns
t_{PLH}	UNCKA↑, UNCKB↑	$\overline{\text{FULLA}}$, $\overline{\text{FULLB}}$	5	17	ns
	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low		7	22	
t_{pd}	LDCKA↑, LDCKB↑	AF/AEA, AF/AEB	7	18	ns
	UNCKA↑, UNCKB↑		7	18	
t_{PLH}	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low	AF/AEA, AF/AEB	1	16	ns
t_{PLH}	LDCKA↑, LDCKB↑	HFA, HFB	6	17	ns
t_{PHL}	UNCKA, UNCKB	HFA, HFB	7	17	ns
	$\overline{\text{RSTA}}$ low, $\overline{\text{RSTB}}$ low		1	16	
t_{pd}	SAB/SBA‡	B/A	1	12	ns
	A/B		1	11	
t_{en}	GBA/GAB	A/B	1	10	ns
t_{dis}	GBA/GAB	A/B	1	13	ns

† All typical values are at 5 V, T_A = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

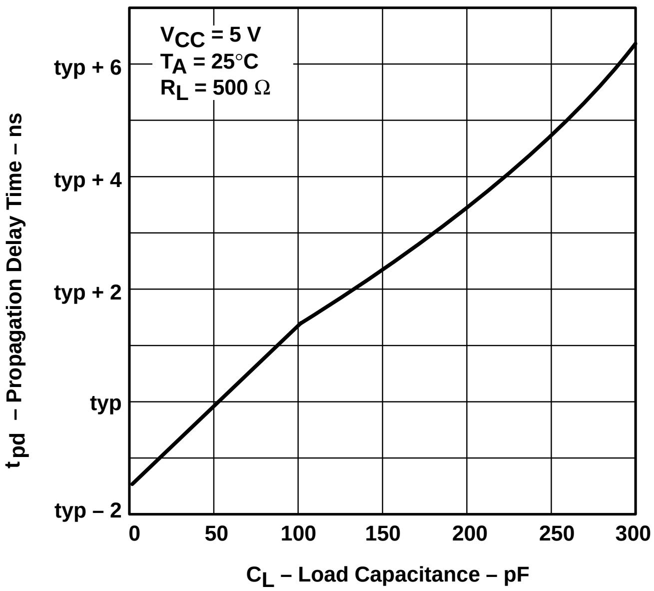


Figure 3

SUPPLY CURRENT
vs
CLOCK FREQUENCY

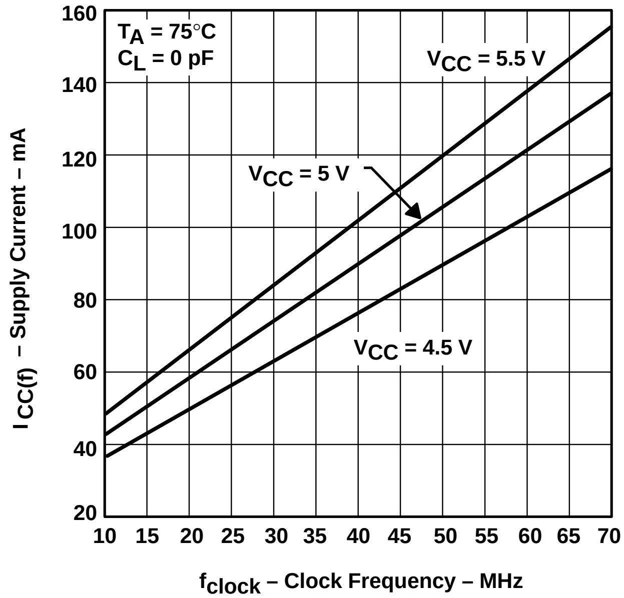


Figure 4

calculating power dissipation

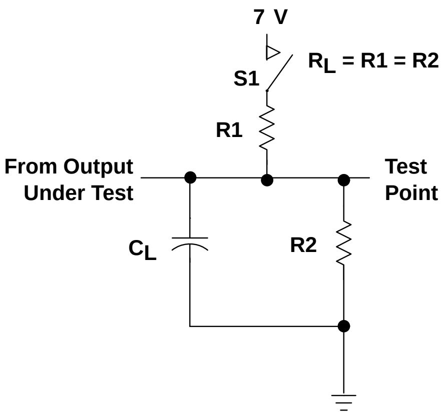
With $I_{CC(f)}$ taken from Figure 4, the maximum power dissipation (P_T) based on all outputs changing states on each read can be calculated by:

$$P_T = V_{CC} \times I_{CC(f)} + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

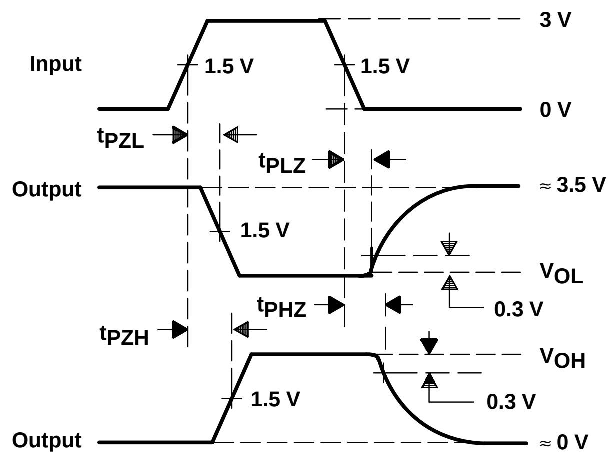
where:

$I_{CC(f)}$ = maximum I_{CC} per clock frequency
C_L = output capacitive load
f_o = data output frequency

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

PARAMETER		R1, R2	C_L†	S1
t_{en}	t_{PZH}	500 Ω	50 pF	Open
	t_{PZL}			Closed
t_{dis}	t_{PHZ}	500 Ω	50 pF	Open
	t_{PLZ}			Closed
t_{pd}		500 Ω	50 pF	Open

† Includes probe and test-fixture capacitance

Figure 5. Load Circuit and Voltage Waveforms