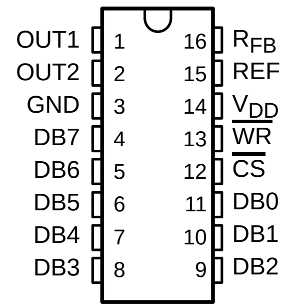
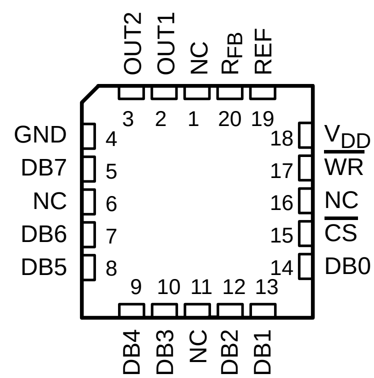
- **Advanced LinCMOS™ Silicon-Gate Technology**
- **Easily interfaced to Microprocessors**
- **On-Chip Data Latches**
- **Monotonicity Over Entire A/D Conversion Range**
- **Segmented High-Order Bits Ensure Low-Glitch Output**
- **Designed to Be interchangeable With Analog Devices AD7524, PMI PM-7524, and Micro Power Systems MP7524**
- **Fast Control Signaling for Digital Signal Processor Applications Including Interface With TMS320**

N PACKAGE
(TOP VIEW)



AD7524J . . . FN PACKAGE
(TOP VIEW)



NC–No internal connection

KEY PERFORMANCE SPECIFICATIONS	
Resolution	8 Bits
Linearity error	1/2 LSB Max
Power dissipation at V_{DD} = 5 V	5 mW Max
Settling time	100 ns Max
Propagation delay	80 ns Max

description

The AD7524 is an Advanced LinCMOS™ 8-bit digital-to-analog converter (DAC) designed for easy interface to most popular microprocessors.

The AD7524 is an 8-bit multiplying DAC with input latches and with a load cycle similar to the write cycle of a random access memory. Segmenting the high-order bits minimizes glitches during changes in the most significant bits, which produce the highest glitch impulse. The AD7524 provides accuracy to 1/2 LSB without the need for thin-film resistors or laser trimming, while dissipating less than 5 mW typically.

Featuring operation from a 5-V to 15-V single supply, the AD7524 interfaces easily to most microprocessor buses or output ports. Excellent multiplying (2 or 4 quadrant) makes the AD7524 an ideal choice for many microprocessor-controlled gain-setting and signal-control applications.

The AD7524A is characterized for operation from 25°C to 85°C, and the AD7524J is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

SYMBOLIZATION		OPERATING TEMPERATURE RANGE
DEVICE	PACKAGE SUFFEXES	
AD7524A	N	– 25°C to 85°C
AD7524J	N, FN	0°C to 70°C

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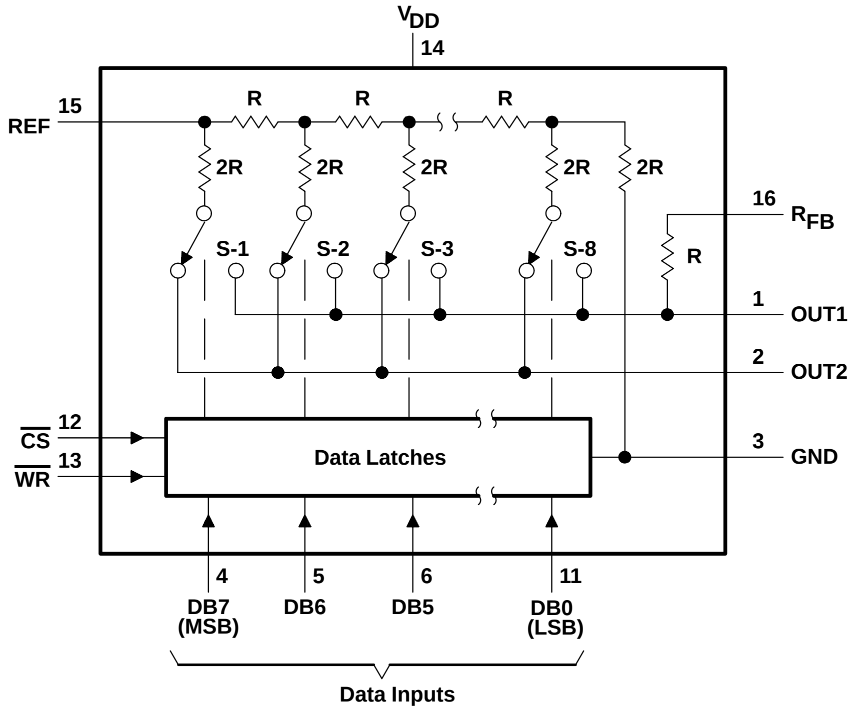
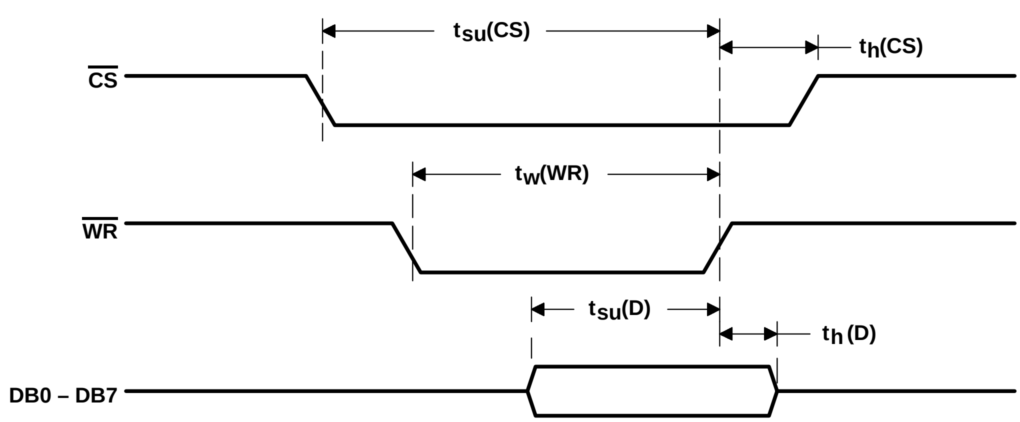
functional block diagram



Pin numbers shown are for the N package.

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{DD}	–0.3 V to 17 V
Voltage between R_{FB} and GND	±25 V
Digital input voltage, V_I	–0.3 V to V_{DD}+0.3 V
Reference voltage, V_{ref}	± 25 V
Peak digital input current, I_I	10 µA
Operating free-air temperature range : AD7524A	–25°C to 85°C
AD7524J	0°C to 70°C
Storage temperature range	–65°C to 150°C
Case temperature for 60 seconds: FN package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: N package	260°C

recommended operating conditions

		V_{DD} = 5 V MIN	V_{DD} = 5 V NOM	V_{DD} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V NOM	V_{DD} = 15 V MAX	UNIT
Supply voltage, V_{DD}		4.75	5	5.25	14.5	15	15.5	V
Reference voltage, V_{ref}			±10			±10		V
High-level input voltage, V_{IH}		2.4			13.5			V
Low-level input volage, V_{IL}				0.8			1.5	V
$\overline{CS}$ setup time, $t_{su(CS)}$		40			40			ns
$\overline{CS}$ hold time, $t_{h(CS)}$		0			0			ns
Data bus input setup time, $t_{su(D)}$		25			25			ns
Data bus input hold time, $t_{h(D)}$		10			10			ns
Pulse duration, $\overline{WR}$ low, $t_{w(WR)}$		40			40			ns
Operating free-air temperature, T_A	AD7524A	–25		85	–25		85	°C
	AD7524J	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V TYP	V_{DD} = 15 V MAX	UNIT
I_{IH}	High-level input current		$V_I = V_{DD}$	Full-range			10			10	µA
				25°C			1			1	
I_{IL}	Low-level input current		$V_I = 0$	Full-range			–10			–10	µA
				25°C			–1			–1	
I_{lkg}	Output leakage current	OUT1	DB0 – DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full-range			±400			±200	nA
				25°C			±50			±50	
		OUT2	DB0–DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V, V_{ref} = ±10 V	Full-range			±400			±200	
				25°C			±50			±50	
I_{DD}	Supply current	Quiescent	DB0 – DB7 at V_{IH}min or V_{IL}max	Full-range			2			2	mA
				25°C			1			2	
		Standby	DB0 – DB7 at 0 V or V_{DD}	Full-range			500			500	µA
				25°C			100			100	
k_{SVS}	Supply voltage sensitivity, Δgain/ΔV_{DD}		ΔV_{DD} = 10%	Full-range		0.01	0.16		0.005	0.04	%/%
				25°C		0.002	0.02		0.001	0.02	pF
C_i	Input capacitance, DB0 – DB7, $\overline{WR}$, $\overline{CS}$		$V_I = 0$				5			5	pF
C_o	Output capacitance	OUT1	DB0 – DB7 at 0, $\overline{WR}$ and $\overline{CS}$ at 0 V				30			30	pF
		OUT2					120			120	
		OUT1	DB0 – DB7 at V_{DD}, $\overline{WR}$ and $\overline{CS}$ at 0 V				120			120	
		OUT2					30			30	
	Reference input impedance (REF to GND)				5		20	5		20	kΩ

† Full range is 0°C to 70°C for the AD7524J and –25°C to 85°C for the AD7524A.

operating characteristics over recommended operating free-air temperature range, V_{ref} = 10 V, OUT1 and OUT2 at GND (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		V_{CC} = 5 V MIN	V_{CC} = 5 V MAX	V_{DD} = 15 V MIN	V_{DD} = 15 V MAX	UNIT
Linearity error				±0.2		±0.2	%FSR
Gain error	See Note 2	Full range		±1.4		±0.6	%FSR
		25°C		±1		±0.5	
Settling time (to 1/2 LSB)	See Note 2			100		100	ns
Propagation delay from digital input to 90% of final analog output current	See Note 2			80		80	ns
Feedthrough at OUT1 or OUT2	V_{ref} = ±10 V (100 kHz sinewave), $\overline{WR}$ and $\overline{CS}$ at 0, DB0 – DB7 at 0	Full range		0.5		0.5	%FSR
		25°C		0.25		0.25	
Temperature coefficient of gain	T_A = 25°C to t_{min} or t_{max}			±0.004		±0.001	%FSR/°C

† Full range is 0°C to 70°C for the AD7524J and –25°C to 85°C for the AD7524A.

NOTES: 1. Gain error is measured using the internal feedback resistor. Nominal Full Scale Range (FSR) = V_{ref} – 1 LSB.
2. OUT1 load = 100 Ω, C_{ext} = 13 pF, $\overline{WR}$ at 0 V, $\overline{CS}$ at 0 V, DB0 – DB7 at 0 V to V_{DD} or V_{DD} to 0 V.

PRINCIPLES OF OPERATION

The AD7524 is an 8-bit multiplying D/A converter consisting of an inverted R-2R ladder, analog switches, and data input latches. Binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each ladder leg independent of the switch state. The high-order bits are decoded and these decoded bits, through a modification in the R-2R ladder, control three equally weighted current sources. Most applications only require the addition of an external operational amplifier and a voltage reference.

The equivalent circuit for all digital inputs low is seen in Figure 1. With all digital inputs low, the entire reference current, I_{ref}, is switched to OUT2. The current source 1/256 represents the constant current flowing through the termination resistor of the R-2R ladder, while the current source I_{lkg} represents leakage currents to the substrate. The capacitances appearing at OUT1 and OUT2 are dependent upon the digital input code. With all digital inputs high, the off-state switch capacitance (30 pF maximum) appears at OUT2 and the on-state switch capacitance (120 pF maximum) appears at OUT1. With all digital inputs low, the situation is reversed as shown in Figure 1. Analysis of the circuit for all digital inputs high is similar to Figure 1; however, in this case, I_{ref} would be switched to OUT1.

Interfacing the AD7524 D/A converter to a microprocessor is accomplished via the data bus and the $\overline{CS}$ and $\overline{WR}$ control signals. When $\overline{CS}$ and $\overline{WR}$ are both low, the AD7524 analog output responds to the data activity on the DB0 – DB7 data bus inputs. In this mode, the input latches are transparent and input data directly affects the analog output. When either the $\overline{CS}$ signal or $\overline{WR}$ signal goes high, the data on the DB0 – DB7 inputs are latched until the $\overline{CS}$ and $\overline{WR}$ signals go low again. When $\overline{CS}$ is high, the data inputs are disabled regardless of the state of the $\overline{WR}$ signal.

The AD7524 is capable of performing 2-quadrant or full 4-quadrant multiplication. Circuit configurations for 2-quadrant or 4-quadrant multiplication are shown in Figures 2 and 3. Input coding for unipolar and bipolar operation are summarized in Tables 1 and 2, respectively.

PRINCIPLES OF OPERATION

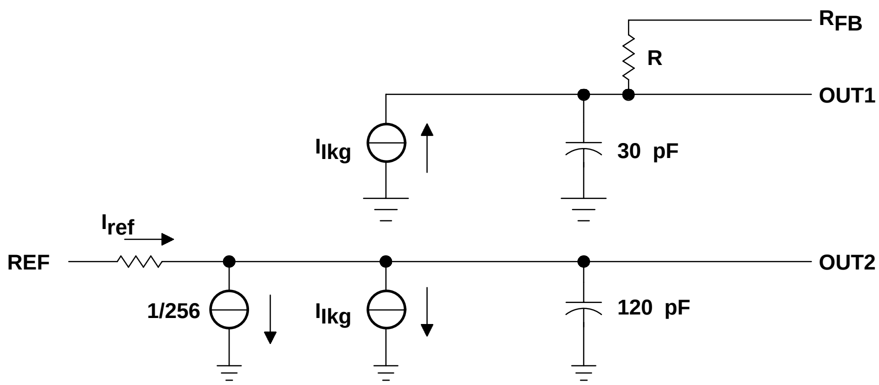


Figure 1. AD7524 Equivalent Circuit With All Digital Inputs Low

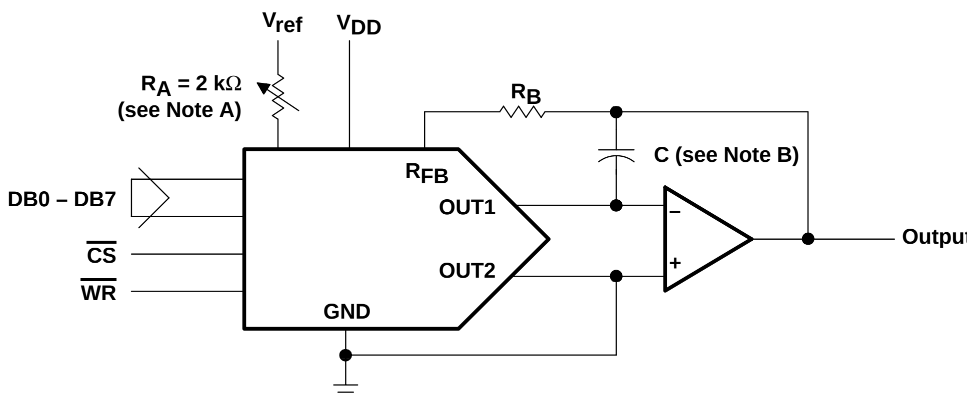


Figure 2. Unipolar Operation (2-Quadrant Multiplication)

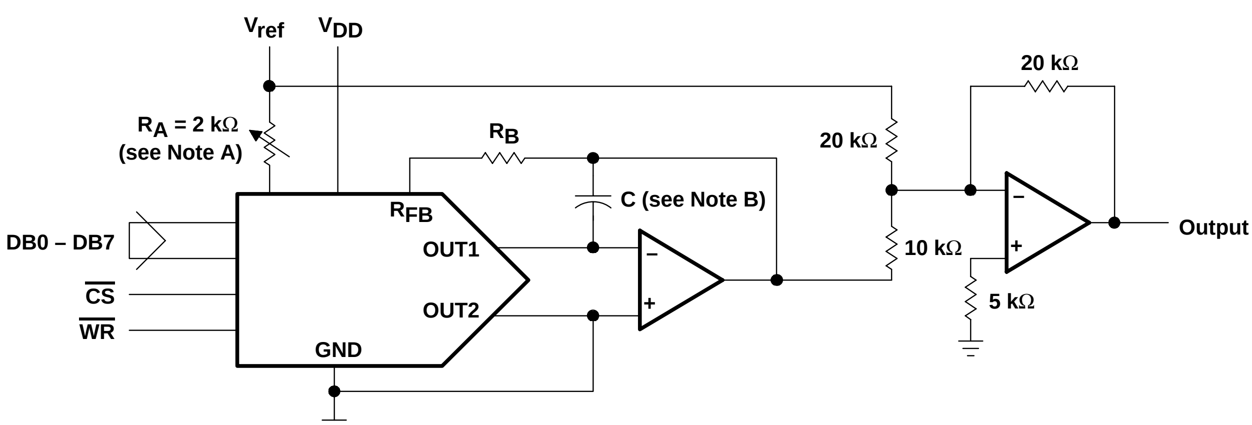


Figure 3. Bipolar Operation (4-Quadrant Operation)

NOTES: A. R_A and R_B used only if gain adjustment is required.
B. C phase compensation (10 – 15 pF) is required when using high-speed amplifiers to prevent ringing or oscillation.

PRINCIPLES OF OPERATION

Table 1. Unipolar Binary Code

DIGITAL INPUT (SEE NOTE 3) MSB LSB	ANALOG OUTPUT
11111111	$-V_{ref}$ (255/256)
10000001	$-V_{ref}$ (129/256)
10000000	$-V_{ref}$ (128/256) = $-V_{ref}$ /2
01111111	$-V_{ref}$ (127/256)
00000001	$-V_{ref}$ (1/256)
00000000	0

Table 2. Bipolar (Offset Binary) Code

DIGITAL INPUT (SEE NOTE 4) MSB LSB	ANALOG OUTPUT
11111111	V_{ref} (127/128)
10000001	V_{ref} (1/128)
10000000	0
01111111	$-V_{ref}$ (1/128)
00000001	$-V_{ref}$ (127/128)
00000000	$-V_{ref}$

NOTES: 3. LSB = 1/256 (V_{ref}).
4. LSB = 1/128 (V_{ref}).

microprocessor interfaces

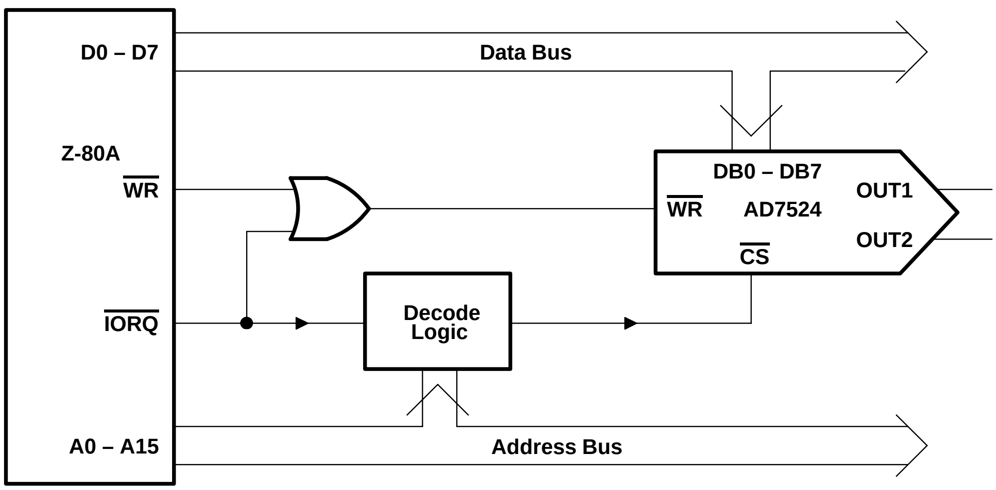


Figure 4. AD7524 – Z-80A Interface

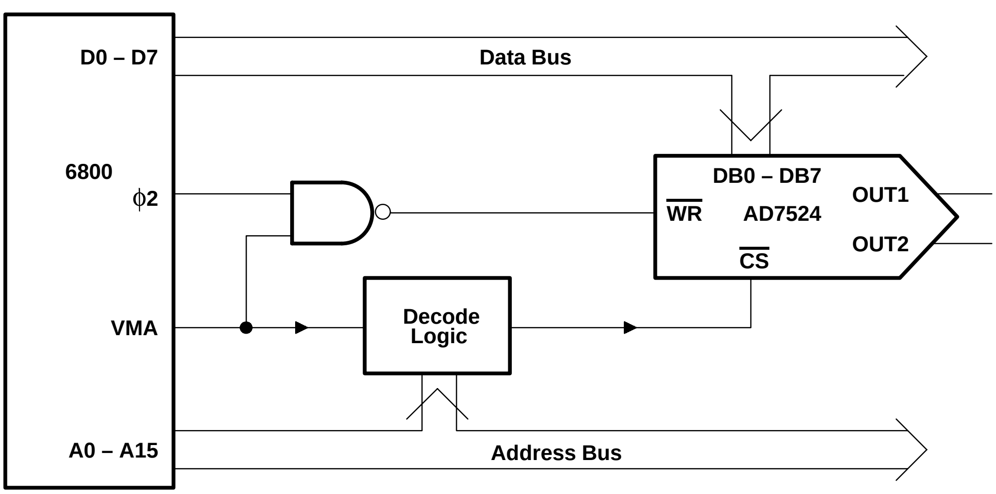


Figure 5. AD7524 – 6800 Interface

microprocessor interfaces (continued)

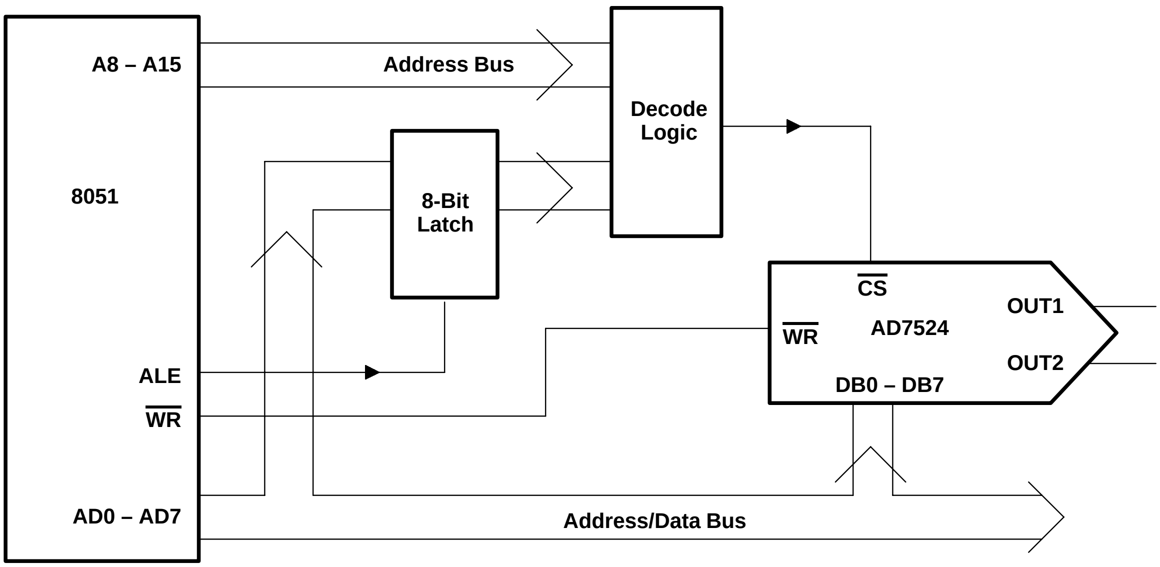


Figure 6. AD7524 -8051 Interface

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