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Low Voltage Differential Signaling (LVDS) Evaluation Module Board (EVM)

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Low Voltage Differential Signaling (LVDS) Evaluation Module Board (EVM)

ABSTRACT

This board will help you evaluate Texas Instruments Low-voltage Differential Signaling (LVDS) products. It can be set-up in a point-to-point transmit-receive interconnection, a multidrop interconnection, and even receive 422 data into an LVDS receiver.

1 Evaluation Module Board

The main components of the EVM are the LVDS transmitter and receiver pair (U1 and U2). The board is divided into a transmitter section (top) and a receiver section (bottom). The transmitter (SN65LVDS31) and the receiver (SN65LVDS32) are both 4-channel devices with the same enabling scheme.

Jumpers, J5 and J6, have been installed so that the supply rails can be isolated and each part can be evaluated independently. If Jumpers J5 and J6 are left in place, then both parts will share the same V_{CC} and ground rails. Note that not all channels on the board have connectors; the first channel on the driver (1A) and the first channel on the receiver (1Y) are without connectors to facilitate other configurations.

Although this EVM is only equipped with the products SN65LVDS31 and SN65LVDS32, the results represent transmitting characteristics also found in SN65LVDS9637, SN65LVDS9638, SN65LVDS3486, and SN65LVDS3487.

2 Required Equipment

1. Power Supply
2. Wire or cable to connect transmitting and receiving channels
3. Function generator to supply TTL signal. These products will operate upwards of 400 MBps.
4. High bandwidth oscilloscope, preferably in the range of 4 GHz to see data from the receiver output.

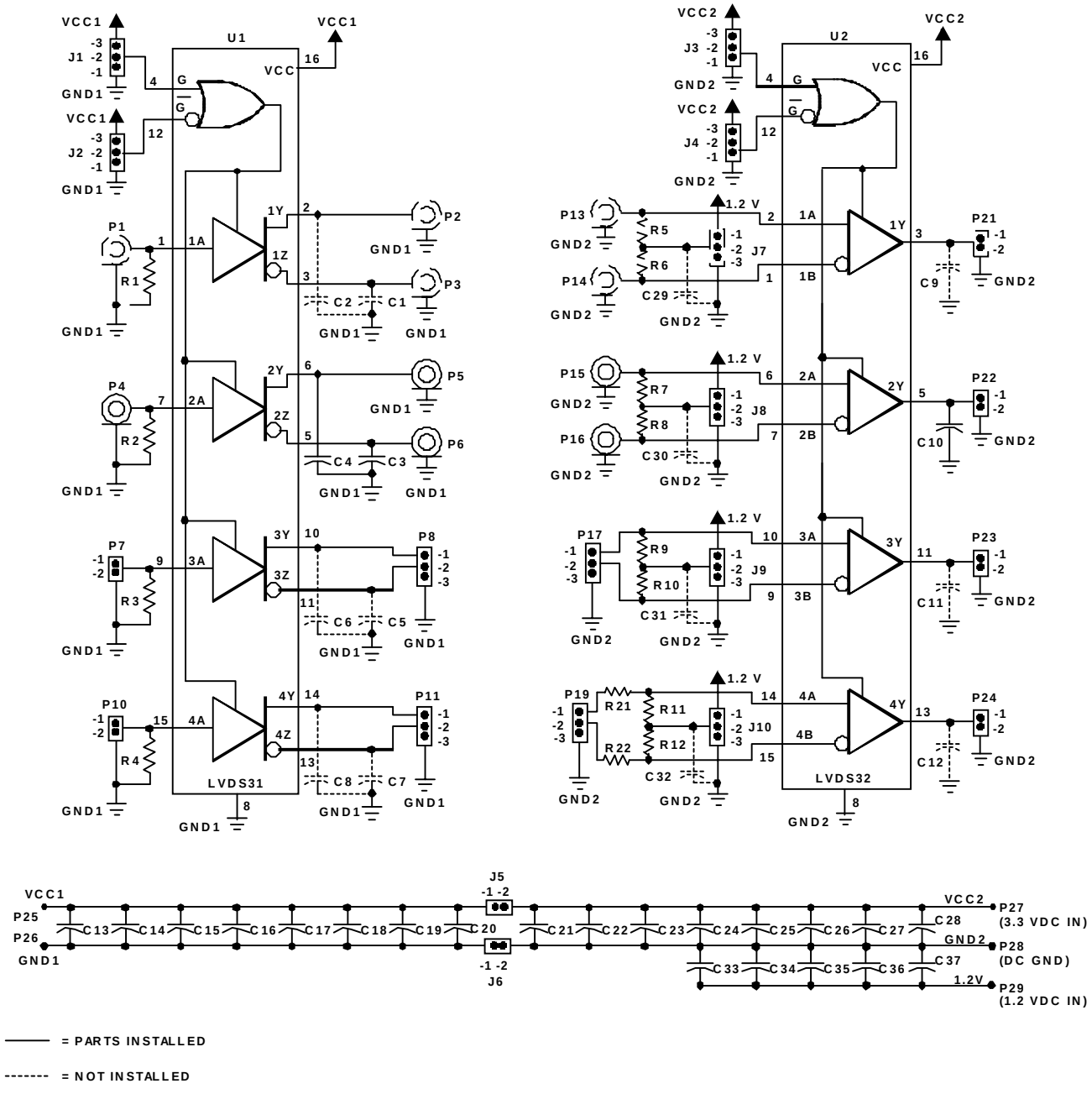

Figure 1. EVM Diagram

Table 1. Parts List

PART #	DESCRIPTION
C1 - C2	5 pF Capacitor (Opt: Not installed)
C3 - C4	5 pF Capacitor
C5 - C8	5 pF Capacitor (Opt: Not installed)
C9, C11, C12	18 pF Capacitor (Opt: Not installed)
C10	18 pF Capacitor
C13, C28, C37	10 µf Capacitor, Tantalum
C14 - C27	0.01 µf Capacitor
C29 - C32	0.01 µf Capacitor (Opt: Not installed)
C33 - C36	0.01 µf Capacitor
J1 - J4	3-Position Jumper Post (with shorting jumpers installed to enabled devices)
J5 - J6	2-Position Jumper Post
J7	3-Position Jumper Post (Not installed)
J8 - J10	3-Position Jumper Post
P1 - P3, P13, P14	Conn, SMA Edge-Mount (Not installed)
P4 - P6, P15, P16	Conn, SMA Edge-Mount
P7, P10	2-Position Jumper Post
P8, P11	3-Position Jumper Post
P9, P12, P18, P20	Not used
P17, P19	3-Position Jumper Post
P21	2-Position Jumper Post (Not installed)
P22 - P24	2-Position Jumper Post
P25 - P29	Banana Jack Connectors
R1	Resistor, 51 Ω (Not installed)
R2 - R4	Resistor, 51 Ω
R5 - R6	Resistor, 51 Ω
R7 - R10	Resistor, 51 Ω
R11 - R12	Resistor, 51 Ω
R13 - R16	Resistor, 51 Ω (Optional: Not installed)
R17 - R20	Not used
R21 - R22	Resistor, 45.3 Ω
U1	SN65LVDS31
U2	SN65LVDS32

3 Point-to-Point Configuration

Point-to-point (one driver to one receiver) is the preferred solution for transmitting LVDS signals. Signal quality is superior in this uncomplicated configuration since no stubs or discontinuity in impedance are present. While evaluating this configuration you may want to slow down your edges. This can be achieved by varying your capacitance across the output of the driver (i.e. C3 and C4).

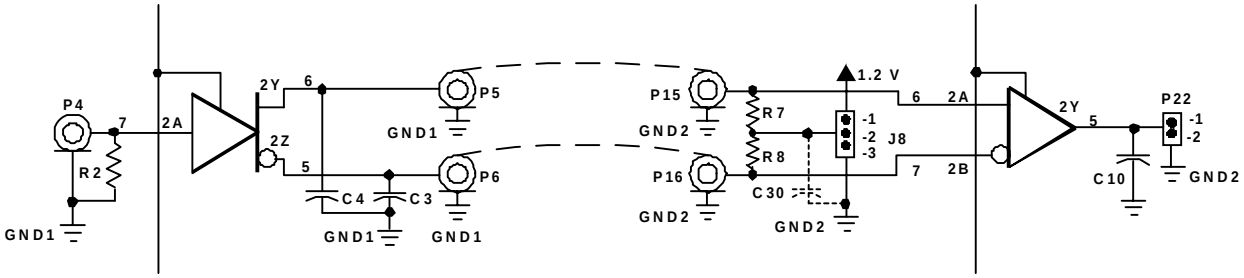

Figure 2. Point-to-Point Schematic Diagram

4 Multidrop Configuration

The board can be set up for multidrop configuration (one driver to two or three receivers). Connect the devices for either a two or three receive channel as shown in Figure 4. If you are using a two-channel multidrop, channels 1Y and 2Y have been set up this configuration. Only a terminating resistor must be placed at end of the transmission line. Multiple terminating receivers would attenuate the signal, since they would present a low impedance load to the driver. For three receivers the board must be modified. Unsolder the connectors from P5 and P6 and solder at P13 and P14. Remove R7 and R8 resistors to maintain signal termination at the end of the transmission line.

In multidrop configuration up to 17 receivers with no common-mode termination and up to 36 receivers with common-mode termination may be tied to the bus. The stubs between the line and each receiver must be kept to a minimum (<12 mm) because at high signaling rates, they may act as transmission lines creating reflections, and they may also cause an impedance discontinuity.

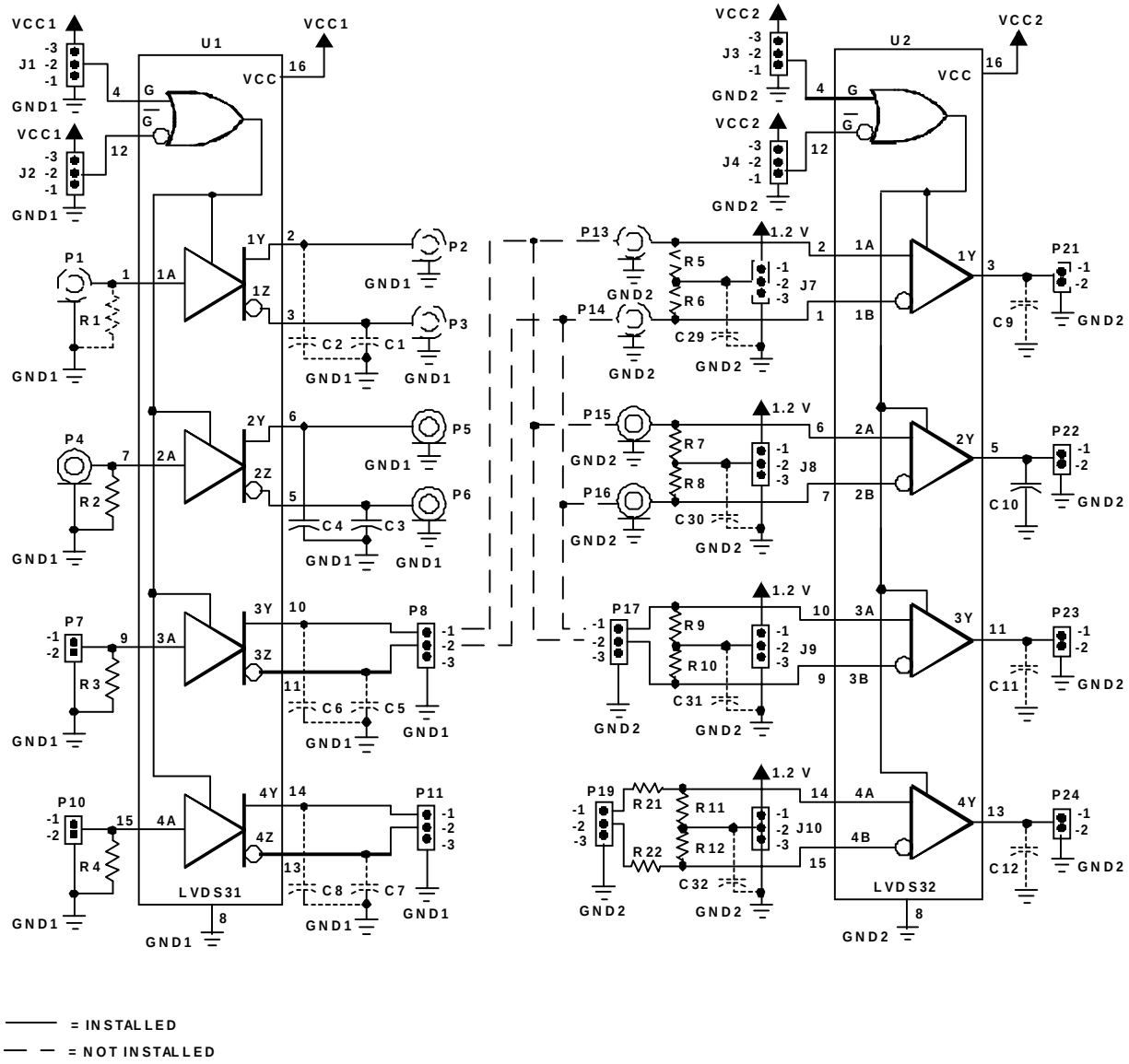

Figure 3. Multidrop Schematic Diagram

5 422 Data Into an LVDS Receiver Configuration

The fourth channel on the receiver, coupled with resistors R21 and R22, helps evaluate 422 data into an LVDS receiver. Set the generator to provide the signaling of 422 data. Resistors R21 and R22 attenuate the 422 levels to that which is required by the LVDS receiver. A simple resistor-divider solves this challenge. The resistors R21 and R22 at both the 4A and 4B inputs are 45.3 Ω, and R11 and R12 are 5.11 Ω.

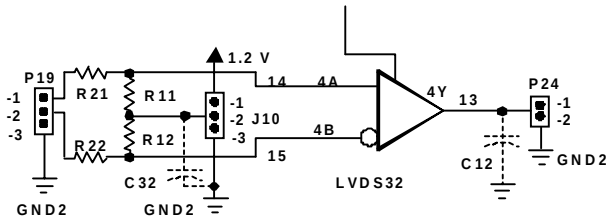

Figure 4. 422 Data into LVDS Receiver Schematic Diagram

References

Following is a list of the LVDS Literature available at printing time. Please visit TI's web site at http://www.ti.com/docs/msp/datatran/default.htm for the most update information.

1. *LVDS Designer's Notes, Lit #SLLA014*
2. *Reducing EMI with Low Voltage Differential Signaling, Lit #SLLA030*
3. *IBIS Models*
4. *1998 Data Transmission Data Book, Lit #SLLD001B*