NOTES, UNLESS OTHERWISE SPECIFIED:

1. VCC IS APPLIED TO PIN 8 OF ALL 8-PIN IC'S,
   PIN 14 OF ALL 14-PIN IC'S, PIN 16 OF ALL
   16-PIN IC'S, PIN 20 OF ALL 20-PIN IC'S, ETC.

2. GROUND IS APPLIED TO PIN 4 OF ALL 8-PIN IC'S,
   PIN 7 OF ALL 14-PIN IC'S, PIN 8 OF ALL
   16-PIN IC'S, PIN 10 OF ALL 20-PIN IC'S, ETC.

3. RESISTANCE VALUES ARE IN OHMS.

4. CAPACITANCE VALUES ARE IN MICROFARADS.

5. HIGHEST REFERENCE DESIGNATOR USED:

A. CAPACITORS	C65
B. RESISTORS	R79
C. IC'S	U26
D. DUAL LED'S	DLED4
E. HEADERS	J8
F. JUMPERS	JP4
G. SELECTORS	SL14
H. INDUCTORS	L4
I. POWER JACKS	PWR1
J. PUSHBUTTONS	PB2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
*			

Board Features:

> Each DSP has 256K 1ws SRAM with 512K addressable via Bank Logic GAL.

Memory Banks:

Bank 0	0h	-	0FFFFh	(Note 1)
Bank 1	10000h	-	1FFFFh	
Bank 2	20000h	-	2FFFFh	
Bank 3	30000h	-	3FFFFh	
Bank 4	40000h	-	4FFFFh	(Note 1)
Bank 5	50000h	-	5FFFFh	(Memory chip select available)
Bank 6	60000h	-	6FFFFh	(Memory chip select available)
Bank 7	70000h	-	7FFFFh	(Memory chip select available)
Bank 8	80000h	-	8FFFFh	(Memory chip select available)

Note 1: Memory Map can be configured to include
Bank 0 -OR- Bank 4, but not both.

> Each DSP has 1- 64K memory bank configurable for local memory (0h-ffffh) or extended (40000h-4ffffh).

> CPU_A and CPU_B HPI's are connected together, deselected via HPIENA jumper, disconnected via GPIO.

> DSP's I/O space maps the other DSP's HPI and/or general purpose I/O via the CONFIG GAL.

> Additional I/O latches (6) are available for each DSP via their respective CONFIG GAL's.

> CPU_A and CPU_B TDM port's can be configured in TDM mode or standard mode via the jumpers.

> Each DSP has a dedicated perf-board area for prototyping.

> Master clocks are from the socketed clock oscillator or resonator circuit.

> All signals are connected to headers to allow expandability and daughter card connections.

> Dirty and clean VCC's of each DSP are jumpered for easy power measurements.

> Each DSP has a dedicated RESET pushbutton.

> Each DSP's HPI boot mode is hardware configurable.

> JTAG chain is hardware configurable to allow additional JTAG compliant devices on duaghter boards.

> Rev B board daughter board connectors are NOT compatible with the 'C6x header spec.

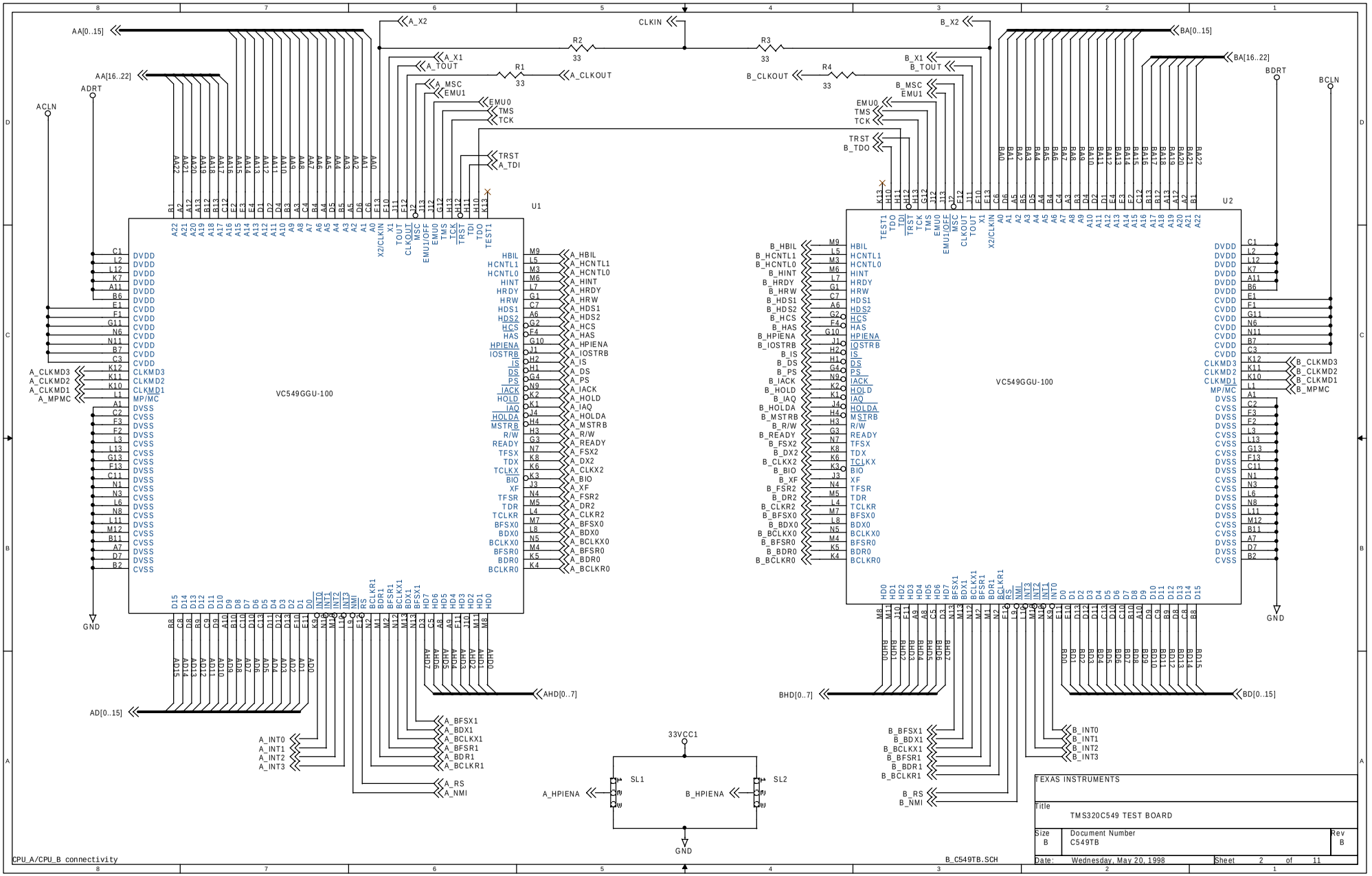
REVISION STATUS OF SHEETS										
REV										ENGR G. CAPWELL
SH REV										
SH REV	*	*	*	*	*	*	*	NEXT ASSY	USED ON	
SH	1	2	3	4	5	6	7	APPLICATION		

TEXAS INSTRUMENTS
Fixed-Point DSP Applications
SEMICONDUCTOR GROUP
HOUSTON, TEXAS

Title: TMS320C549 Test Board

Size	Document Number	Rev
B	C549TB	B

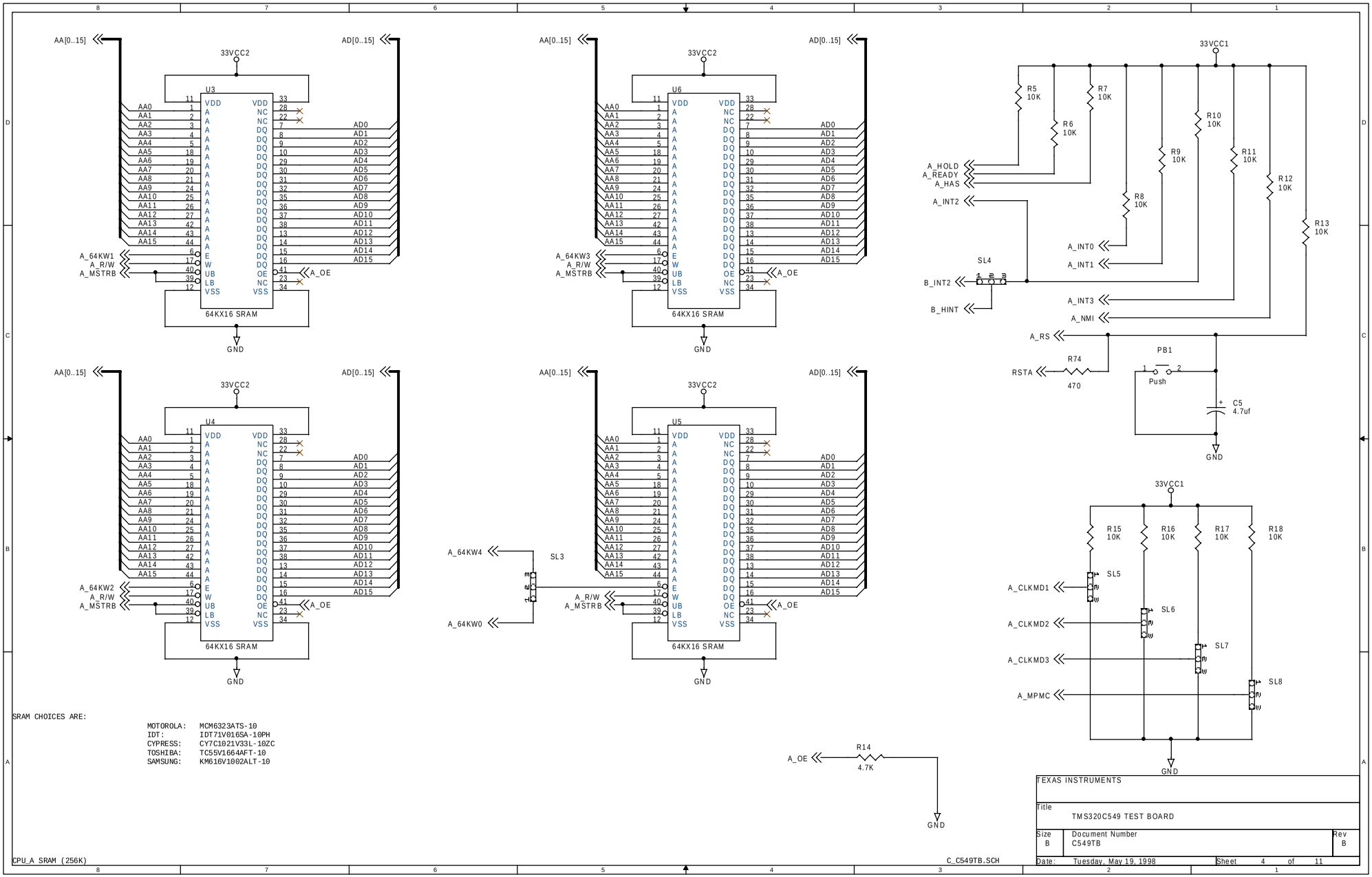
A_C549TB.SCH | Date: Tuesday, June 30, 1998 | Sheet 1 of 11


AA[0..15]
AA[16..22]
ADRT
ACLN
A_X2
A_X1
A_TOUT
A_MSC
EMU1
EMU0
TMS
TCK
TRST
A_TDI
A_CLKOUT
R1
R2
R3
R4
33
CLKIN
B_X2
B_X1
B_TOUT
B_MSC
EMU1
EMU0
TMS
TCK
TRST
B_TDO
B_CLKOUT
BA[0..15]
BA[16..22]
BDRT
BCLN
U1
VC549GGU-100
U2
VC549GGU-100
A_CLKMD3
A_CLKMD2
A_CLKMD1
A_MPMC
B_CLKMD3
B_CLKMD2
B_CLKMD1
B_MPMC
GND
AD[0..15]
AHD[0..7]
BHD[0..7]
BD[0..15]
A_INT0
A_INT1
A_INT2
A_INT3
A_BFSX1
A_BDX1
A_BCLKX1
A_BFSR1
A_BDR1
A_BCLKR1
A_RS
A_NMI
B_INT0
B_INT1
B_INT2
B_INT3
B_BFSX1
B_BDX1
B_BCLKX1
B_BFSR1
B_BDR1
B_BCLKR1
B_RS
B_NMI
33VCC1
SL1
SL2
A_HPIENA
B_HPIENA
TEXAS INSTRUMENTS
TMS320C549 TEST BOARD
Size B
Document Number C549TB
Rev B
Date: Wednesday, May 20, 1998
Sheet 2 of 11
CPU_A/CPU_B connectivity
B_C549TB.SCH

THIS IS THE ROOT SHEET OF THIS DESIGN.
IT CONTAINS THE |LINK PIPE COMMAND AND
THE LIST OF FILES NECESSARY TO PROCESS
A FLAT DESIGN.

```
|link
|B_C549TB.SCH
|C_C549TB.SCH
|D_C549TB.SCH
|E_C549TB.SCH
|F_C549TB.SCH
|G_C549TB.SCH
|H_C549TB.SCH
|I_C549TB.SCH
|J_C549TB.SCH
```

TEXAS INSTRUMENTS		
Title: TMS320C549 TEST BOARD		
Size: A	Document Number: C549TB	Rev: B
Date: Wednesday, May 20, 1998	Sheet 3 of 11	



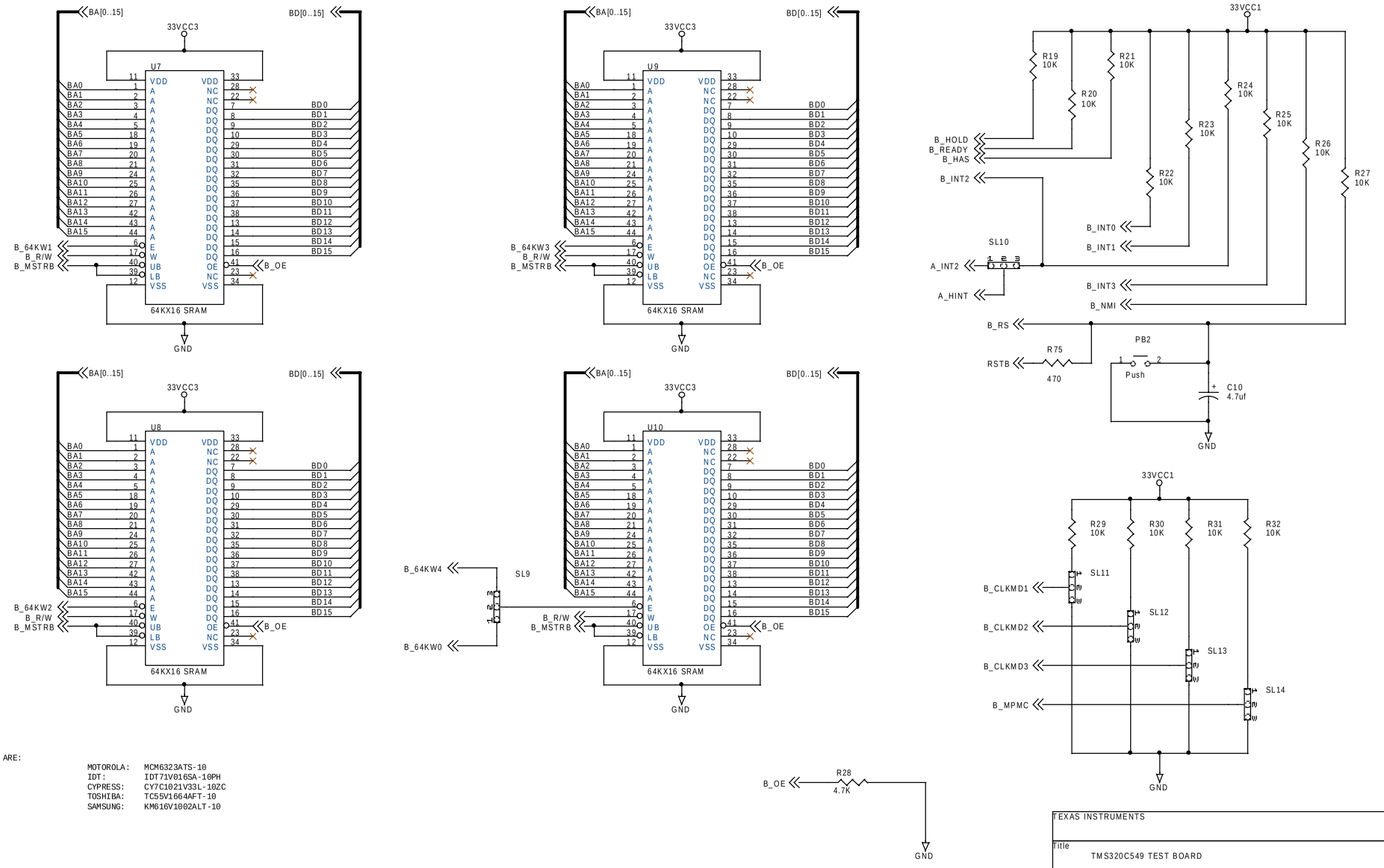
SRAM CHOICES ARE:

MOTOROLA:	MCM6323ATS-10
IDT:	IDT71V016SA-10PH
CYPRESS:	CY7C1021V33L-10ZC
TOSHIBA:	TC55V1664AFT-10
SAMSUNG:	KM616V1002ALT-10

TEXAS INSTRUMENTS		
Title: TMS320C549 TEST BOARD		
Size: B	Document Number: C549TB	Rev: B
Date: Tuesday, May 19, 1998	Sheet 4 of 11	

CPU_A SRAM (256K)

C_C549TB.SCH



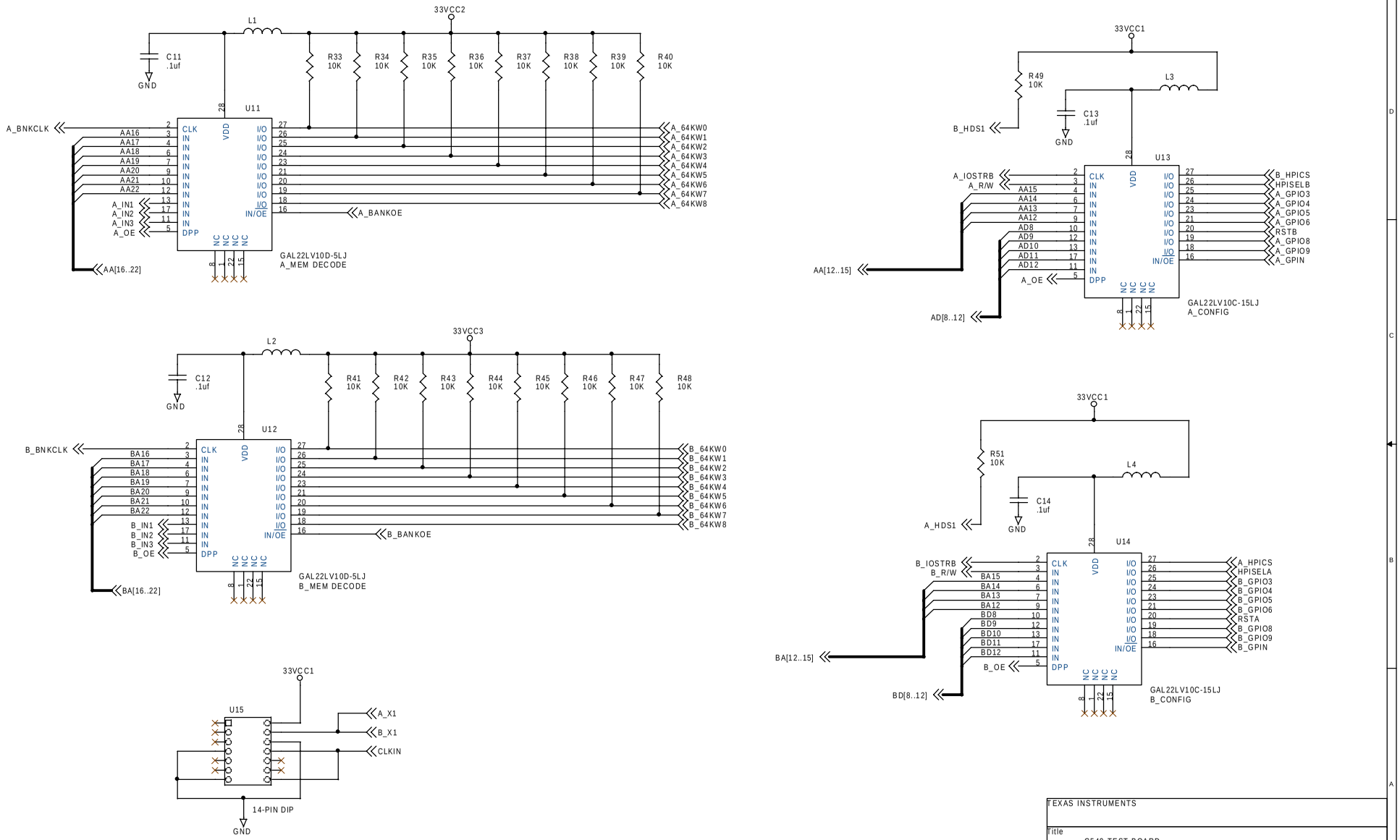
SRAM CHOICES ARE:

MOTOROLA:	MCM6323ATS-10
IDT:	IDT71V016SA-10PH
CYPRESS:	CY7C1021V33L-10ZC
TOSHIBA:	TC55V1664AFT-10
SAMSUNG:	KM616V1002ALT-10

TEXAS INSTRUMENTS		
Title: TMS320C549 TEST BOARD		
Size: B	Document Number: C549TB	Rev: B
Date: Tuesday, May 19, 1998	Sheet 5 of 11	

CPU_B SRAM (256K)

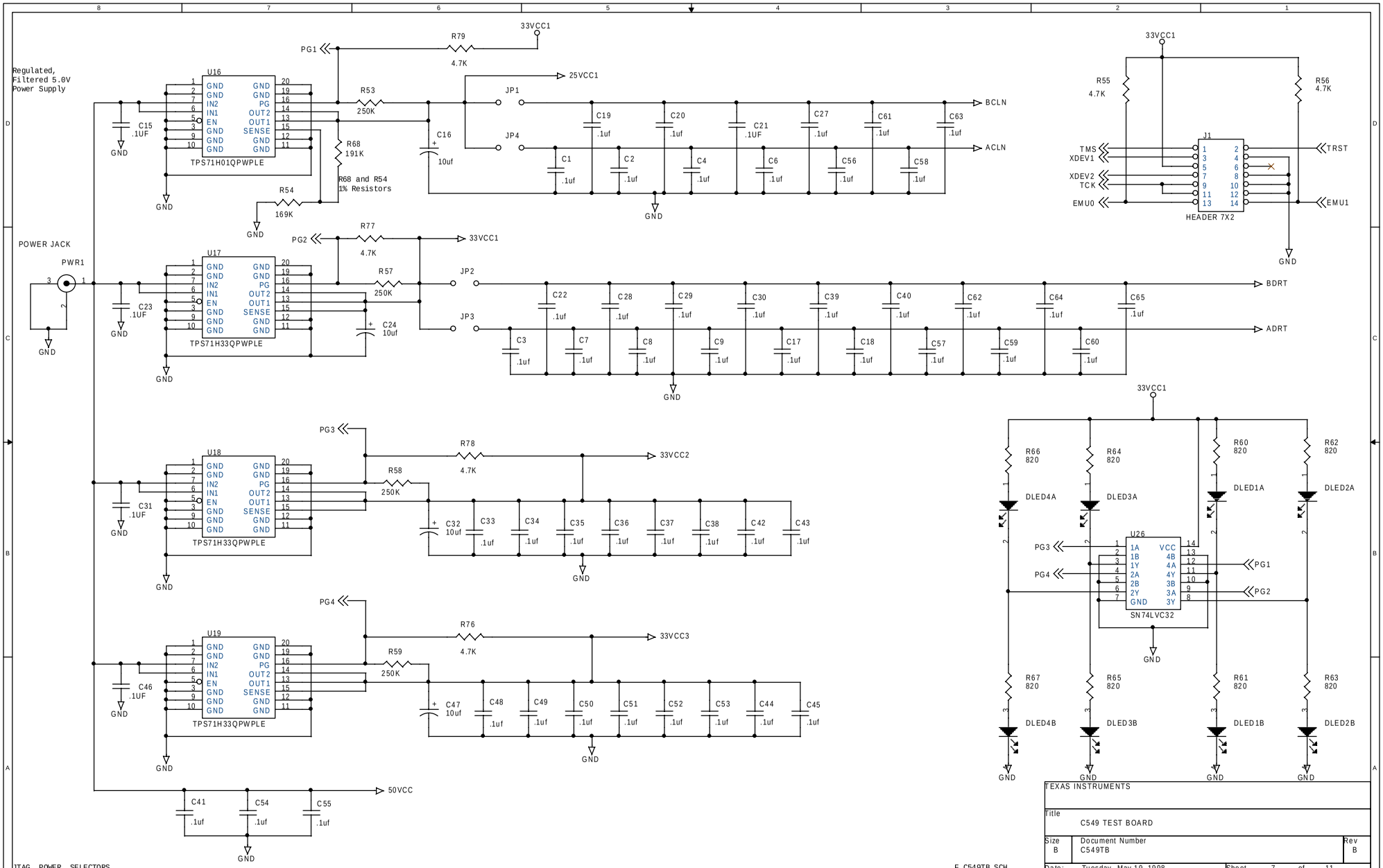
D_C549TB.SCH

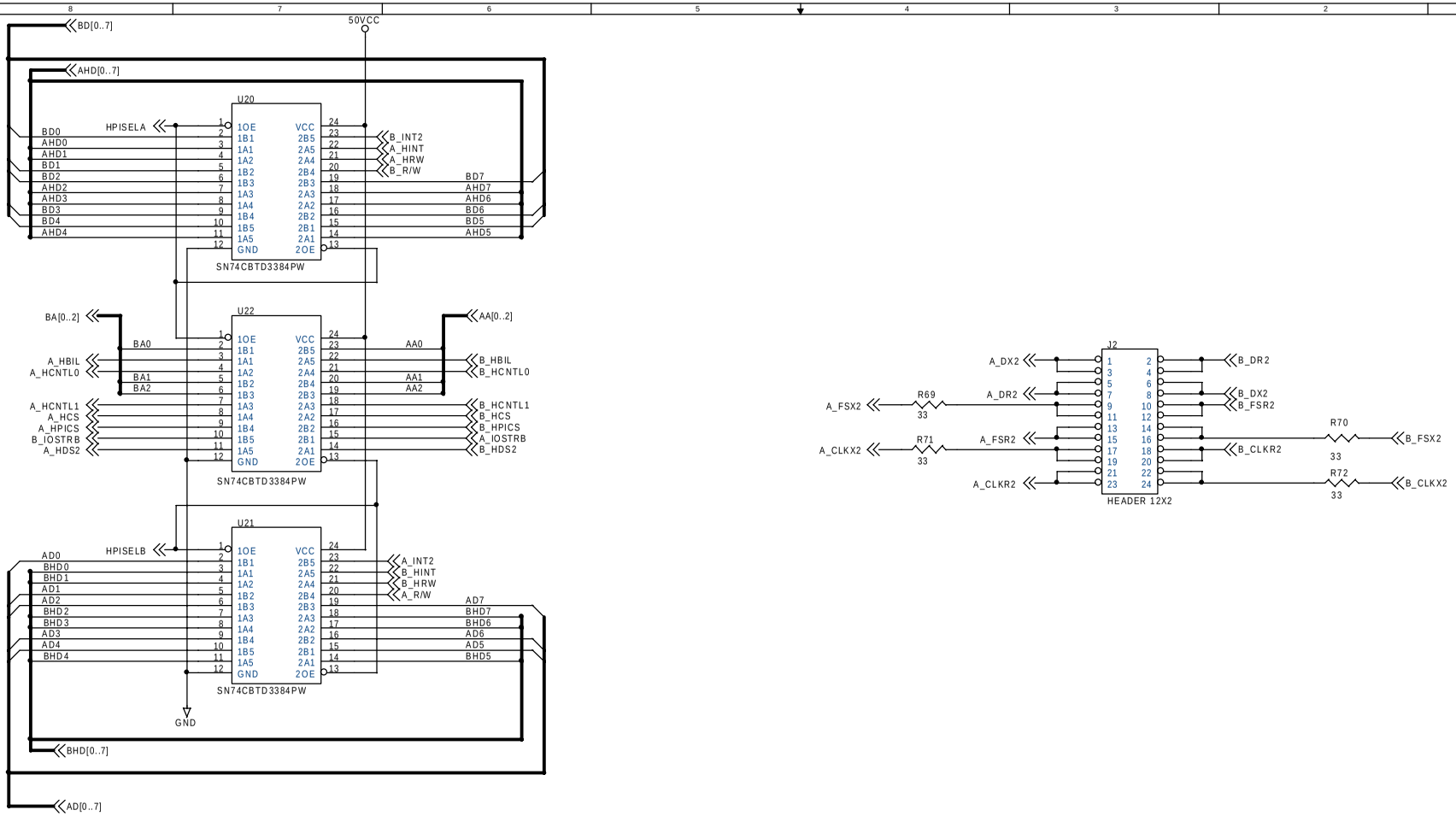


TEXAS INSTRUMENTS		
Title: C549 TEST BOARD		
Size: B	Document Number: C549TB	Rev: B
Date: Tuesday, May 19, 1998	Sheet 6 of 11	

Programmable Logic devices

E_C549TB.SCH

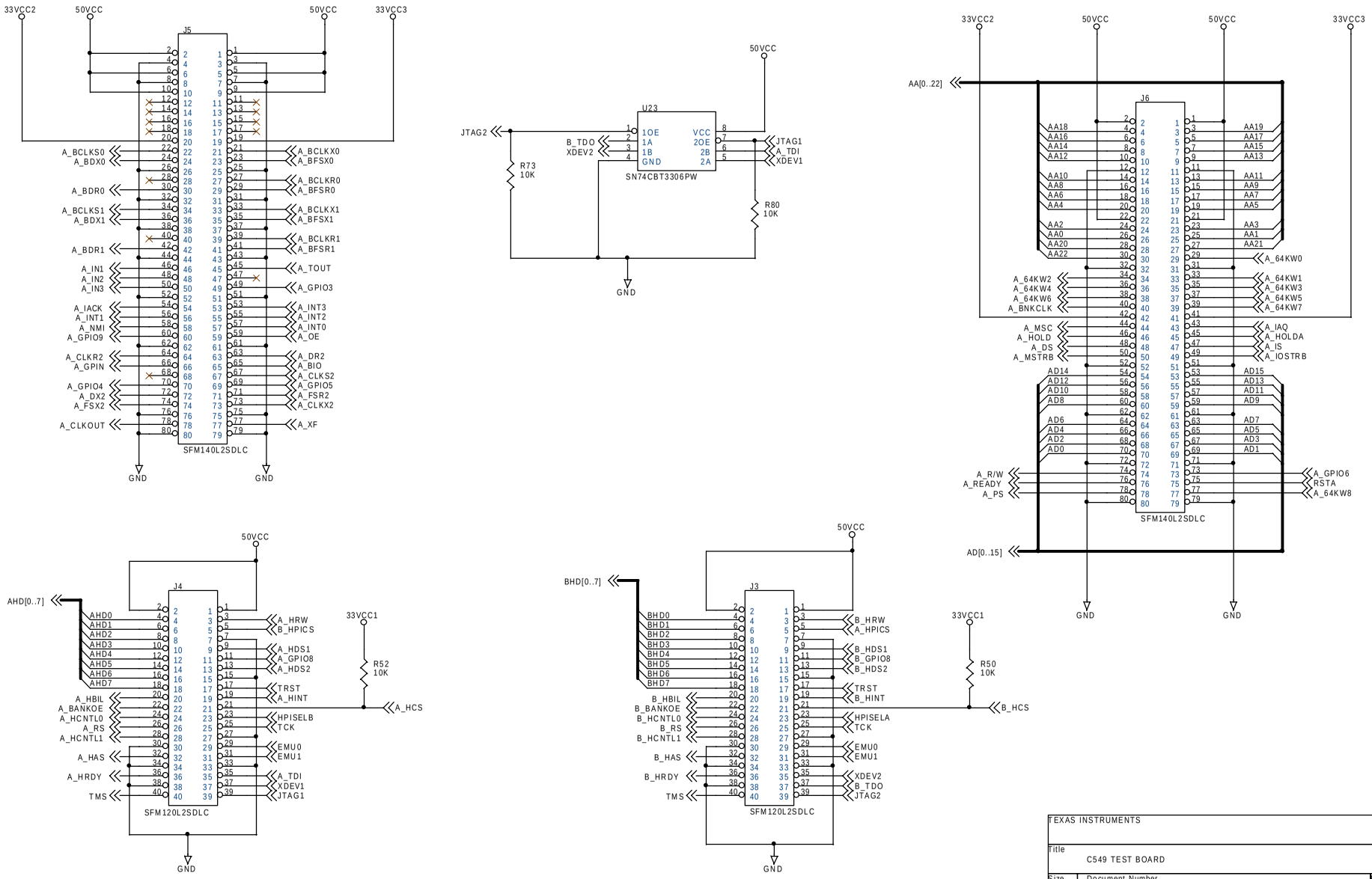

Regulated,
Filtered 5.0V
Power Supply
POWER JACK
PWR1
U16
U17
U18
U19
TPS71H01QPWPLE
TPS71H33QPWPLE
33VCC1
33VCC2
33VCC3
50VCC
25VCC1
PG1
PG2
PG3
PG4
R79
4.7K
R53
250K
R68
191K
R68 and R54
1% Resistors
R54
169K
R77
R57
R78
R58
R76
R59
JP1
JP4
JP2
JP3
BCLN
ACLN
BDRT
ADRT
C15 .1UF
C16 10uf
C23 .1UF
C24 10uf
C31 .1UF
C32 10uf
C46 .1UF
C47 10uf
C41
C54
C55
GND
J1
HEADER 7X2
TMS
XDEV1
XDEV2
TCK
EMU0
TRST
EMU1
R55
R56
U26
SN74LVC32
R66 820
R64 820
R60 820
R62 820
R67 820
R65 820
R61 820
R63 820
DLED4A
DLED3A
DLED1A
DLED2A
DLED4B
DLED3B
DLED1B
DLED2B
TEXAS INSTRUMENTS
C549 TEST BOARD
Document Number
C549TB
Size B
Rev B
Date: Tuesday, May 19, 1998
Sheet 7 of 11
JTAG, POWER, SELECTORS
F_C549TB.SCH

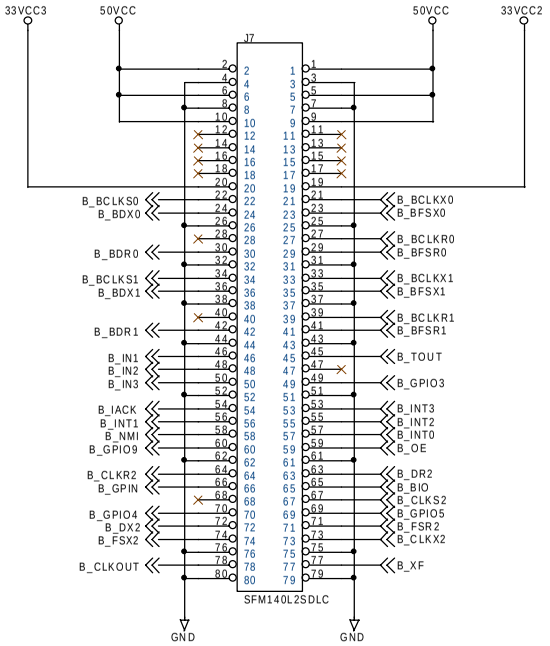


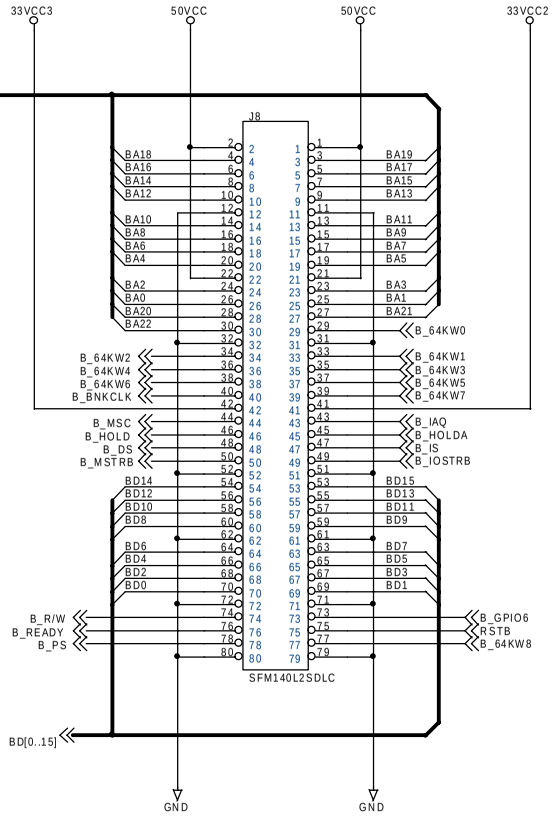
HPI and TDM connectivity

G_C549TB.SCH

TEXAS INSTRUMENTS		
Title: C549 TEST BOARD		
Size: B	Document Number: C549TB	Rev: B
Date: Wednesday, May 20, 1998	Sheet 8 of 11	


33VCC2
50VCC
50VCC
33VCC3
J5
A_BCLKS0
A_BDX0
A_BDR0
A_BCLKS1
A_BDX1
A_BDR1
A_IN1
A_IN2
A_IN3
A_IACK
A_INT1
A_NMI
A_GPIO9
A_CLKR2
A_GPIN
A_GPIO4
A_DX2
A_FSX2
A_CLKOUT
A_BCLKX0
A_BFSX0
A_BCLKR0
A_BFSR0
A_BCLKX1
A_BFSX1
A_BCLKR1
A_BFSR1
A_TOUT
A_GPIO3
A_INT3
A_INT2
A_INT0
A_OE
A_DR2
A_BIO
A_CLKS2
A_GPIO5
A_FSR2
A_CLKX2
A_XF
SFM140L2SDLC
GND
GND
50VCC
U23
JTAG2
B_TDO
XDEV2
1OE
1A
1B
GND
VCC
2OE
2B
2A
SN74CBT3306PW
JTAG1
A_TDI
XDEV1
R73
10K
R80
10K
GND
33VCC2
50VCC
50VCC
33VCC3
AA[0..22]
J6
AA18
AA16
AA14
AA12
AA10
AA8
AA6
AA4
AA2
AA0
AA20
AA22
AA19
AA17
AA15
AA13
AA11
AA9
AA7
AA5
AA3
AA1
AA21
A_64KW0
A_64KW2
A_64KW4
A_64KW6
A_BNKCLK
A_64KW1
A_64KW3
A_64KW5
A_64KW7
A_MSC
A_HOLD
A_DS
A_MSTRB
A_IAQ
A_HOLDA
A_IS
A_IOSTRB
AD14
AD12
AD10
AD8
AD6
AD4
AD2
AD0
AD15
AD13
AD11
AD9
AD7
AD5
AD3
AD1
A_R/W
A_READY
A_PS
A_GPIO6
RSTA
A_64KW8
SFM140L2SDLC
AD[0..15]
GND
GND
50VCC
AHD[0..7]
J4
AHD0
AHD1
AHD2
AHD3
AHD4
AHD5
AHD6
AHD7
A_HBIL
A_BANKOE
A_HCNTL0
A_RS
A_HCNTL1
A_HAS
A_HRDY
TMS
A_HRW
B_HPICS
A_HDS1
A_GPIO8
A_HDS2
TRST
A_HINT
HPISELB
TCK
EMU0
EMU1
A_TDI
XDEV1
JTAG1
SFM120L2SDLC
33VCC1
R52
10K
A_HCS
GND
50VCC
BHD[0..7]
J3
BHD0
BHD1
BHD2
BHD3
BHD4
BHD5
BHD6
BHD7
B_HBIL
B_BANKOE
B_HCNTL0
B_RS
B_HCNTL1
B_HAS
B_HRDY
TMS
B_HRW
A_HPICS
B_HDS1
B_GPIO8
B_HDS2
TRST
B_HINT
HPISELA
TCK
EMU0
EMU1
XDEV2
B_TDO
JTAG2
SFM120L2SDLC
33VCC1
R50
10K
B_HCS
GND
TEXAS INSTRUMENTS
Title
C549 TEST BOARD
Size
B
Document Number
C549TB
Rev
B
Date:
Wednesday, May 20, 1998
Sheet
9
of
11
Headers 1
H_C549TB.SCH

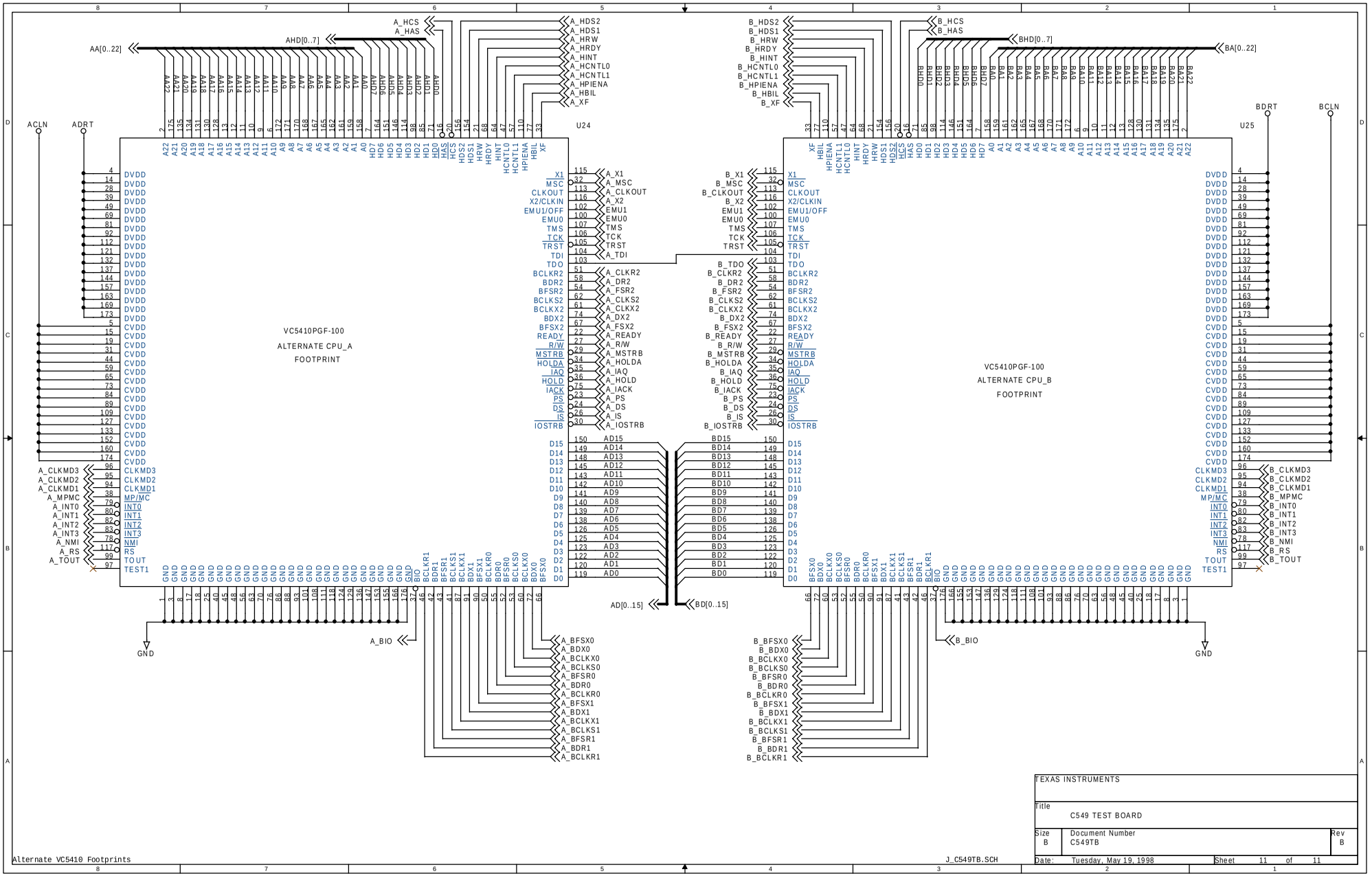




TEXAS INSTRUMENTS		
Title: C549 TEST BOARD		
Size: B	Document Number: C549TB	Rev: B
Date: Wednesday, May 20, 1998	Sheet 10 of 11	

Headers 2

I_C549TB.SCH


VC5410PGF-100
ALTERNATE CPU_A
FOOTPRINT
VC5410PGF-100
ALTERNATE CPU_B
FOOTPRINT
U24
U25
AA[0..22]
AHD[0..7]
BA[0..22]
BHD[0..7]
AD[0..15]
BD[0..15]
A_BIO
B_BIO
GND
ACLN
ADRT
BDRT
BCLN
TEXAS INSTRUMENTS
C549 TEST BOARD
Size B
Document Number C549TB
Rev B
Date: Tuesday, May 19, 1998
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Alternate VC5410 Footprints
J_C549TB.SCH