TMS320 DSP
Number 84A
DESIGNER'S NOTEBOOK

Detecting the reset source on the TMS320x240 DSP Controller

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Design Problem

The TMS320x240 ('x240) DSP Controller allows three internal and two external methods to generate device resets. How do I configure the 'x240 to detect which source initiated the reset?

Solution

The 'x240 DSP Controller provides the capability to detect the source of a reset through the use of the System Status Register (SYSSR@701Ah). This register contains a status bit for four of the five possible reset sources. The fifth source, the external $\overline{RS}$ pin, does not have a status bit, and is identifiable when the other four bits are cleared. These bits are summarized below:

Bit 15	PORST	external Power-on Reset ($\overline{PORESET}$) pin
Bit 12	ILLADR	Illegal Address Access
Bit 10	SWRST	Software Reset
Bit 9	WDRST	Watchdog Timer
None of these set -		External Reset ($\overline{RS}$) pin

The reset service routine should be written to check the status of each bit and take the appropriate action. When the status bit equals 1, the indicated event triggered the reset. In the case when none of the reset status bits are set, the external $\overline{RS}$ pin triggered the reset.

On detection of power-on-reset, the programmer should initialize the PLL, if necessary, configure the CLKOUT pin for the desired function, and clear the PORST status bit. In addition, the programmer may wish to implement a wait loop while the PLL locks. Once the PLL locks, the internal clock will run at the programmed frequency. This ensures that software-timed events will work as expected.

An assembly language code example is included below for reference.

Example 1. Code Listing

```
; .set definitions for useful constants

DP_PF1    .set   224       ;page 1 of periph. file (7000h/80h)
SYSCR     .set   07018h    ;System Module Control Register
SYSSR     .set   0701Ah    ;System Module Status Register
RTICR     .set   07027h    ;RTI Control register
WDTCR     .set   07029h    ;WD Control register
CKCR0     .set   0702ah    ;PLL Clock Control Register 0
CKCR1     .set 0702ch      ;PLL Clock Control Register 1
;Bit codes for Test bit instruction (BIT)
BIT15     .set   0000h     ;Bit Code for 15
BIT12     .set   0003h     ;Bit Code for 12
BIT10     .set   0005h     ;Bit Code for 10
BIT9      .set   0006h     ;Bit Code for 9
BIT5      .set   000Ah     ;Bit Code for 5
   .text
RESET: B  START
       B  INT1_ISR      ;User's interrupt vector table inserted
                        ;here
    :
   (etc …)
;=================================================================
; This first segment of code is executed after every reset.
; The CPU modes, such as sign extension, overflow, XF output
; state, and global interrupt mask are initialized for clarity
; In addition, the data page pointer is set to access the first
; page in the peripheral register file, address 0x7000. Finally,
; the watchdog timer is configured to be disabled if Vccp = 5V,
; and run with the maximum period for both the watchdog timer and
; the real time interrupt timer.
;=================================================================
START:
   SETC   CNF
   CLRC   OVM    ; Reset overflow mode
   CLRC   SXM    ; Reset sign extension mode
   CLRC   XF
   SETC   INTM      ; Set global interrupt mask
; Set DP to first peripheral file page, 0x7000-7f.
   LDP #DP_PF1
; initialize WDT registers
   SPLK   #06Fh, WDTCR ; clear WDFLAG, Disable WDT, set WDT for 1
                       ; second overflow (max)
   SPLK   #07h, RTICR  ; clear RTI Flag, set RTI for 1 second
                       ; overflow (max)
;configure SYSCLK=CPUCLK/2 after reset
   LACC   CKCR0        ; ACC=CKCR0
   OR     #01h         ; set PLLPS=1
   SACL   CKCR0        ; and write back to CKCR0
;=================================================================
; The following section of code executes only once, on power-up.
;=================================================================
; Detect Power On Reset
PORCHK:   BIT SYSSR,BIT15
   BCND   ILLCHK,NTC   ;if power on reset continue,
                       ;  else branch to next reset source
; set up PLL clockin=10Mhz,CPUCLK=20Mhz,SYSCLK=10Mhz
   SPLK   #00b1h,CKCR1
   SPLK   #0081h,CKCR0
; Clear all reset status bits: POR, ILLADR, WDTRST, SWRST
   LACC   SYSSR
   AND #0FFh
   SACL   SYSSR
; Set up CLKOUT to be SYSCLK
   SPLK   #4080h,SYSCR
```

```
; Wait until PLL is locked before executing main section of code
PLLCHK:   BIT CKCR0,BIT5
   BCND   PLLCHK,NTC
             ;Any additional initialization code may be
             ;inserted here.
   B  MAIN
;===============================================================
; This ends the power-up code section and begins the reset source
; identification section. The following code checks for Illegal
; Address, Software, and Watchdog resets. If found, the
; corresponding bit in the system status register, SYSSR, is
; cleared. In addition to clearing the status bits, the user may
; execute code specific to each reset type before executing the
; main code.
;===============================================================
ILLCHK:   BIT SYSSR,BIT12
   BCND   SWCHK,NTC
   LACL   SYSSR
   AND #0EFFFh       ;Clear ILLADR bit
   SACL   SYSSR
             ;User specific code may be inserted here.
   B  MAIN
SWCHK: BIT SYSSR,BIT10
   BCND   WDCHK,NTC
   LACL   SYSSR
   AND #0FBFFh       ;Clear SWRST bit
   SACL   SYSSR
             ;User specific code may be inserted here.
   B  MAIN
WDCHK: BIT SYSSR,BIT9
   BCND   EXTRST,NTC
   LACL   SYSSR
   AND #0FDFFh       ;Clear WDRST bit
   SACL   SYSSR
             ;User specific code may be inserted here.
   B  MAIN
EXTRST:   NOP        ;User specific code may be inserted here.
MAIN:
```