Galvanic Isolation of a 1394 Node

Burke Henehan
Texas Instruments
bhenehan@ti.com

Can I Teach What You Need to Know in 1/2 Hour?

- NO
- Need to Read App Note and Sections of 1394-1995 & P1394a (in app note)
- Will Cover the Most Asked Questions & Newly Added Information
  - When Might I Need Isolation?
  - How Does Bus Holder Isolation Work?
  - What Signals Do I Need to Initialize?
  - Do I need a large Cap to Decouple GNDS?
  - How Do I Check Isolation?

The Problem:

- All PHYs on a single 1394 bus must be at the same GND potential for speed signaling (and other thresholds & levels) to function correctly.
  - In the 6-pin cable this is accomplished by connecting all PHY GNDs together using the cable GND of the cable power-GND pair.
  - In the 4 pin cable this is done using the cable shields.

Does a 1394 Std. Require Isolation?

- 1394-1995 can be construed to require Isolation. But industry interpretation is that it is NOT required.
- 1394a Explicitly states isolation is NOT required by the Standard and removes most mention of it.
- The Microsoft/Intel PC99 specification does NOT require isolation

Does a 1394 Node Require Isolation?

- A Node MAY require Isolation if it can be connected to another non-isolated node that COULD connect its PHY ground to its chassis ("green wire") GND. OR if the second node's PHY GND could be connected to another device that could be connected to chassis GND; OR if that device could have its GND connected to another device's chassis GND; OR ...

No Galvanic Isolation

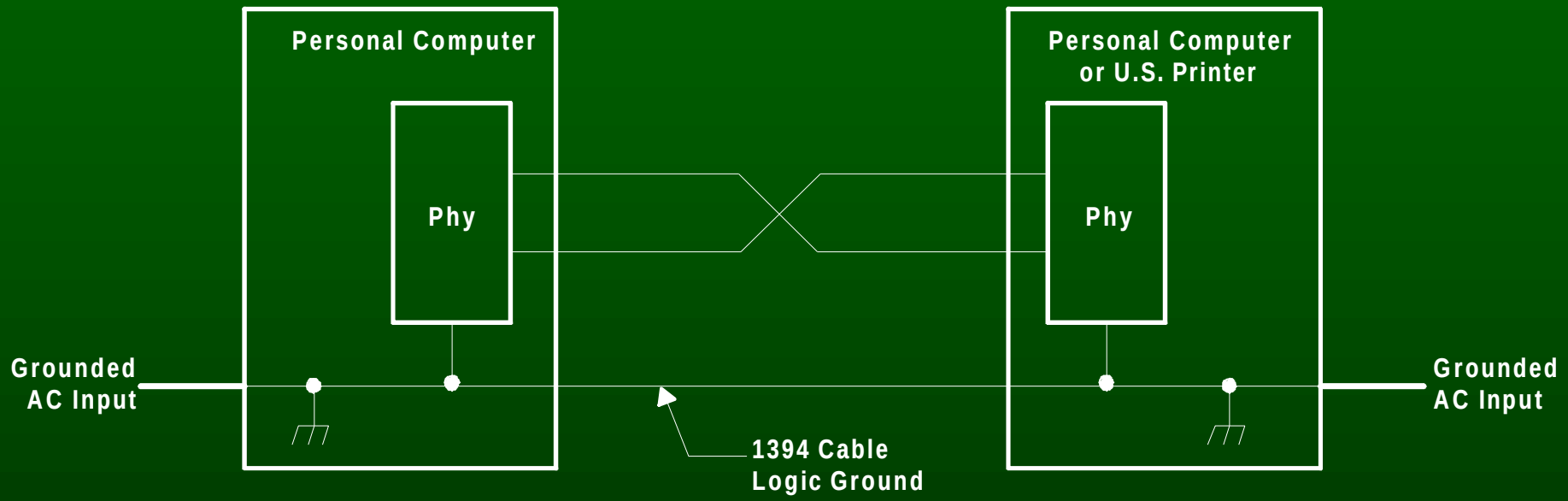


Figure 1. No Galvanic Isolation

Potential Ground Loop

nf - *Penalties of Ground Loops*

- Degradation of data signals on the cable
- EMI from the cable
- Ground currents high enough to damage components in the system
- If the potential difference is large enough, a personal shock hazard.

Node Only Powered by Cable with No External Connections - No Isolation Needed

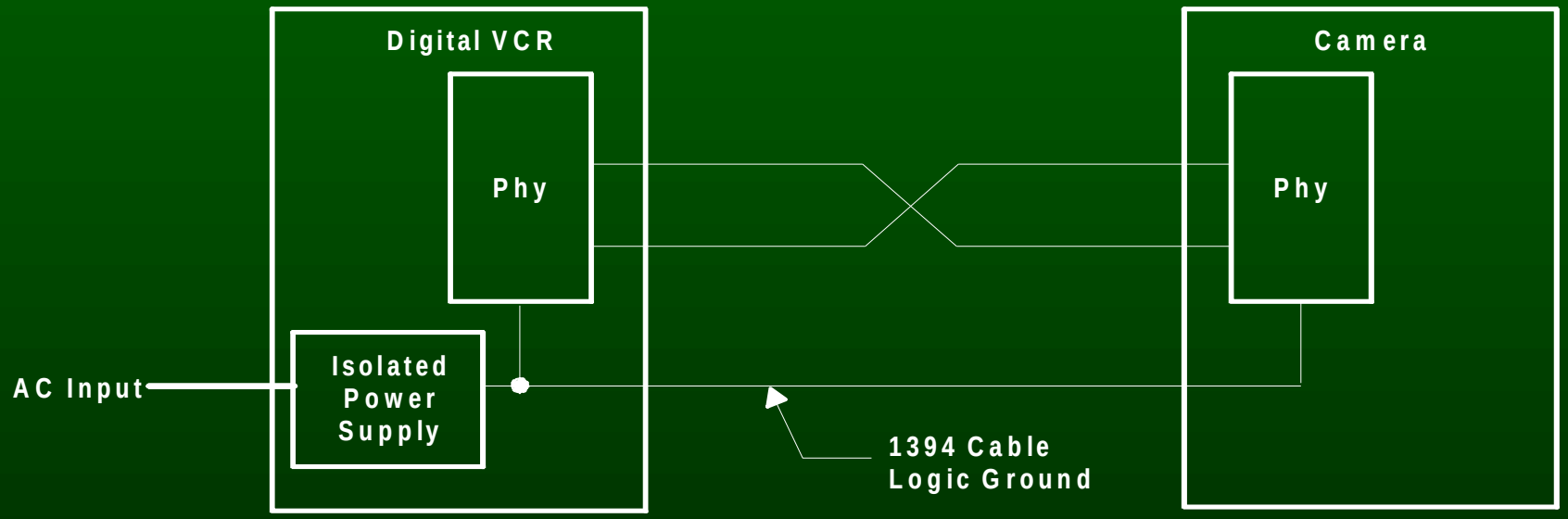
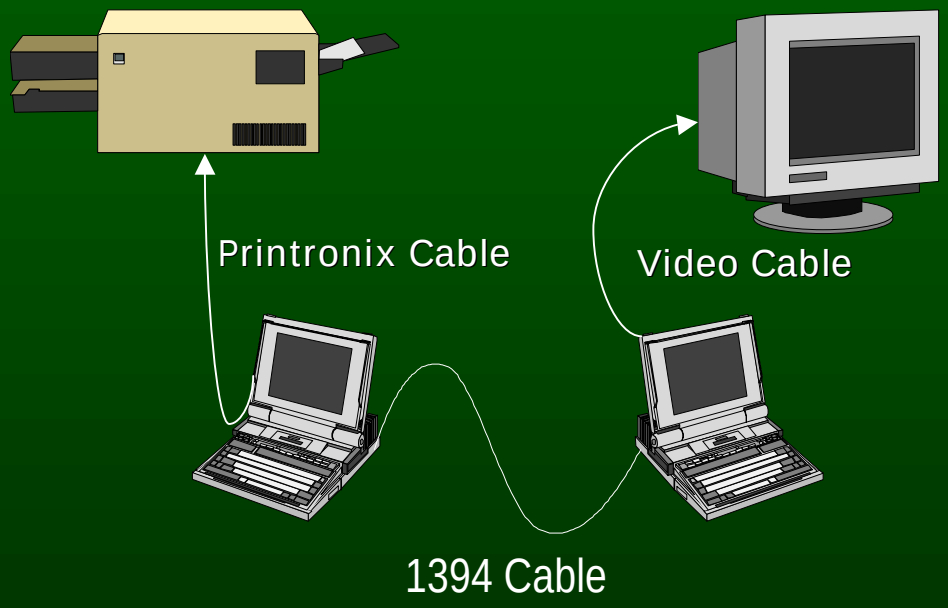


Figure 3. Leaf Node Not Requiring Isolation

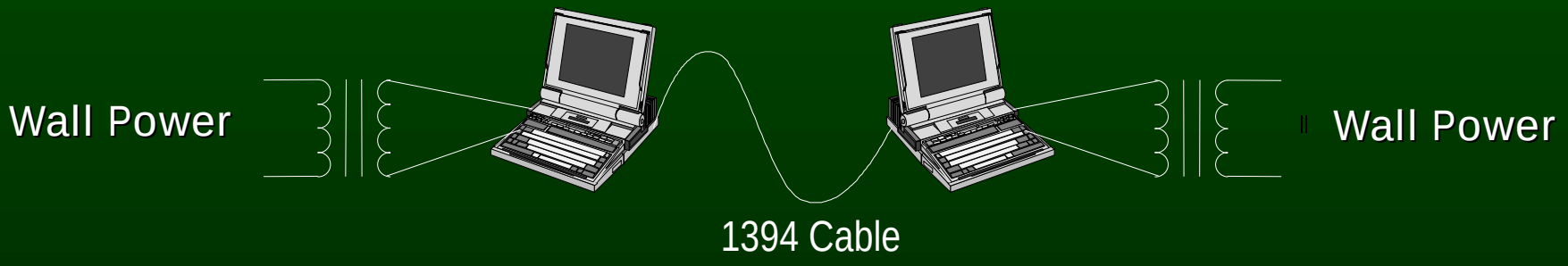
Example: When Might I Need Galvanic Isolation of the 1394 Bus?



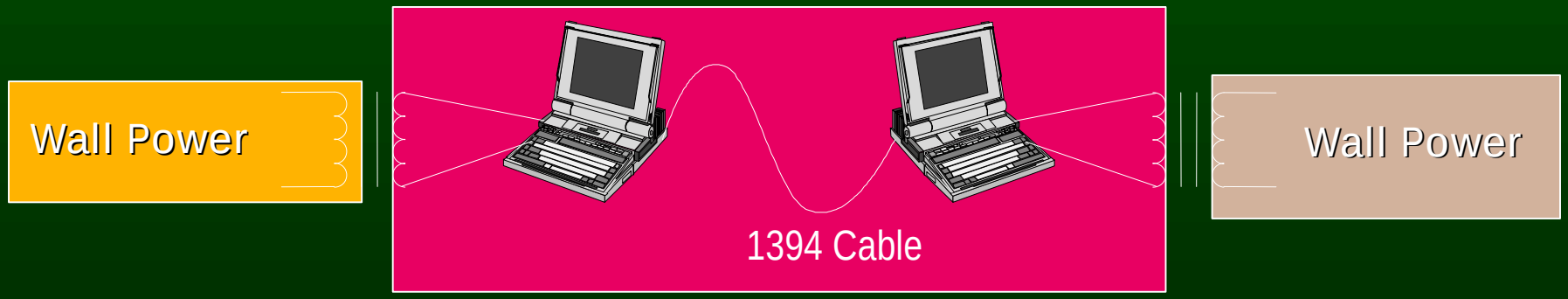
Laptop PC Example Assumptions:

1. No 1394 Galvanic Isolation Used

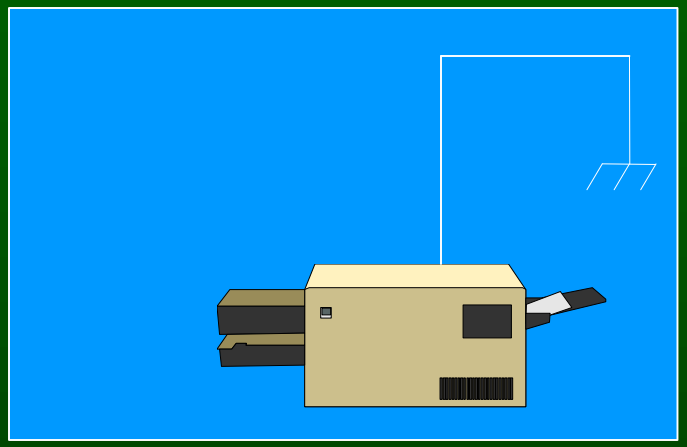
2. Laptops Use Isolating Transformers

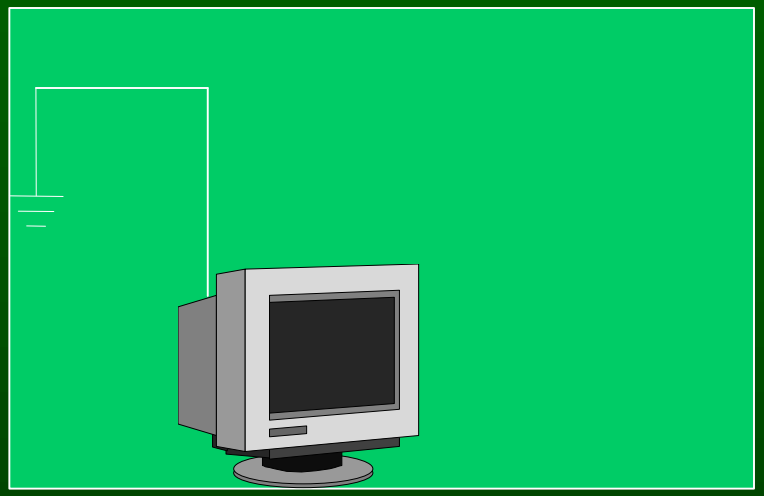


Actually 3 Possible Distinct GND Domains

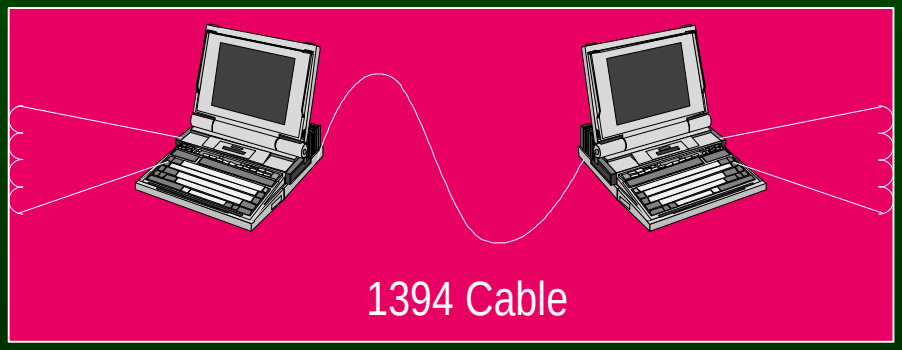


Now What about Peripherals!



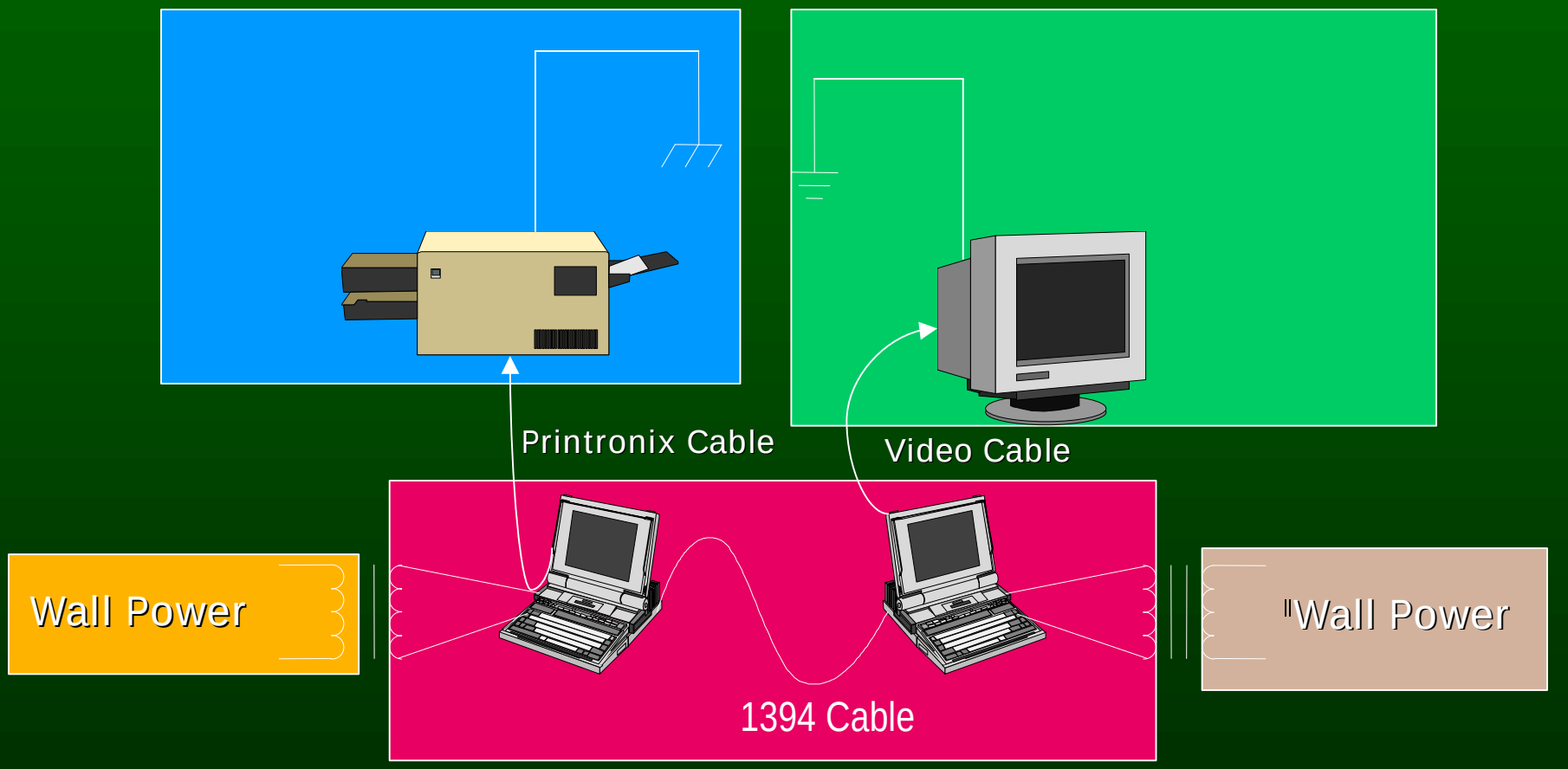


Wall Power

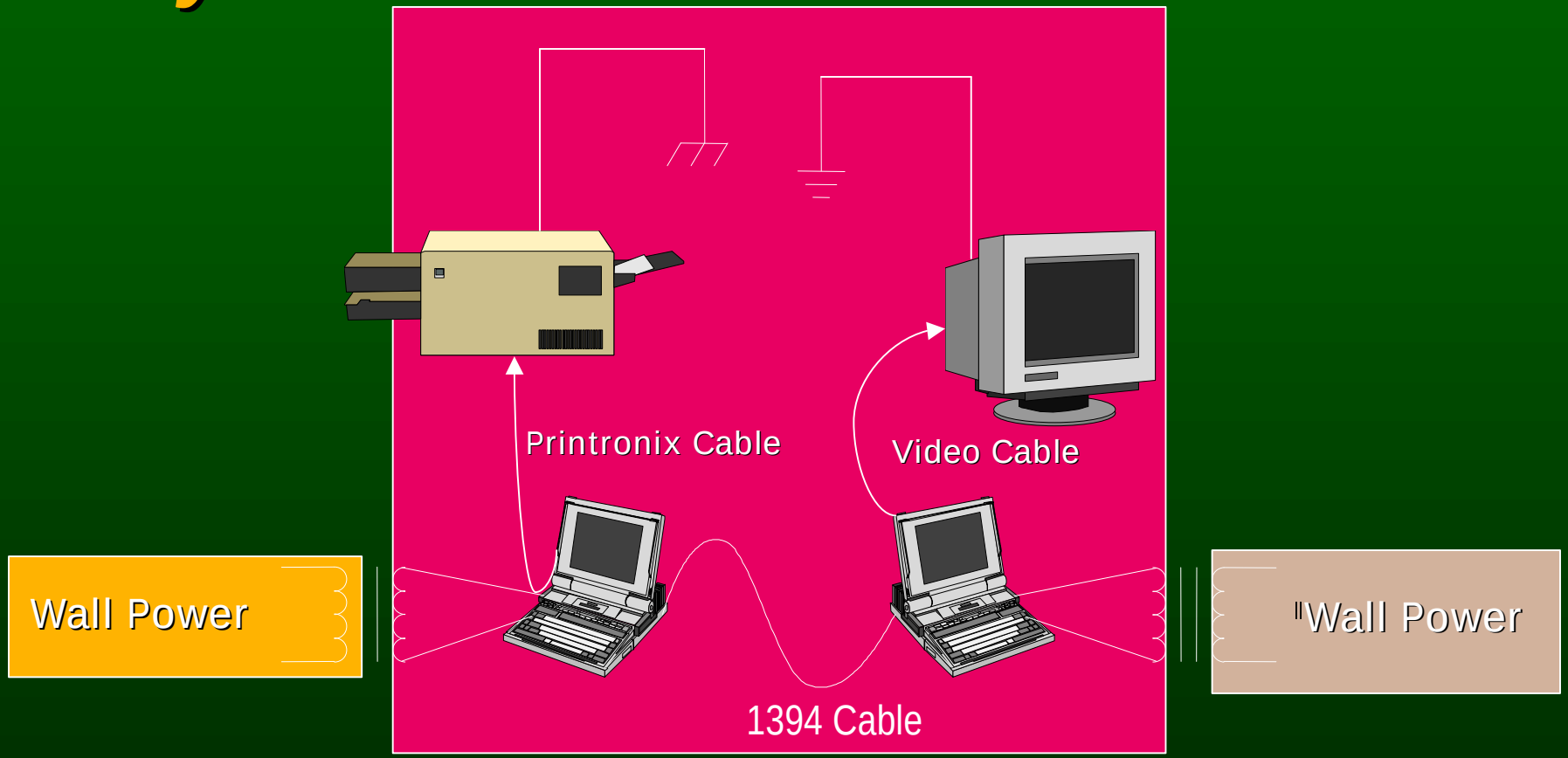


Wall Power

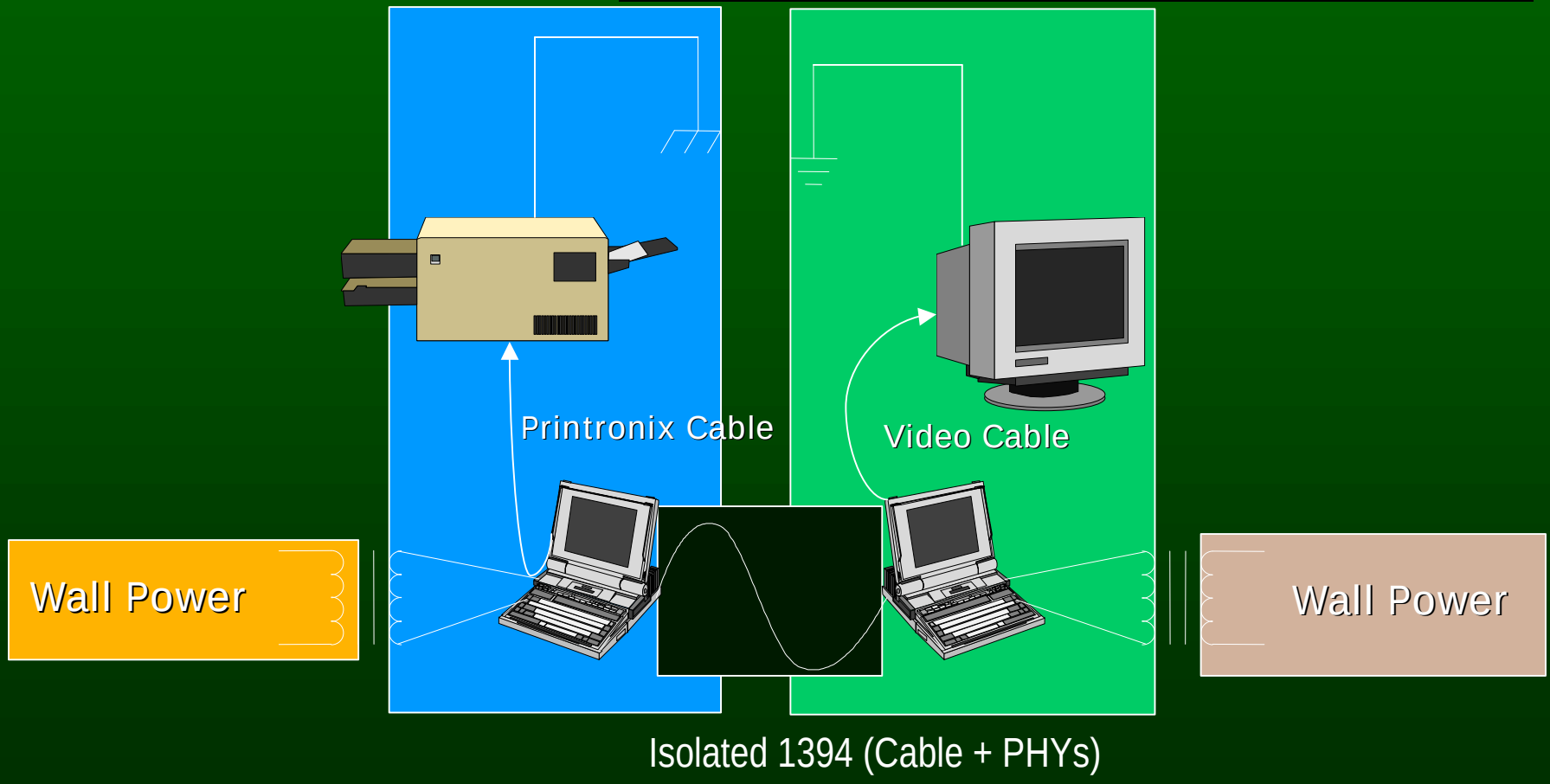
Fine Until Plug in Peripherals



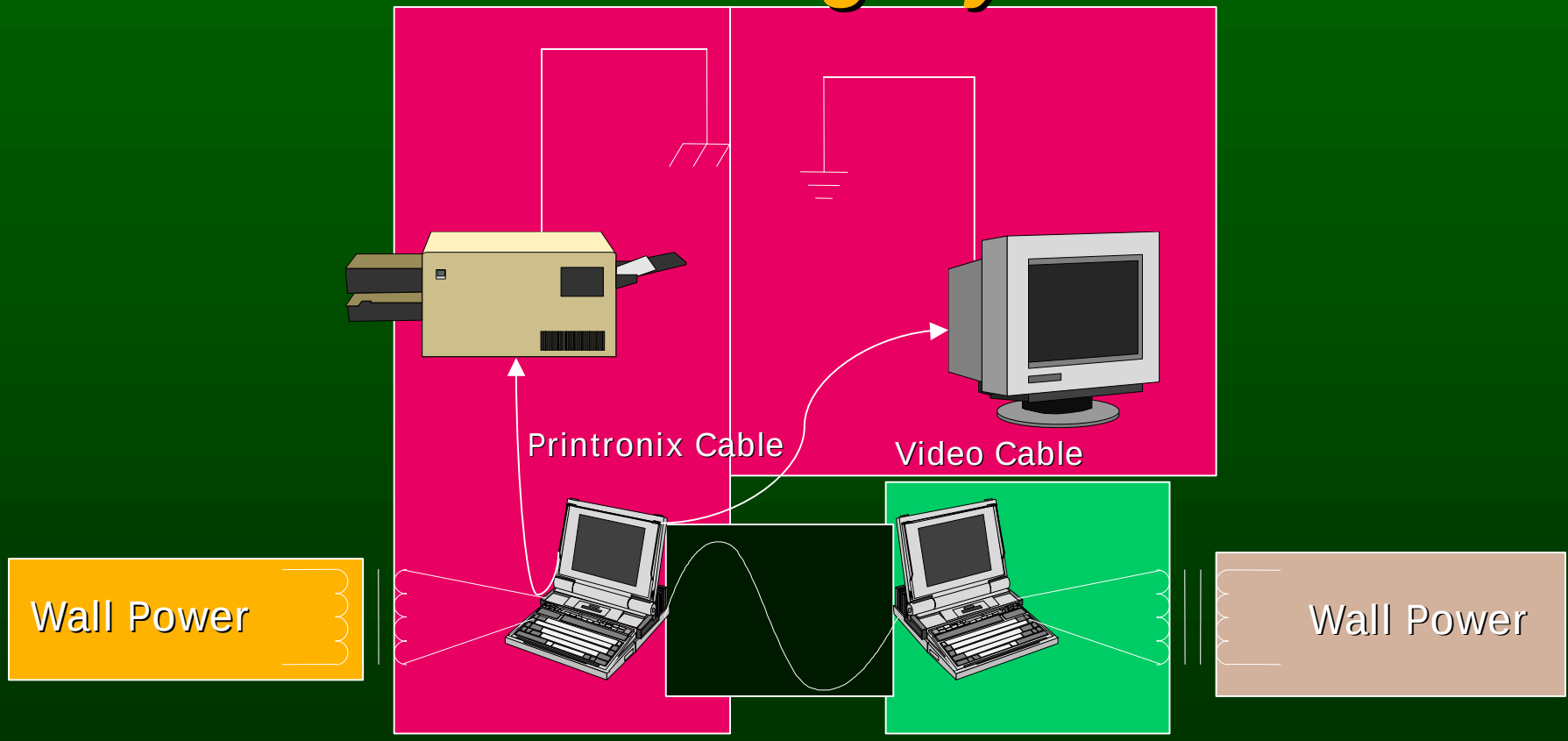
Ground Domains Will Try to Equalize. May Get GND Currents in all 3 cables



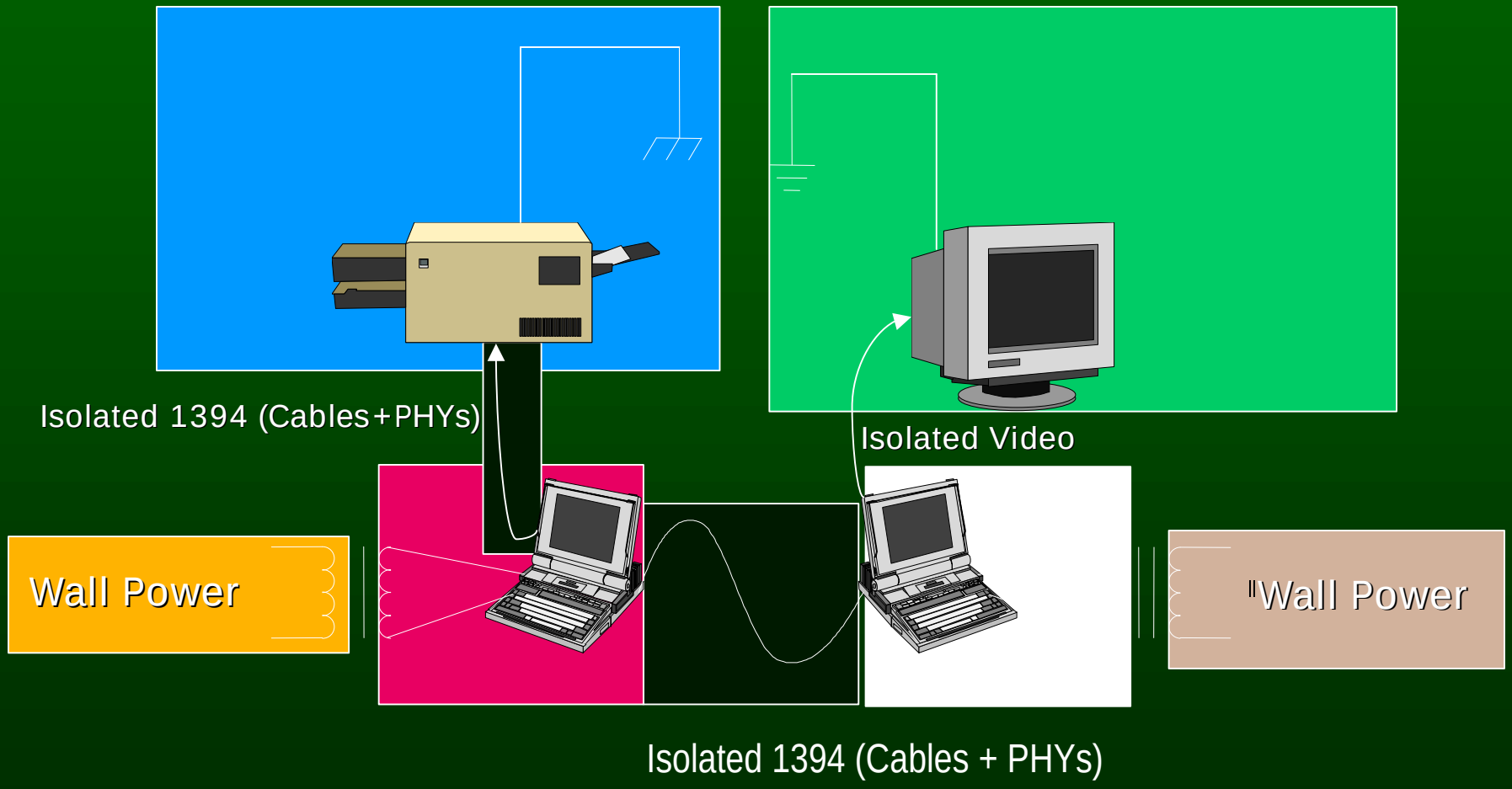
If Add Isolation to 1394, Solve Isolation Problem… For THIS Configuration



Even With 1394 Isolation a Problem is Possible with Legacy Connections



Only if All Connections are Isolated are GND Currents Prevented



If Isolation is Required, What Must be Done?

- Cable Power Isolation
  - Must be 8->33V relative to PHY GND, floating relative to chassis GND
- Cable Shield Termination Isolation
  - DC Isolated via capacitive network
- Signal Line Isolation
  - TI Proprietary Bus Holder Isolation
  - Other Solutions Available
    - 1394-1995 Annex J covered by Apple Patent

Implementation of Isolation Using Bus Holder Isolation (see app note)

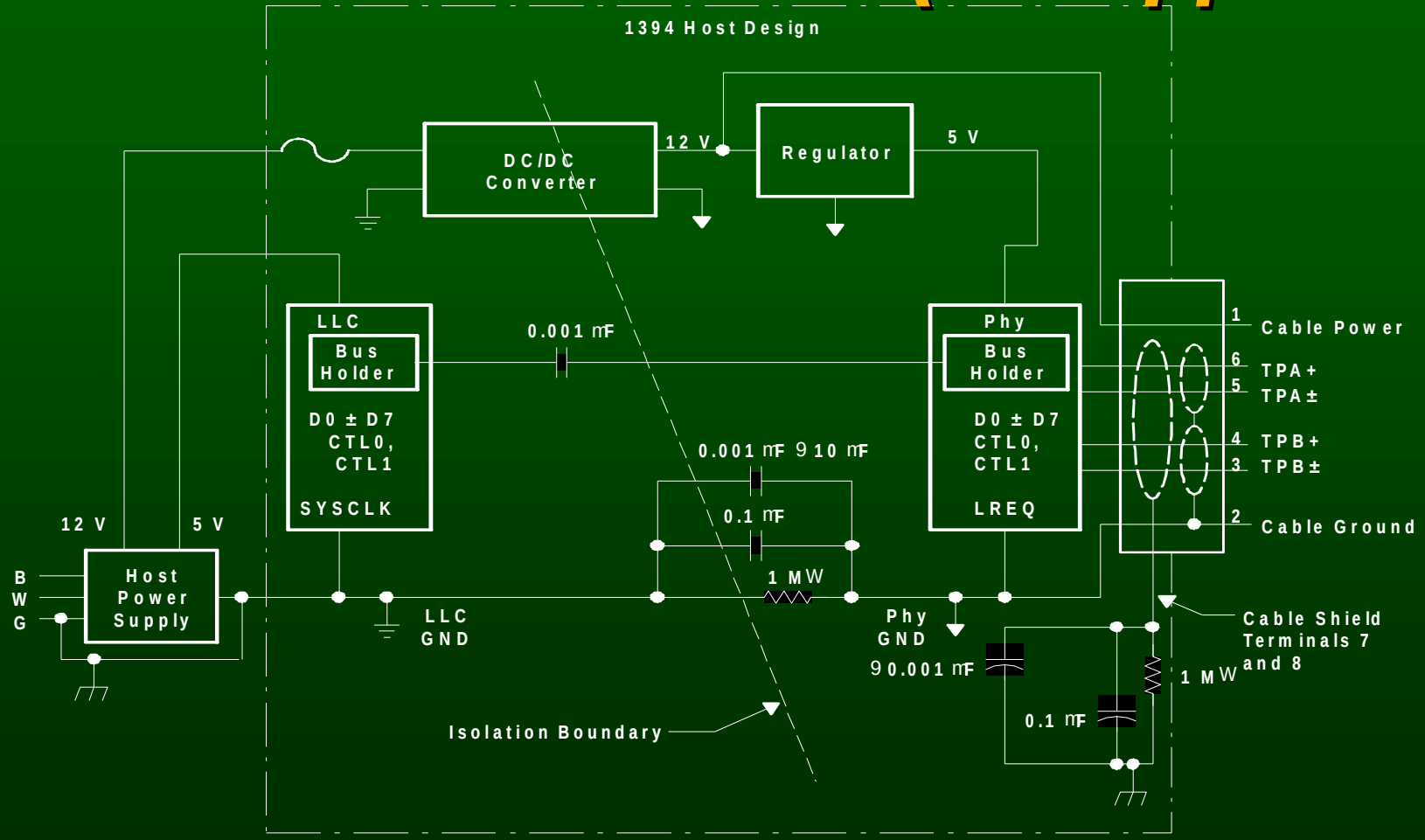


Figure 8. InternalBus-Holder Isolation

Implementation of Isolation Using Bus Holder Isolation - GND Domains

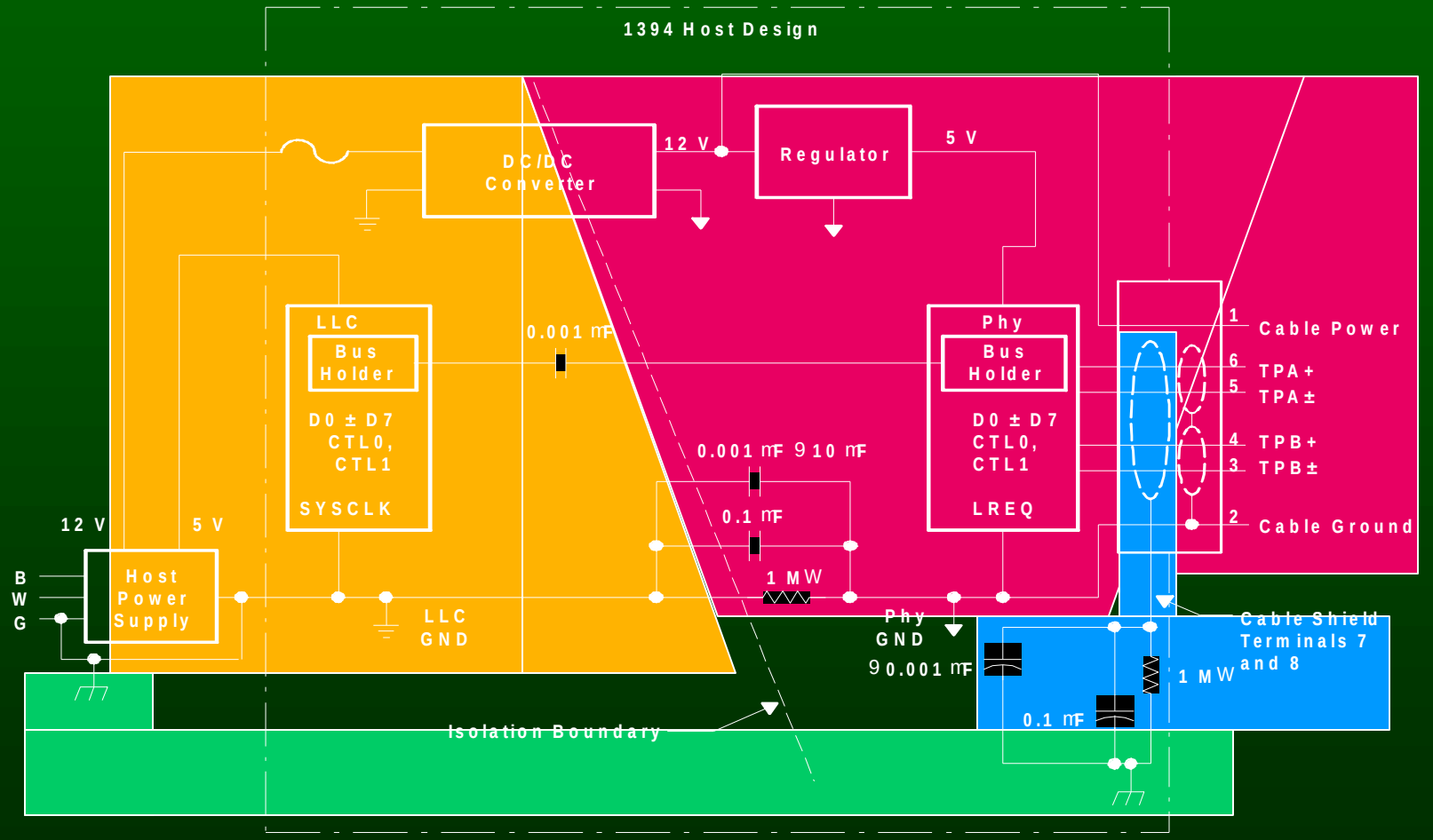


Figure 8. InternalBus-Holder Isolation

Bus Holder Functionality

Local GND relative
to reference GND = 30V

Local GND relative
to reference GND = 20V

Difference between GNDs is 30-20 = 10V

Voltage Level = 30V
Logic Level = Low

Voltage Level = 20V
Logic Level = Low

Signal Level
Time->

Signal Level
Time->

Isolation Boundary

Reference GND = 0.0 V

No Bus Holders

Local GND relative
to reference GND = 30V

Local GND relative
to reference GND = 20V

Voltage Level = 33V
Logic Level = High

Voltage Level = 23V->20V
Logic Level = High to Low

Signal Level

Time->

Signal Level

Time->

Isolation Boundary

Reference GND = 0.0 V

With Bus Holders

Local GND relative
to reference GND = 30V

Local GND relative
to reference GND = 20V

Voltage Level = 33V
Logic Level = High

Voltage Level = 23V
Logic Level = Captured High

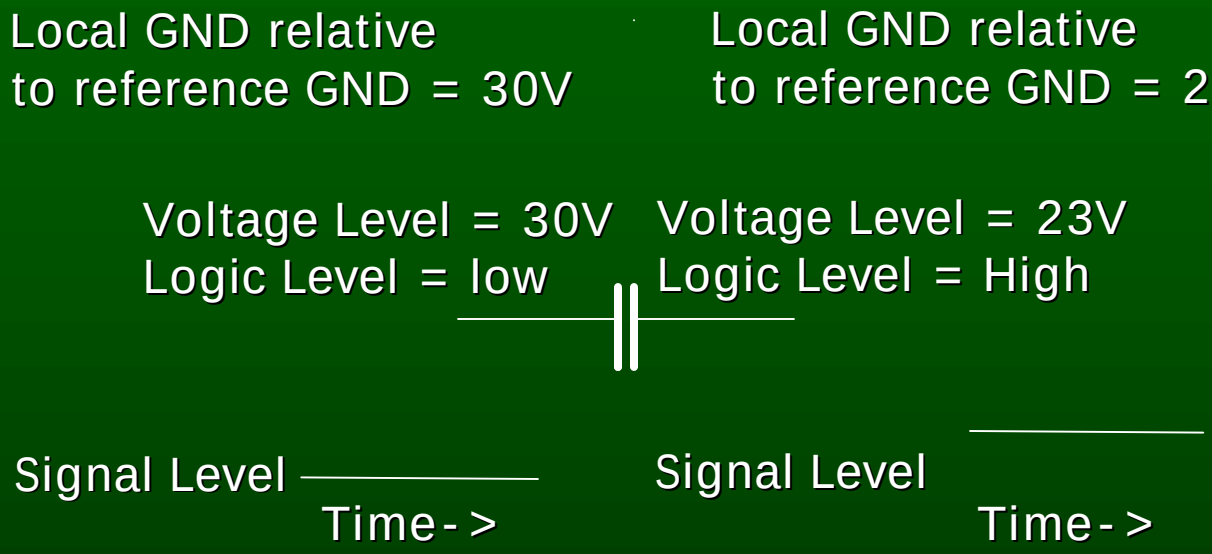
Signal Level
Time->

Signal Level
Time->

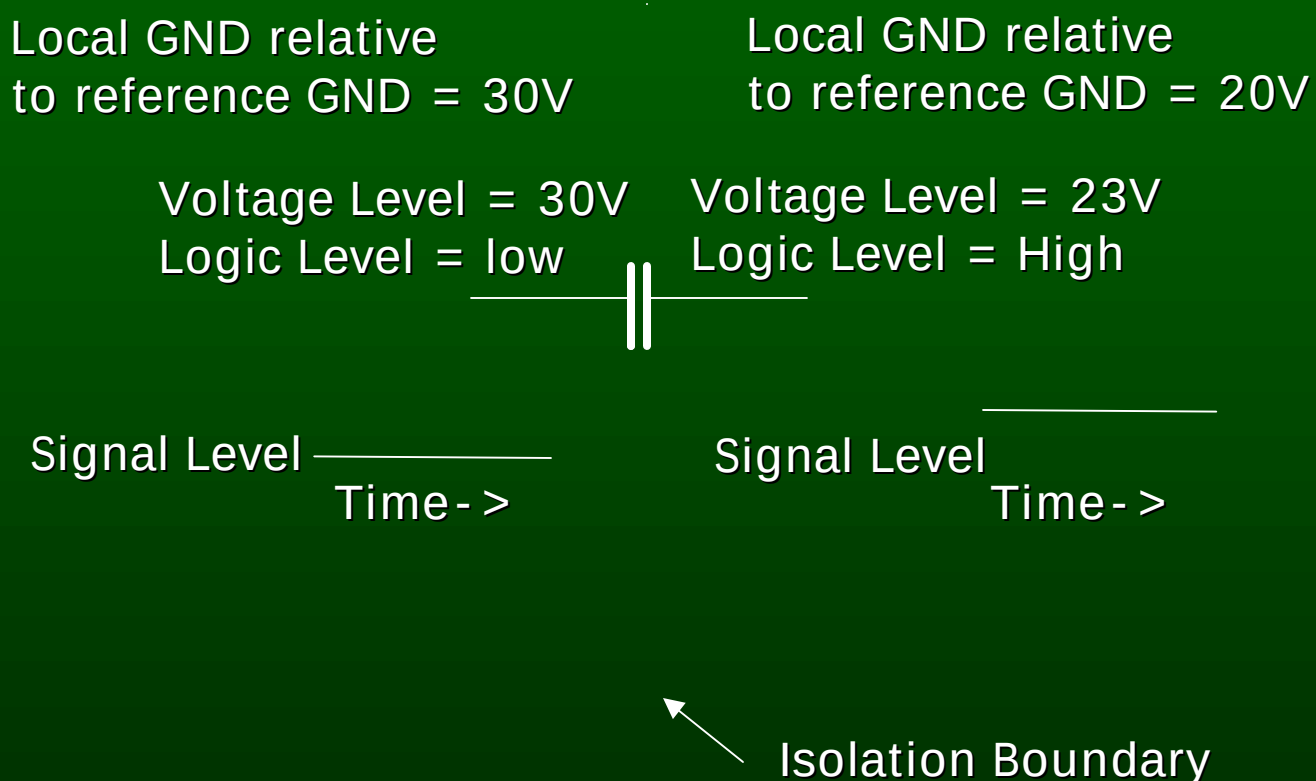
Isolation Boundary

Reference GND = 0.0 V

Initialization of Capacitive Isolation After Power-Up, GND Bounce, etc



Assume "Left" Side Begins by Driving a 0 (low), Bit Propogated is Wrong!



Assume “Left” Side Then Drives a 1 (High), Interface Now Synchronized

Local GND relative
to reference GND = 30V

Voltage Level = 33V
Logic Level = High

Signal Level

Time->

Local GND relative
to reference GND = 20V

Voltage Level = 23.6V
Logic Level = High

Signal Level

Time->

Isolation Boundary

Reference GND = 0.0 V

Assume "Left" Side Then Drives a 0 (Low)

Local GND relative
to reference GND = 30V

Local GND relative
to reference GND = 20V

Voltage Level = 30V
Logic Level = Low

Voltage Level = 23.6V->20.0V
Logic Level = Low

Signal Level

Time->

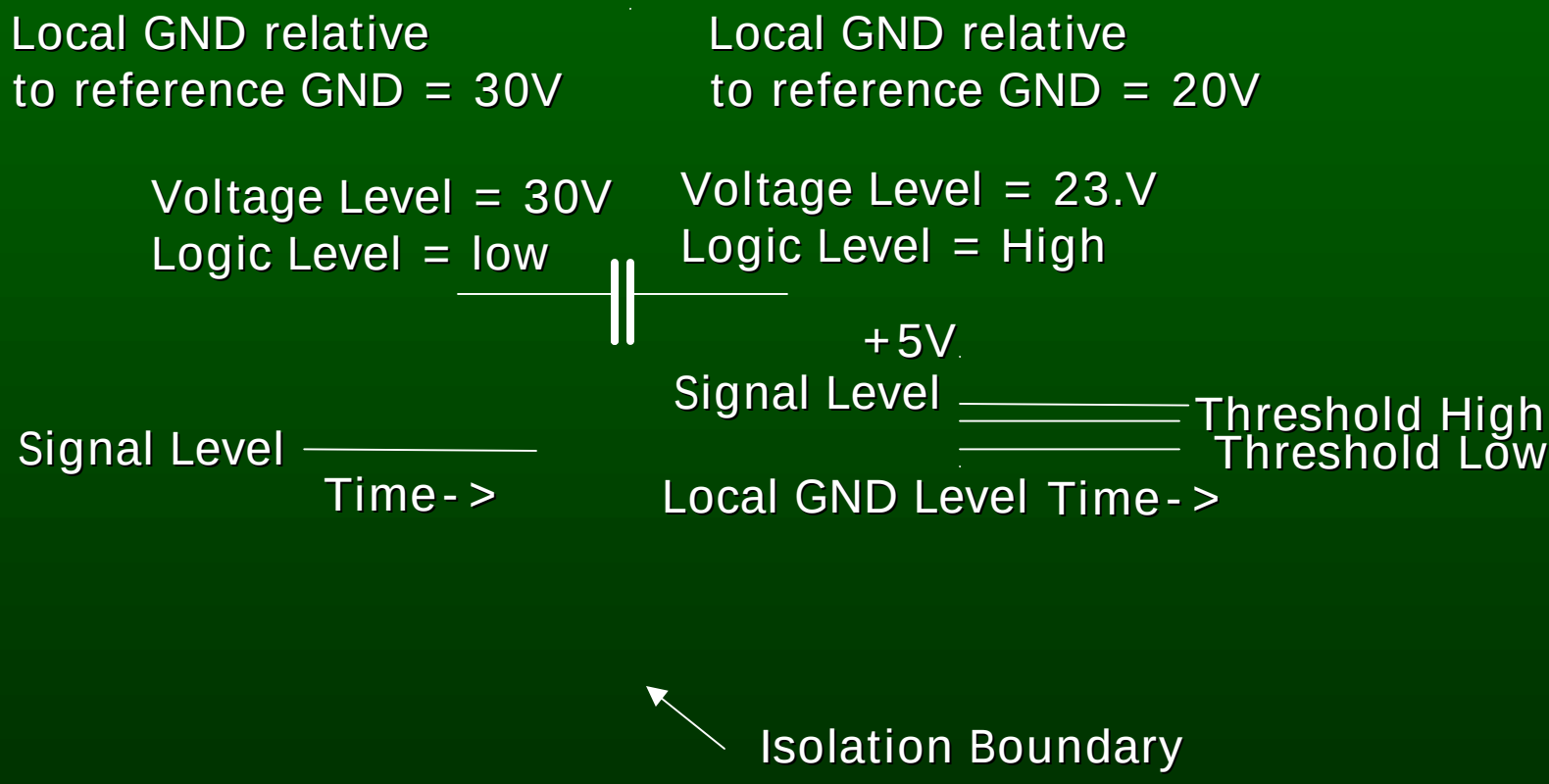
Signal Level

Time->

Isolation Boundary

Reference GND = 0.0 V

Oscillating Signal Driven to 5V tolerant Device, Initial State out of Sync



Now Left Side Drives Oscillating Signal Which Never Crosses Low Threshold

Local GND relative
to reference GND = 30V

Local GND relative
to reference GND = 20V

Voltage Level = 30V
Logic Level = low

Voltage Level = 23.V
Logic Level = High

+5V

Signal Level

Threshold High

Threshold Low

Signal Level

Time - >

Local GND Level

Time - >

Isolation Boundary

Reference GND = 0.0 V

So What Signals do I Need to Initialize?

- *ALL OF THEM*
  - Every Signal must have HW that initializes both sides of the isolation barrier to the same state upon:
    - Powerup
    - Command from the Microprocessor (Link) side of the PHY-Link Interface (in case of wrong state induced during normal operation)

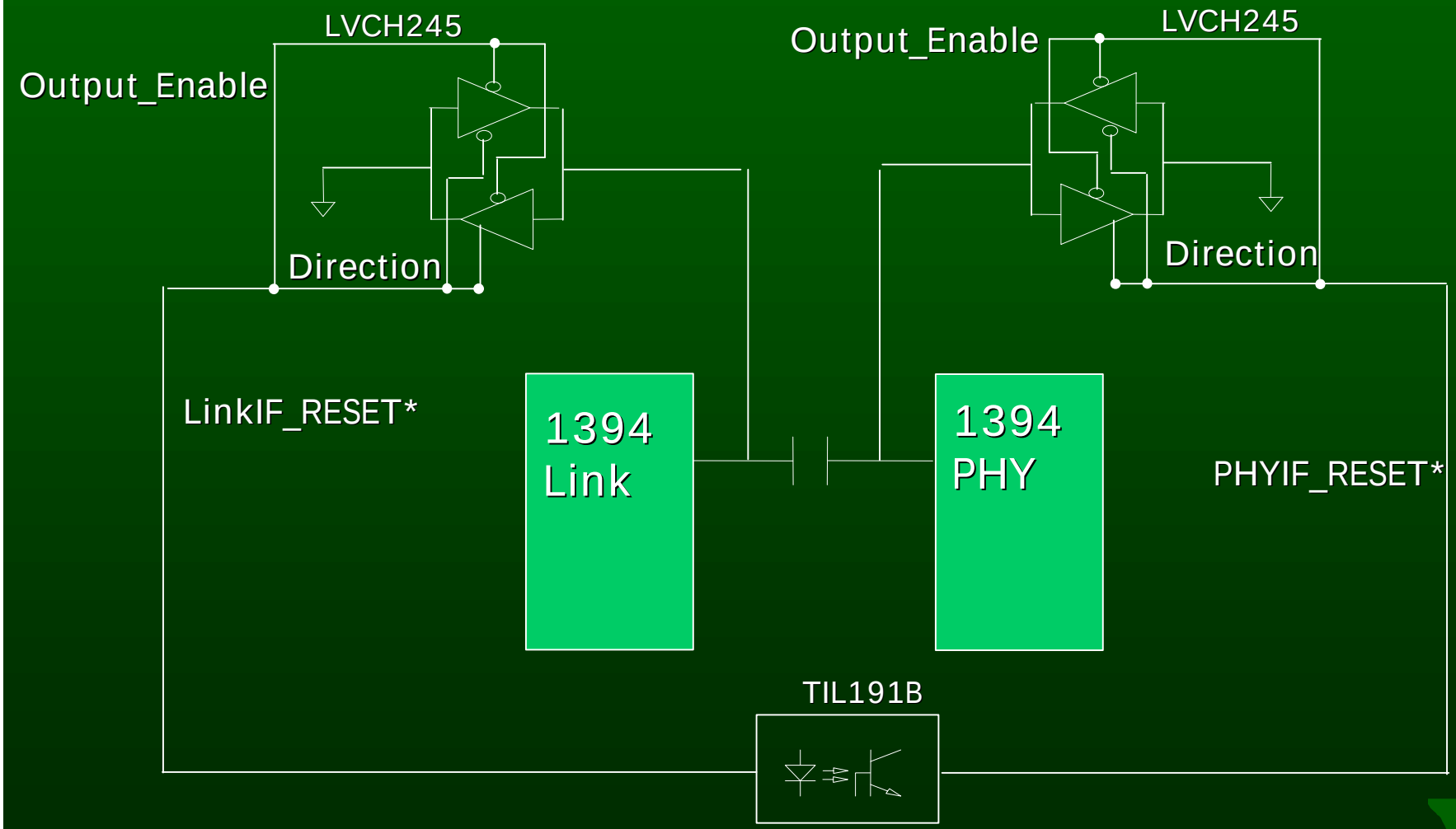
How May Initialization Be Done?

- 1394a Link and Phy
- External Buffers on Each Side of Isolation Barrier (to drive a state)
- Opto-isolators (active drivers to establish states)
  - Currently there are no known opto-isolators fast enough and with low enough latency to operate on the data, control, SCLK, or LREQ signals
- Etc.

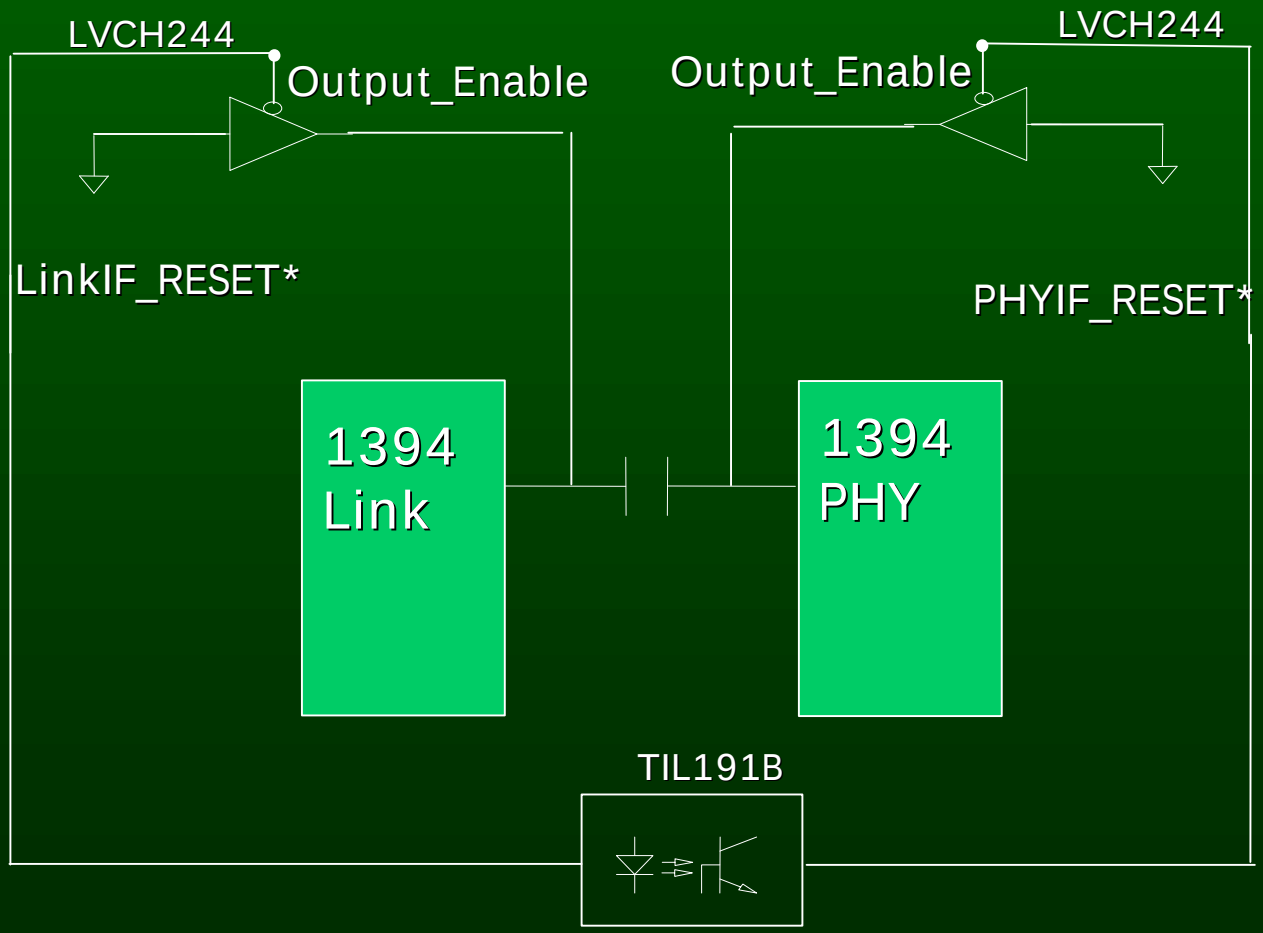
1394a PHY-Link Interface Initialization

- When SCLK is valid the PHY drives Data & CTL low for 7 clocks while the link drives Data, CTL, & LREQ low for 1 clock then makes them high impedance
- On the 8th Cycle the PHY drives Receive on CTL & Data Prefix on Data

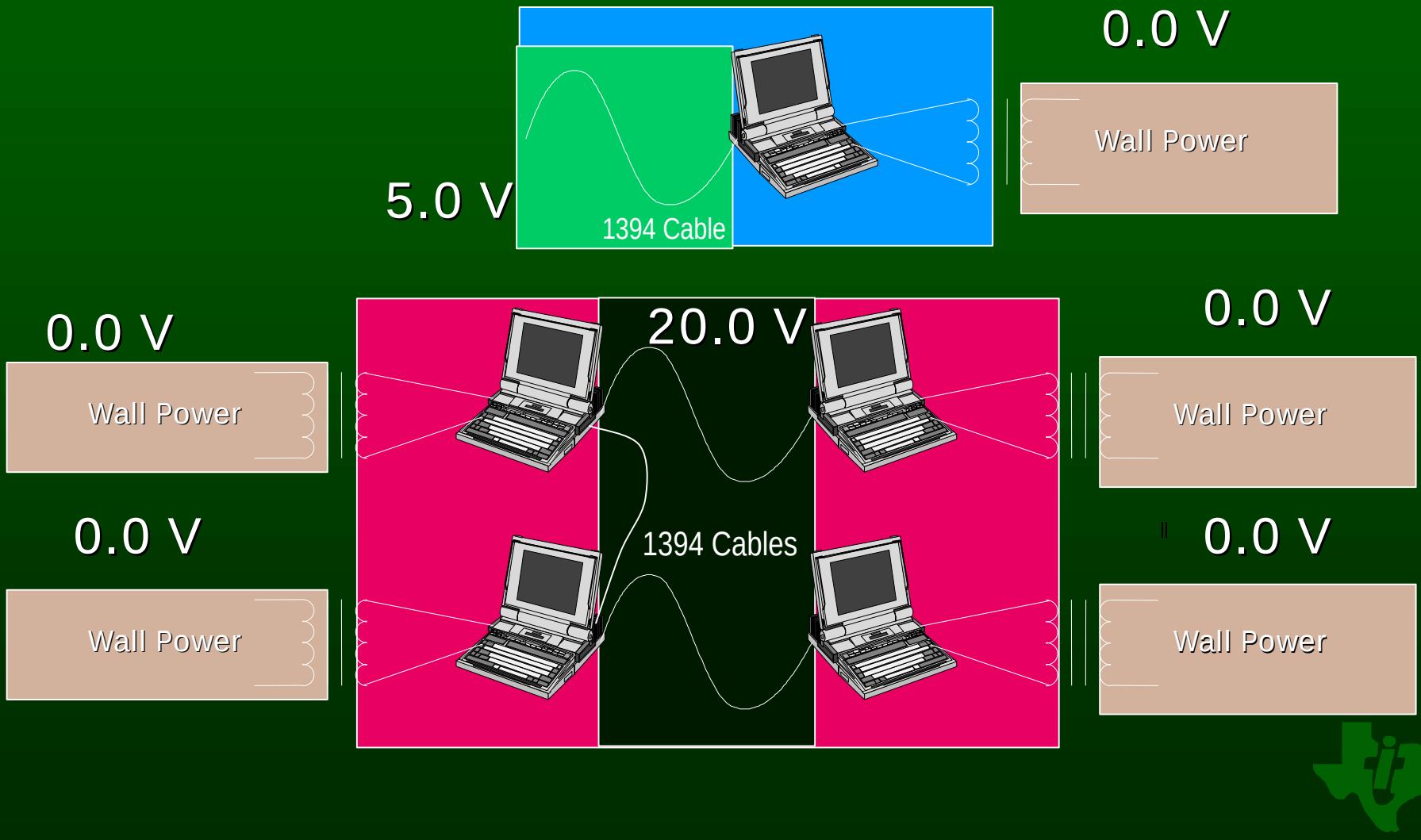
External Bus Holder, Non-1394a PHY-Link Interface Initialization



Internal Bus Holder, No 1394a PHY-Link Interface Initialization



What Happens when plug top node into bottom network?



Implementing Isolated Nodes

- Putting in isolation adds unknowns to board debug
- Build Enough Boards to:
  - Build the first set of nodes with the isolation shorted out (replace caps with 0 Ohm resistors) to get 1394 working
  - Keep "known good set" (or give to SW team)
  - Build up Isolated boards one step at a time

Implementing Isolated Nodes - Continued

- Take Task in Steps
  - Isolate signals, but leave all GND domains the same (install signal isolation caps, leave GND isolation caps shorted)
  - After this functions install GND caps
  - Offset floating domain to verify isolated
- Need access to both sides of isolated interface
- Be Aware of Different GND Domains!

nf Advantages of Bus Holder Isolation

EXAMPLE COMPARISON FOR 400–Mbits/s NODE (DATA, CTL, LREQ, SYSCLK)			
PARAMETERS	**ANNEX J METHOD**	**TI METHOD**	**TI BUS–HOLDER BENEFITS**
External capacitors	22	12	Reduced PWB area Reduced complexity Reduced cost
External resistors	76	2	Reduced PWB area Reduced power Reduced complexity Reduced cost
Voltage swing	$V_{DD}/2$	Rail to rail	Better noise margin
Digital differentiaters on outputs	Required	None	Reduced complexity Reduced cost
Special threshold requirements	Required	None	Reduced complexity Reduced cost
Isolation network power drain	Holds input cells at $V_{DD}/2$	Method causes no impact	Minimal quiescent power drain No special input cell requirement Reduced cost
Hysteresis on inputs	Requires Schmitt triggers on inputs	None	Reduced complexity Reduced cost

References

- TI App Note: "Galvanic Isolation of the IEEE 1394 Serial Bus" - SLLA011 dated in 1998 - www.ti.com/sc/1394
- IEEE 1394-1995 Standard for a High Performance Serial Bus - http://stdsbbs.ieee.org/products/catalog/catalog.html
- IEEE P1394a Draft 2.0 Standard for a High Performance Serial Bus (Supplement)