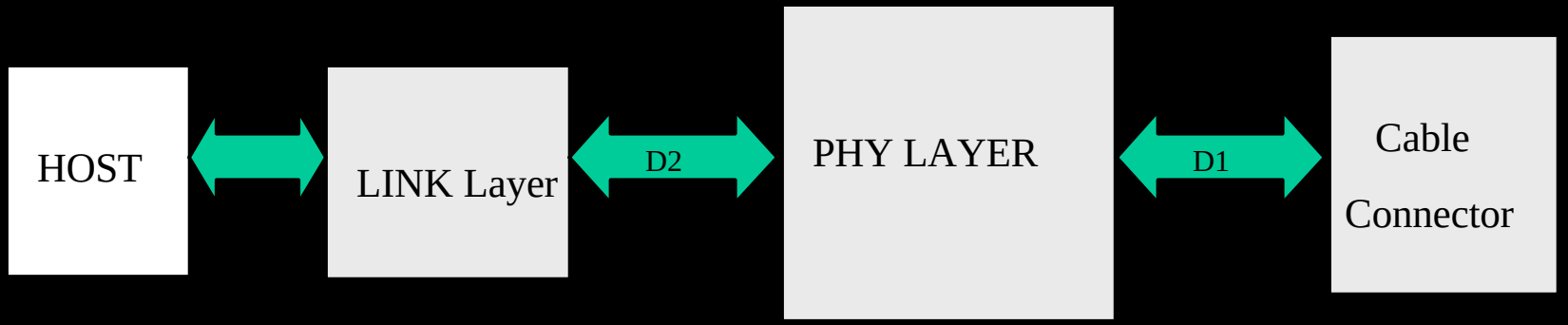
PHY DESIGN RECOMMENDATIONS FOR PCB LAYOUT

Ron Raybarman
s-raybarman1@ti.com
Texas Instruments

Topics of discussion:

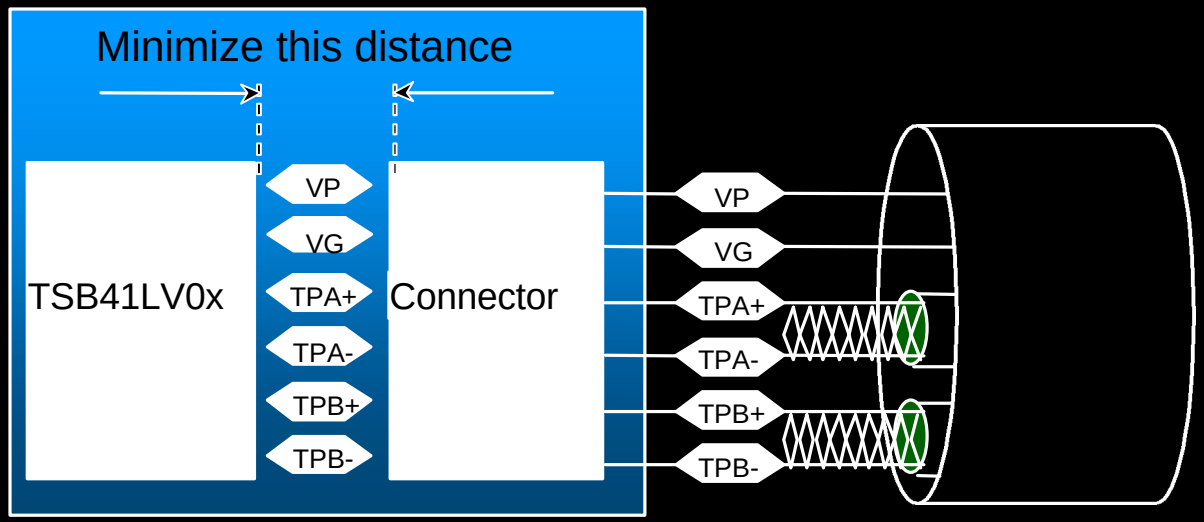
- 1. Specific for 1394 - (Not generic PCB layout)
  - Etch lengths
  - Termination Network
  - Skew reduction
- General EMI Issues

A typical IEEE1394 node environment



- D1 - Distance between PHY and cable connector
- D2 - Distance between PHY and the Link

Minimize etch length between PHY and Connector to:

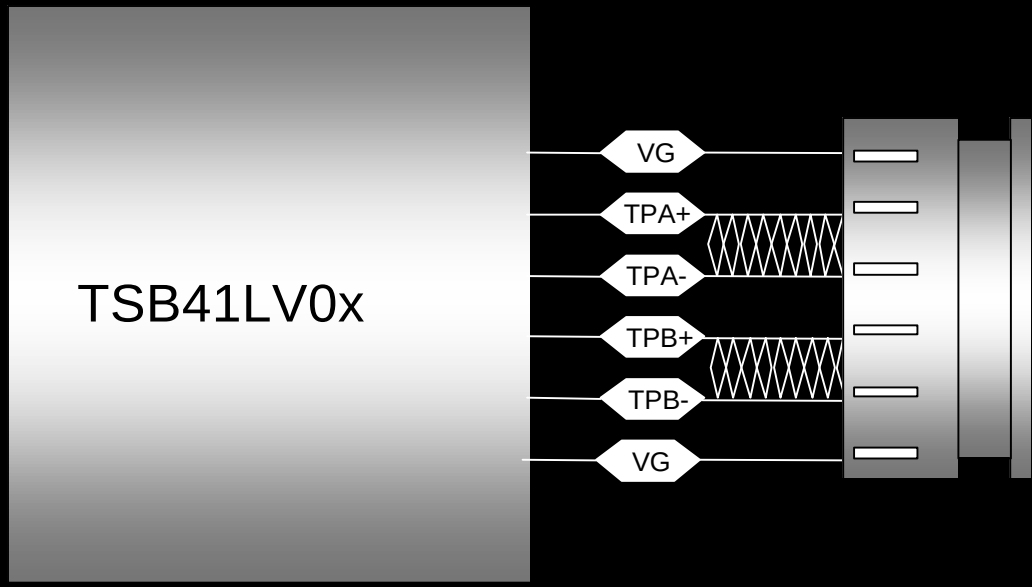


- Minimize transmission line effects
- Minimize differential and common mode noise interference
- Minimize antenna effects

Minimize etch length between PHY and Connector (cont)

Calculating a recommended etch length depends heavily on several factors

- Edge Rates
- Propagation Time
- Matching Impedance



- Transmission line effects
- Antenna effects
- Differential noise interference

Minimize etch length between PHY and Connector (cont)

Rule of thumb for max etch length without matching impedance

$L_{etch} < D_{max} / (2ë)^{0.5}$ or more conservative

$L_{etch} < D_{max}/6$

L_{etch} - acceptable etch length

$D_{max} = T_{risetime} * S$; max distance traveled during risetime

$T_{risetime}$ - risetime

$S = C / (E_r)^{0.5}$; propagation speed of signal

C = speed of light

E_r = Dielectric constant

Minimize etch length between PHY and Connector (cont)

Example of max etch length without impedance match

Conservative example:

- $L_{etch} = (T_{risetime} * S)/divisor\_factor$

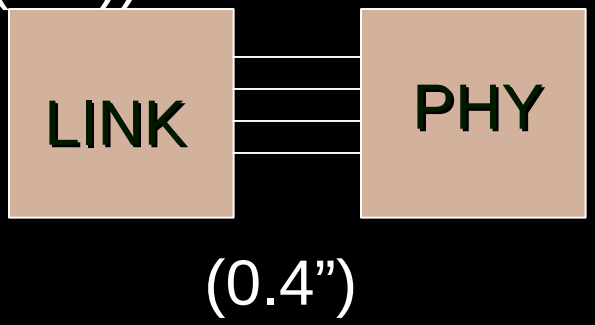
Minimum 1394a Spec risetime = 0.5 ns

Maximum typical FR-4 dielectric constant = 5.3

Maximum divisor factor = 6

L_{etch} = (0.5E -09 s)(2.997E 08 m/s) / (sqrt(5.3)) / 6

L_{etch} = 0.011 meter (0.4”)



Minimize etch length between PHY and Connector (cont)

Example of max etch length without impedance match

Unrealistic best case example:

- $L_{etch} = (T_{risetime} * S)/divisor\_factor$

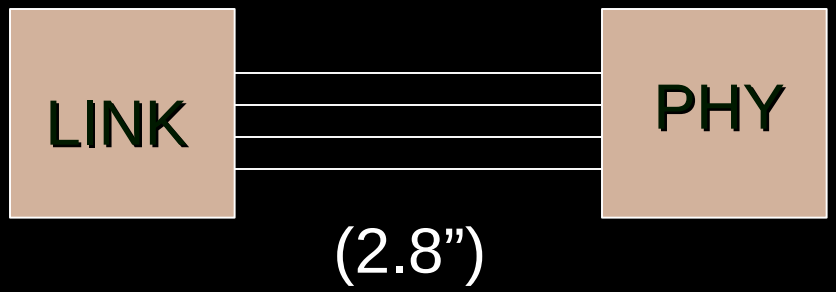
Maximum Spec risetime (400 Mbps) = 1.2 ns

Minimum typical FR-4 dielectric constant = 4.1

Minimum divisor factor = sqrt(2ë) = 2.51

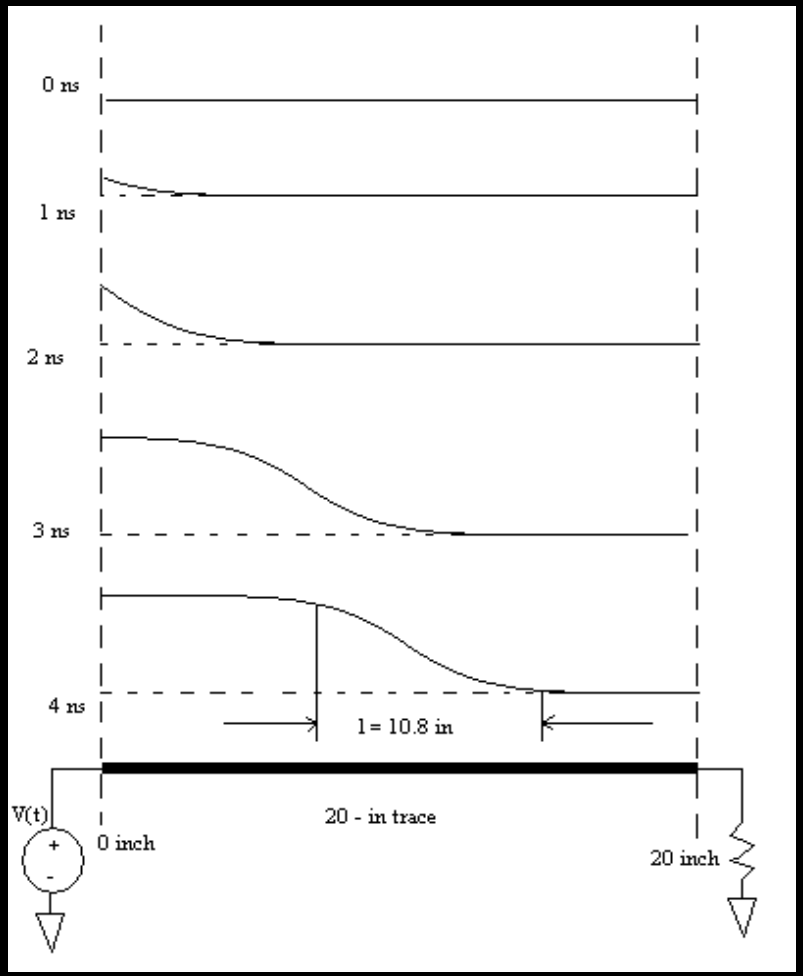
L_{etch} = (1.2E -09 s)(2.997E 08 m/s) / (sqrt(4.1)) /2.51

L_{etch} = 0.071 meter (2.8”)



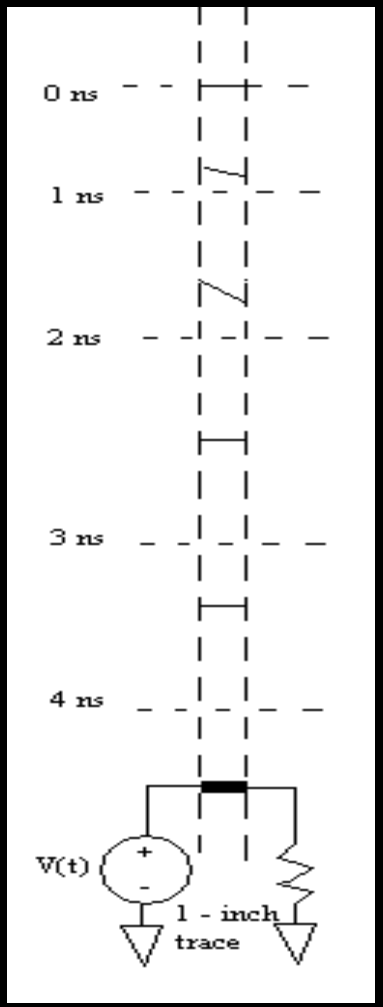
Minimize etch length between PHY and Connector (cont)

For example: When the etch length is 20 inches the signal leading edge wave is distributed across the impedance of the line itself. So there is a voltage drop across the line itself. This forms an etch path that should be treated as a transmission line.



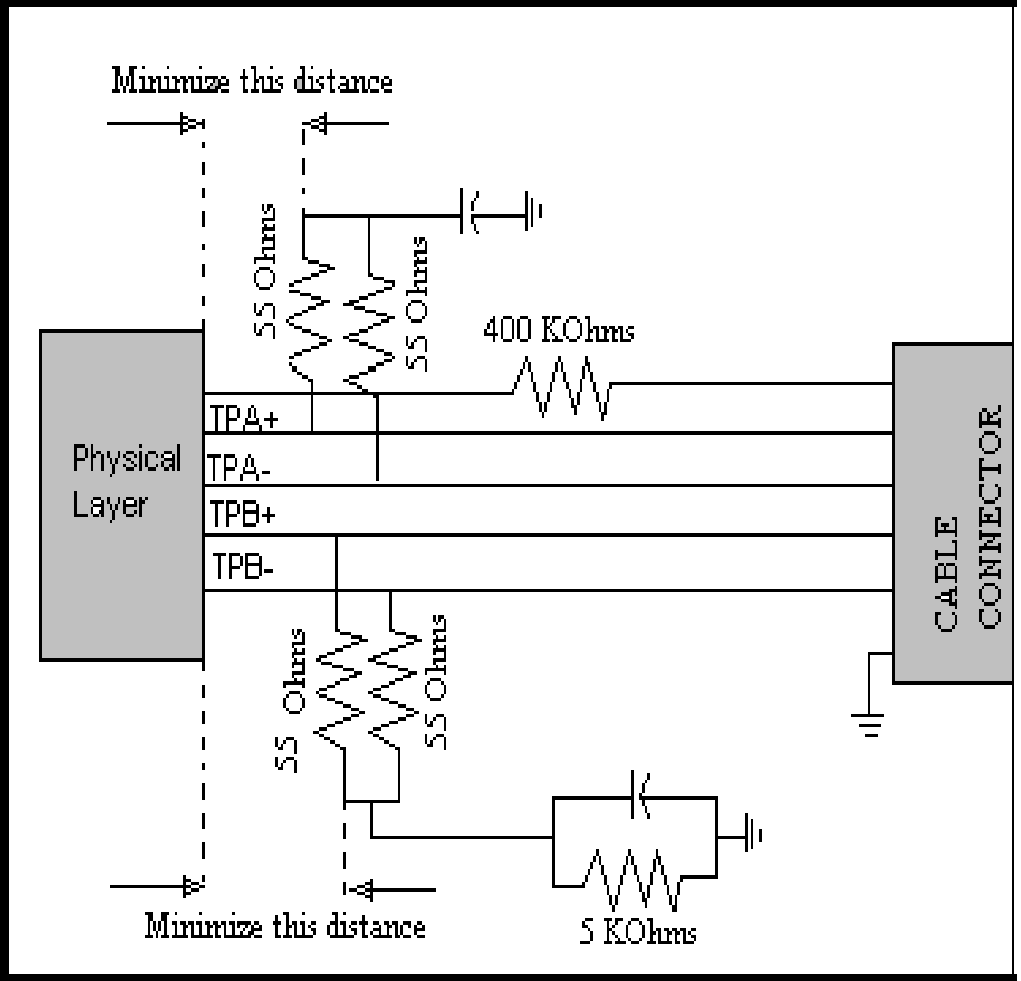
Minimize etch length between PHY and Connector (cont)

In a shorter etch the impedance is uniform . The voltage on every part of this line is (almost) uniform at all times. Therefore if it is short enough it does not need to be treated as a transmission line.



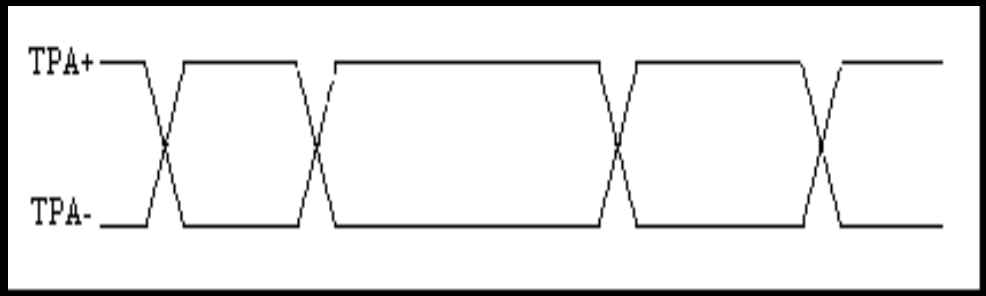
Terminating resistor network

- Termination resistors should be located ACAP to the TP terminals on the PHY
- Terminate to match Impedance of the TP lines
- Minimize stub lengths for reduced antennae effect

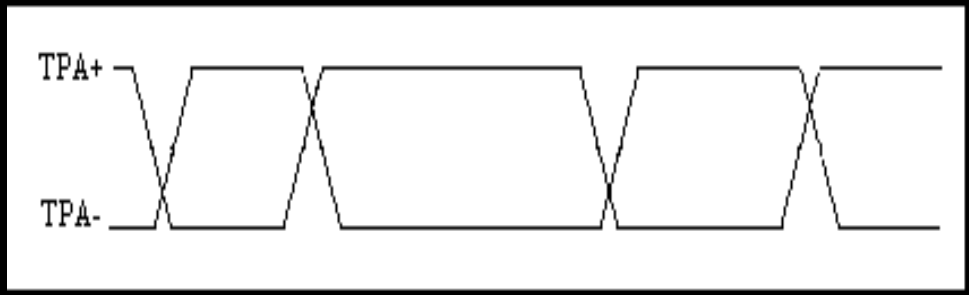


Etch length of twisted pairs

- Match etch length of the twisted pair lines
  - Reduce skew
  - Change in length will result in change in timing relationship This will reduce the skew margin of the signal



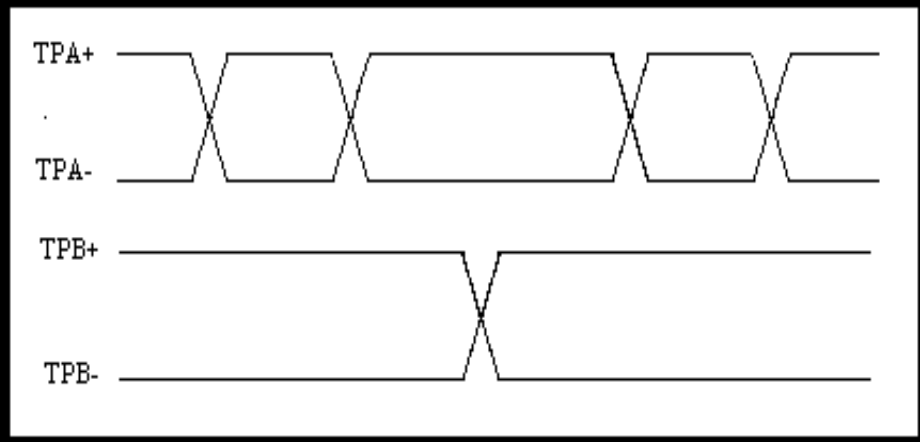
Matched Length



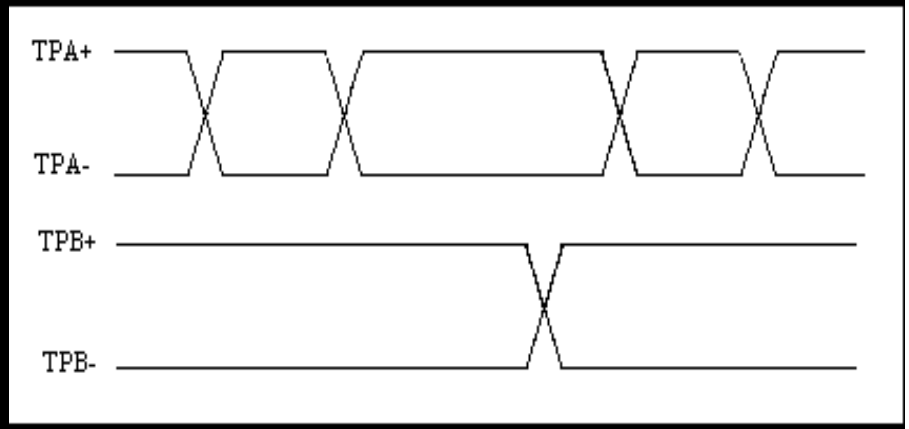
TPA- Longer

Etch length of twisted pairs

The etch length of the TPA and the TPB must be matched. The Data Strobe encoding of the data sent across the twisted pairs depends on the relative timing between 1 and 0 being signaled on the TPA and TPB. If there is a change in delay, there is a change in timing relationship.



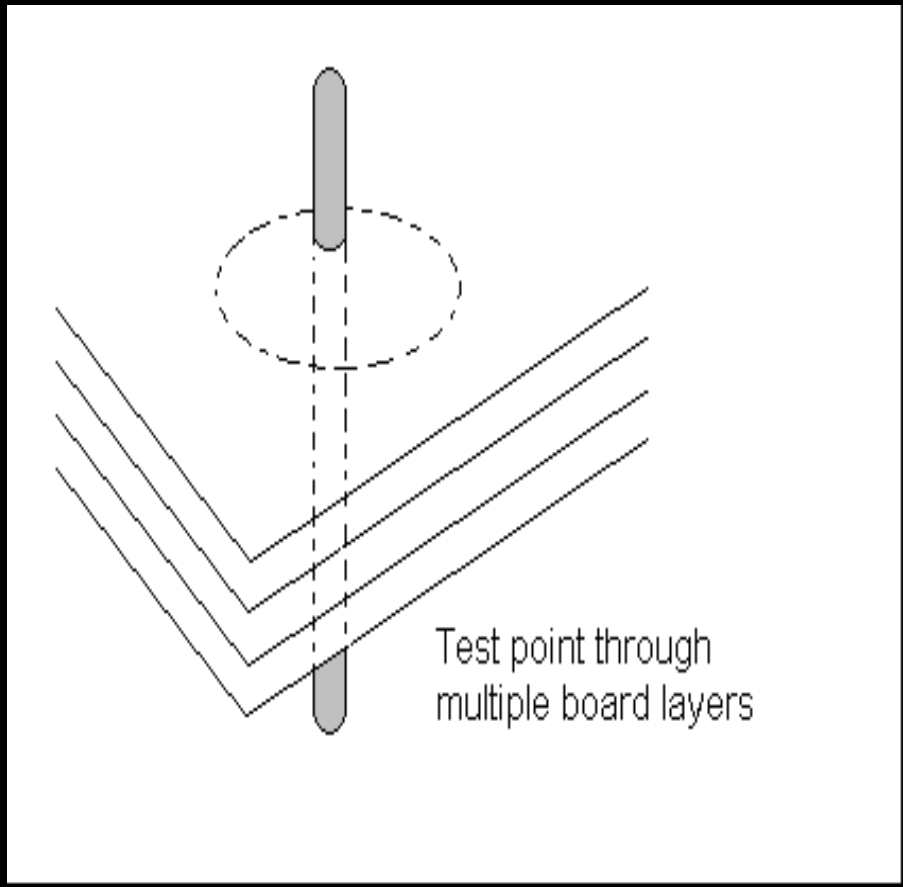
TPA and TPB are matched



TPB is longer

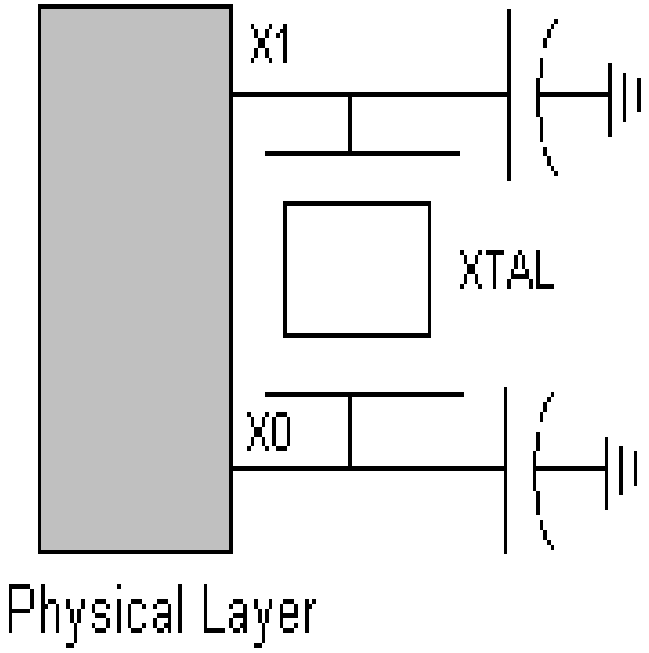
Vias on PCB layout

- Want to minimize disruptions to TP lines
  - Minimize number of via on a twisted pair
  - Increase clearance size around via to minimize capacitance
  - Through hole pins add inductance to transmission lines



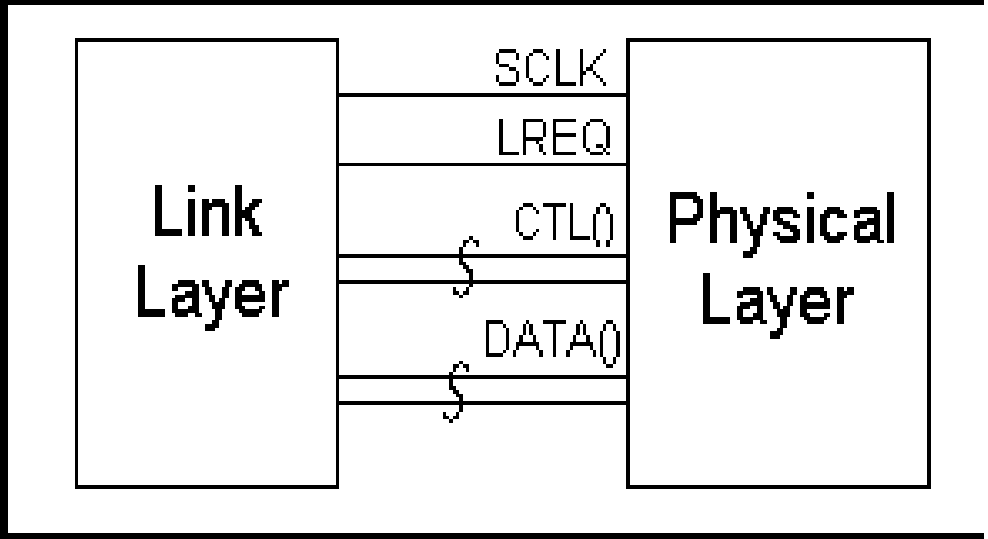
Maintaining clock frequency

- Keep crystal ACAP to PHY
- Longer distance may allow noise to couple in that will interfere with the PLL frequency lock
- The crystal and internal oscillator drive the PLL which generates the reference signal
- The reference signal controls the transmission of the data and strobe signals
- It also controls the clock sent to the link to synchronize the PHY-Link interface



PHY-Link interface

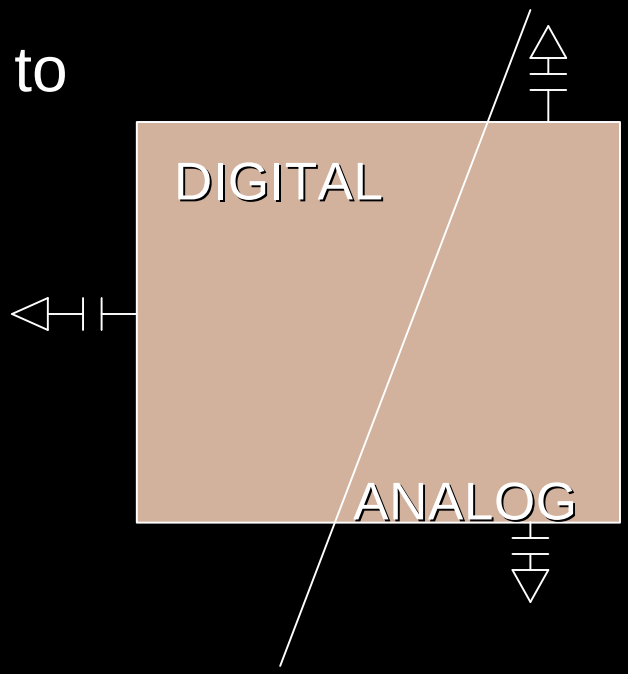
- Maintain equal lengths to reduce propagation delay mismatch
- Keep interface length short
  - Minimize coupled noise
  - Minimize signal loss



Decoupling Capacitor Network for PHYs

Reduce noise across power plane

- We recommend 2 caps per pin. Minimize trace length from Cap to pin, and from Cap to GND.



- A more aggressive strategy is
  - Use two 0.1 *f* caps on the analog plane
  - Use one 0.1 *f* on the digital plane
  - Use 0.01 *f* on the PLLVDD
  - Use 0.001 *f* ACAP on the remaining of the VCC pins

In other words we always recommend a minimum of adecoupling cap per supply pin (or group of all adjacent pins) on the device

EMI Reduction Suggestions

- Series terminate SCLK to help keep a clean clock signal.

- Place resistor ACAP to the PHY. Resistor value is dependent on the characteristic impedance of the board. Series Resistor + Source Impedance ~= Etch impedance

- To reduce EMI from the cable shield and noise coupled on to chassis ground, experiment with different value caps to isolate cable shield ground from chassis ground

- Do not use 90 degree corner traces, causes discontinuities.

EMI Reduction Suggestions

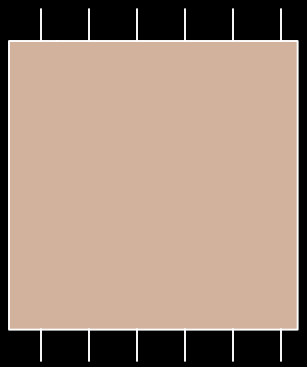
- Avoid discontinuities in ground return paths
- Ensure ground return paths are ACAP to signal paths
- Use minimum spacing allowed between each signal in a twisted pair.
- Avoid running Digital CMOS level signals (SCLK) near sensitive analog signals (TP lines, Crystal, etc) when running traces

PowerPAD™ Packaging :

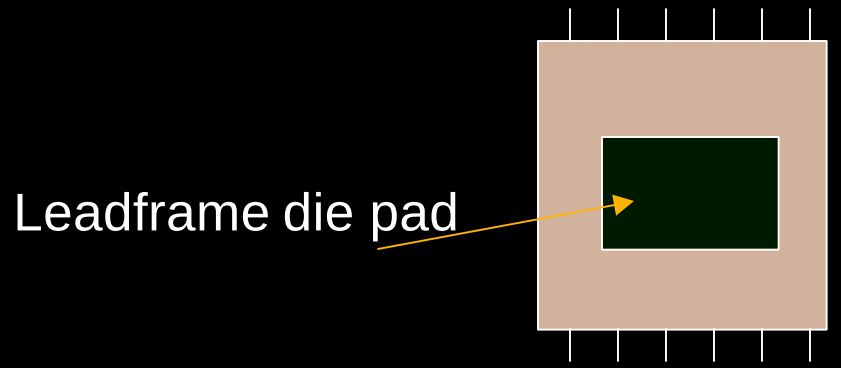
Here is a side by side comparison between the current packaging and the power pad packaging

- In the power pad packaging the lead frame die is exposed at the bottom.

Typical Package



PowerPAD Package

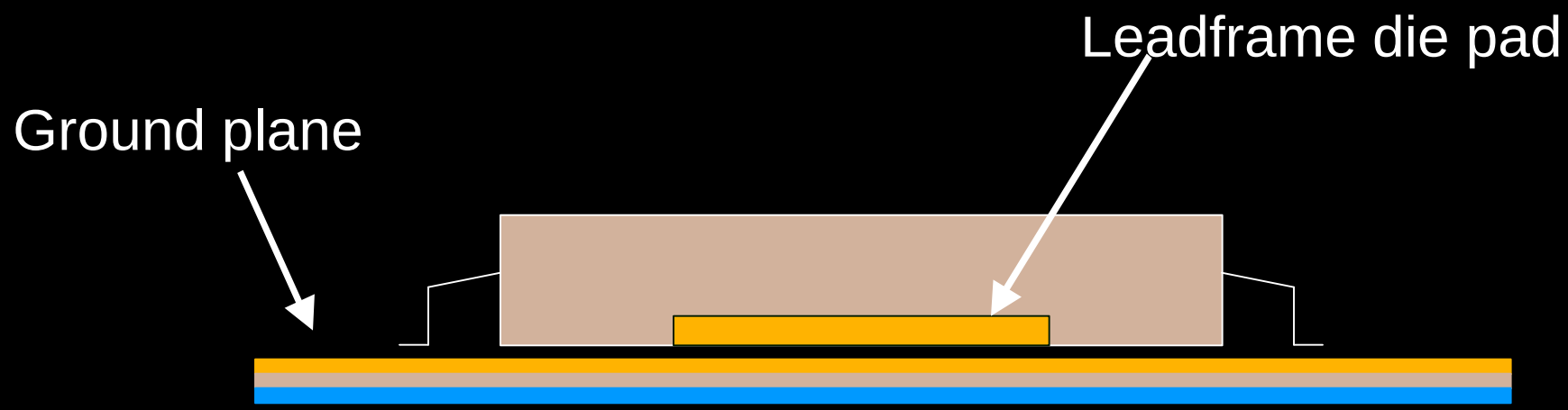


Bottom view of different packages

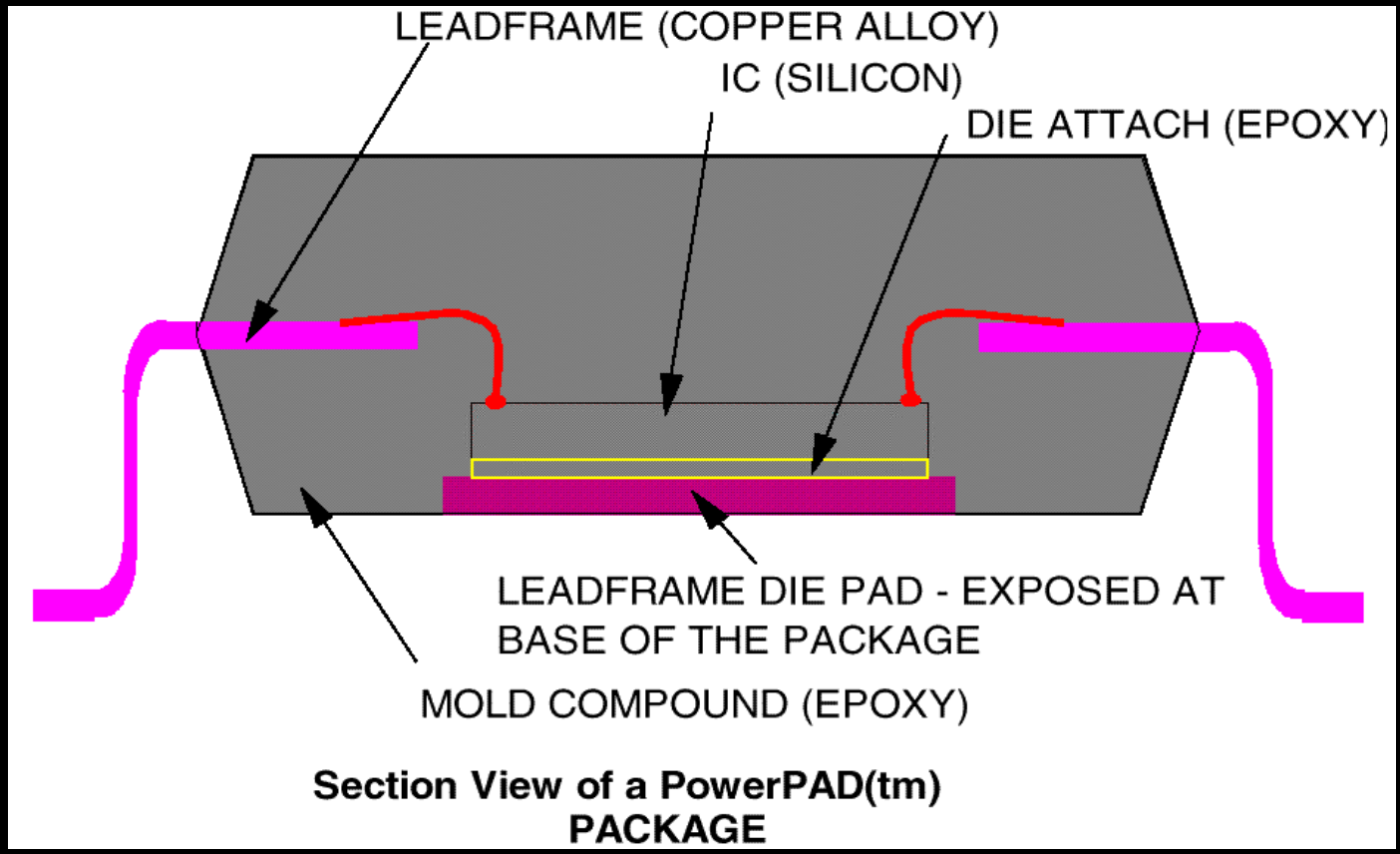
PowerPAD™ Packaging :

- The thermal die pad at the bottom of the device is directly connected to the silicon die.

- A PCB layout that uses power pad packaged components has no requirement for a special layout. But, a special layout will improve thermal characteristics. Connecting the leadframe die pad to a PCB thermal pad or heat sink significantly improves the thermal performance of the package.



PowerPAD™ Packaging gives: ThetaJA of 17.3, ThetaJC of 0.12 (PZP package) with no cost addition



References

- TI web sites

http://www.ti.com/sc/1394

http://www.ti.com /sc/docs/psheets/appnote.htm

- Appnotes:
  - PCB Layout for Improved EMC ***SDYA011***
  - PHY Layout ***SLLA017***
  - The Bypass Cap in High-Speed Environment ***SCBA031***
  - EMI Prevention in Clock Distribution Circuits ***SCAA031***
  - Power Pad Thermally Enhanced Package ***SLMA002***