Advanced Information

TEXAS INSTRUMENTS
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CDC924 133-MHz CLOCK SYNTHESIZER/DRIVER

FOR PC MOTHERBOARDS WITH 3-STATE OUTPUTS

SEPTEMBER 1998

- **Uses a 14.31818 MHz Crystal Input to**
- **Generate Multiple Output Frequencies**
- **Includes Spread Spectrum Clocking (SSC)**
- **Power Management Control Terminals**
- **Low Output Skew and Jitter for Clock Distribution**
- **Operates from 2.5-V and 3.3-V Supplies**
- **Packaged in 56-Pin SSOP Package**
- **Consumes less than 200-μA Quiescent Current**

description

The CDC924 is a clock synthesizer/driver that generates system clocks necessary to support Intel processor-based computer systems on CPU, CPU_DIV2, 3V66, PCI, APIC, 48-MHz, and REF clock signals. All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input instead of a crystal can be provided at the XIN input. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequency. On-chip loop filters and internal feedback eliminate the need for external components.

The host and PCI clock outputs provide low-skew and low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected via control inputs SEL0, SEL1, and SEL133/100.

The outputs are either 3.3-V or 2.5-V single-ended CMOS buffers. With a logic high-level on the PWR_DWN terminal, the device operates normally, but when a logical low-level input is applied, the device powers down completely, with the outputs in a low-level output state. When a high-level is applied to the PCI_STOP or CPU_STOP, the outputs operate normally. With a low-level applied to the PCI_STOP or CPU_STOP terminals, the PCI or CPU and 3V66 outputs, respectively, are held in a low-level state.

The CPU bus can operate at 100 MHz or 133 MHz. Output frequency selection is done with corresponding setting for SEL133/100 control input. The PCI bus frequency is fixed to 33MHz. Because the CDC924 is based on PLL circuitry, it requires a stabilization time to achieve phase lock of the PLL.

This stabilization time is required following power up as well as changes to the SEL inputs. With use of an external reference clock, this signal must be fixed-frequency and fixed-phase before the stabilization time starts.

function tables

SELECT FUNCTIONS

INPUTS†			OUTPUTS							FUNCTION
SEL133/$\overline{100}$	SEL1	SEL0	CPU	CPU_DIV2	3V66	PCI	48MHz	REF	APIC	
L	L	L	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	3-state
L	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
L	H	L	100 MHz	50 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
L	H	H	100 MHz	50 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on
H	L	L	TCLK/2	TCLK/4	TCLK/4	TCLK/8	TCLK/2	TCLK	TCLK/16	Test
H	L	H	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Reserved
H	H	L	133 MHz	66 MHz	66 MHz	33 MHz	Hi-Z	14.318 MHz	16.67 MHz	48-MHz PLL off
H	H	H	133 MHz	66 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	16.67 MHz	48-MHz PLL on

† SEL0 and SEL1 are pulled high internally to allow for normal operation when not connected. SEL133/100 needs an external connection (low or high) for normal operation.

ENABLE FUNCTIONS

INPUTS†			OUTPUTS							INTERNAL	
$\overline{\text{CPU\_STOP}}$	$\overline{\text{PWR\_DWN}}$	$\overline{\text{PCI\_STOP}}$	CPU	CPU_DIV2	APIC	3V66	PCI	PCI_F	REF, 48MHz	Crystal	$\overline{\text{VCOs}}$
X	L	X	L	L	L	L	L	L	L	Off	Off
L	H	L	L	On	On	L	L	On	On	On	On
L	H	H	L	On	On	L	On	On	On	On	On
H	H	L	On	On	On	On	L	On	On	On	On
H	H	H	On	On	On	On	On	On	On	On	On

† CPU_STOP and PCI_STOP are pulled high internally. PWR_DWN is pulled low internally.

OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V_{CC} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
CPU, CPU_DIV2, APIC	2.375 – 2.625	13.5 – 45	TYPE 1
48MHz, REF	3.135 – 3.465	20 – 60	TYPE 3
PCI, PCI_F, 3V66	3.135 – 3.465	12 – 55	TYPE 5

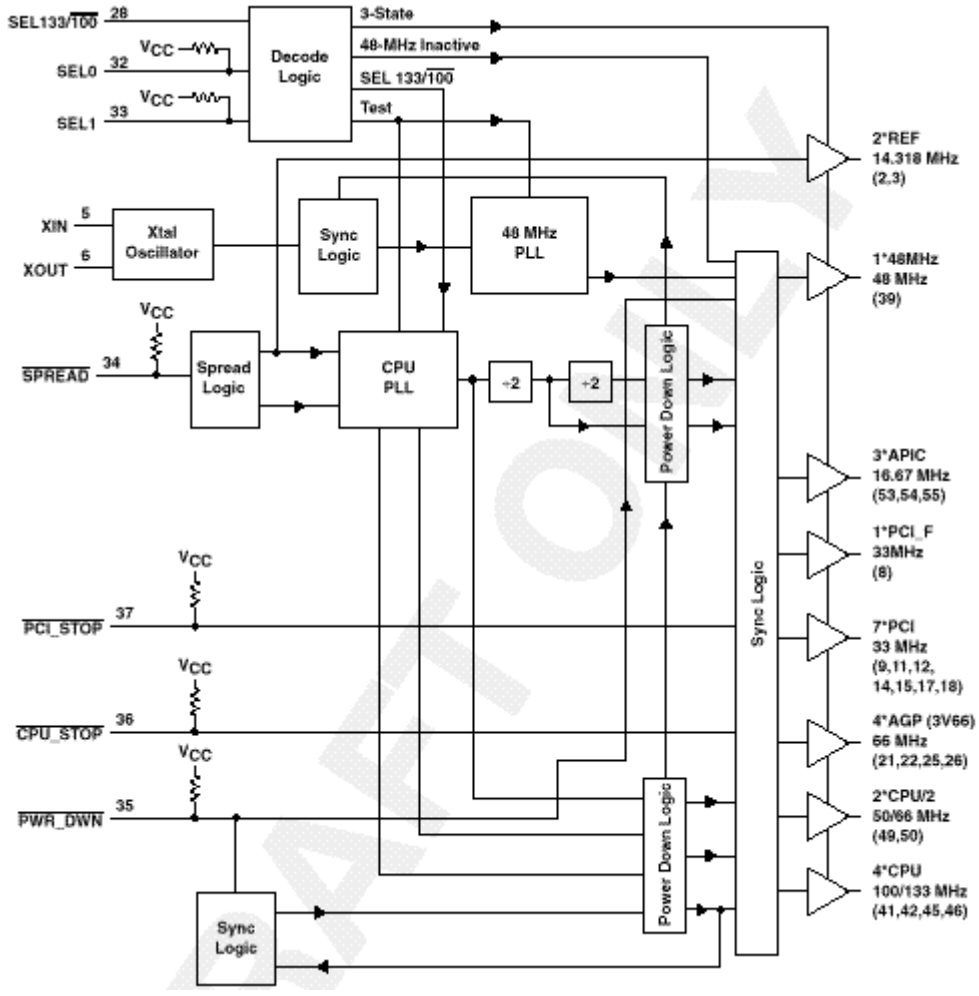
Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
3V66 [0–3]	21, 22, 25, 26	O	3.3 V, Type 5, 66-MHz clock outputs
48MHz	30	O	3.3 V, Type 3, 48-MHz clock output
APIC [0–2]	53, 54, 55	O	2.5 V, Type 2, APIC clock outputs at 16.67 MHz
CPU [0–3]	41, 42, 45, 46	O	2.5 V, Type 1, CPU clock outputs
CPU_DIV2 [0–1]	49, 50	O	2.5 V, Type 1, CPU_DIV2 clock outputs
$\overline{\text{CPU\_STOP}}$	36	I	Disables CPU clock to low state
GND3V66	20		Ground for the 3V66 outputs
GND48	29		Ground for the 48-MHz outputs
GNDAPIC	52		Ground for APIC outputs
GNDCORE	24, 38		Isolated ground for the core
GNDCPU	40, 44, 48		Ground for CPU outputs
GNDPCI	7, 13, 19		Ground for PCI outputs
GNDREF	1		Ground for REFCLK [0–1] outputs
PCI [1–7]	9, 11, 12, 14, 15, 17, 18	O	3.3 V, Type 5, 33-MHz PCI clock outputs
PCI_F	8	O	Free-running 3.3-V, Type 5, 33-MHz PCI clock output
$\overline{\text{PCI\_STOP}}$	37	I	Disables PCI clock to low state
$\overline{\text{PWR\_DWN}}$	35	I	Power down for complete device with outputs forced low
REF0, REF1	2, 3	O	3.3 V, Type 3, 14.318-MHz reference clock output
SEL0, SEL1	32, 33	I	LVTTL level logic select terminals for function selection
SEL133/$\overline{\text{100}}$	28	I	LVTTL level logic select pins for enabling 100/133 MHz
$\overline{\text{SPREAD}}$	34	I	Disables SSC function
V_{CC}3V66	23		Power for the 3V66 outputs
V_{CC}48	31		Power for the 48-MHz outputs
V_{CC}APIC	56		Power for APIC outputs
V_{CC}CORE	27, 39		Isolated power for the core
V_{CC}CPU	43, 47, 51		Power for CPU outputs
V_{CC}PCI	10, 16		Power for PCI outputs
V_{CC}REF	4		Power for REFCLK [0–1] outputs
XIN	5	I	Crystal input – 14.318 MHz
XOUT	6	O	Crystal output – 14.318 MHz

ADVANCED INFORMATION

concerns new products that are in the sampling or new production phase of development. Characteristic data and other specifications are subject to change without notice

Functional Block Diagram



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